Conductive Nanotube-based Scanning Probe Microscopy Applications

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Conductive Nanotube-based Scanning Probe Microscopy Applications

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Abstract: This report from the MFGM049M project presents an evaluation of e-beam assisted deposition and welding and conductive carbon nanotube (c-CNT) tips for electrical scanning probe microscope measurements. Conductive CNT tips were used to measure workfunction, 2D dopant concentration, and dielectric damage metrology by several microscopy techniques. Variations in CNT tip conductivity, contact resistance and CNT-to-CNT conductivity during fabrication were determined.

Keywords: Carbon Nanotubes, Measuring Instruments, Scanning Probe Microscopy

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Table of Contents

List of Figures

List of Tables

Acknowledgments

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1 EXECUTIVE SUMMARY

This work aimed to produce conductive carbon nanotube (CNT) scanning probe microscope (SPM) tips supported on Si cantilevers that are suitable for nanometer scale measurements of carrier concentration profiles, variations in workfunction, and variations in low-k dielectric plasma damage. The SPM-based 2D dopant profiling methods studied included tunneling atomic force microscopy, scanning capacitance microscopy, scanning spreading resistance microscopy, and scanning surface potential microscopy, also known as Kelvin probe microscopy.

Xidex, University of Tennessee at Knoxville (UTK), and the National Institute of Standards and Technology (NIST) prepared and physically characterized conductive CNT SPM tips using focused ion beam (FIB), scanning electron microscopy (SEM), transmission electron microscopy (TEM), scanning tunneling microscopy (STM), and atomic force microscopy (AFM). NIST developed and electrically characterized CNT tips primarily using current-voltage (I-V) measurements. Variations in CNT tip conductivity, contact resistance and CNT-to-CNT conductivity during fabrication were determined.

This principal goal of this work was to produce conductive carbon nanotube (c-CNT) scanning probe microscope (SPM) tips supported on Si cantilevers for various types of semiconductor metrology techniques. These measurements consisted of nanometer scale measurements of carrier concentration profiles on planar and FinFET structures, variations in workfunctions on test structures, and variations in low-k dielectric plasma damage, all requiring high sensitivity and spatial resolution. The SPM-based 2D dopant profiling methods consisted of scanning capacitance microscopy. Xidex Corp (Austin, Texas), the University of Tennessee at Knoxville, the College of Nanoscale Science and Engineering at the State University of New York at Albany (SUNY-Albany), and the National Institute of Standards and Technology (NIST) prepared and physically modified conductive CNT SPM tips using focused ion beam (FIB) and scanning electron microscopy (SEM) to reduce contact resistance and parasitic capacitance. NIST developed and electrically characterized CNT tips primarily using current-voltage (I-V) measurements to compare resistivity due to tip editing. Variations in CNT tip contact resistance were determined as a function of the tip fabrication and editing process. Data indicate that tips having the CNT grown on Si with the catalyst mix had lower total resistance (240-340 kΩ). The I-V characteristics of the CNT-terminated SPM tips measured by TUNA depended on the history of the contact and the voltage ramp range applied between the sample and the CNT. Only very small currents flowed from the tip to the sample below 1 V applied voltage. At higher voltages, currents are much greater. Measurements to date indicate that the CNTs on these tips have a resistivity on the order of 2e-2 Ωcm, about the same as a moderately doped semiconductor. SCM measurements made on wafers implanted and laser-annealed from 1200-1300°C indicate some variation in diffusion based on the anneal temperature. NIST is continuing work doped FinFETs, work function, and low-k dielectric damage characterization.

2 BACKGROUND

With shrinking device features, sub-10 nm resolution, combined with sufficient detection limits (<1e15 atoms/cm^3), is critical. For example, the 2009 *International Technology Roadmap for Semiconductors* (ITRS) requires lateral/depth spatial resolution of 2.4 nm for 2D/3D dopant profiles in 2012.

Scaling CMOS transistors below a 100 nm channel length has necessitated much shallower junctions and higher doping concentrations in the channel. With increasingly smaller dimensions, the metrology of CMOS devices faces challenges in the deep submicron regime. In particular, the need for sub-100 nm junction depths to improve short channel device performance has increased the need for greater measurement accuracy. Conventional techniques such as secondary ion mass spectrometry (SIMS) have been widely used to evaluate dopant profiles and depths, but this is a destructive and time-intensive technique and does not distinguish electrically active, substitutional dopants from non-electrically active interstitial dopants.

Although several methods such as SIMS and electron microscopy have been developed for 2D profiling, scanning probe microscopy (SPM) techniques have become extremely attractive because of their very high spatial resolution and ability to obtain detailed maps of topography, electrical properties, magnetic and electrostatic forces and other properties. SPM-based 2D dopant profiling methods include tunneling atomic force microscopy (TUNA), scanning capacitance microscopy (SCM), scanning spreading resistance microscopy (SSRM), and scanning surface potential microscopy (SSPM) (otherwise known as Kelvin probe microscopy [KPM]). Table 1 summarizes these techniques.

All of these methods require conductive AFM tips. Since the resolution and contrast of topographic and electrical properties are both dictated by tip geometry and composition, new higher resolution probe tips must be developed, as commercially available tips are inferior for advanced profiling experiments. Specifically, metal-coated silicon tips used for atomic force microscopy (AFM)-based electrical measurements rapidly wear out during operation and their quality/performance cannot be assessed during the measurement. Additionally, commercial conductive AFM tips generally have larger probe diameters, which limit the resolution of the measurement to 100s of nm. The large pyramidal and tapered cone-like shapes also prohibit accurate characterization of smaller nanoscopic features and high aspect ratio structures. Longer, sharper conductive AFM tips (with smaller tip radii) are needed for better lateral topographic resolution (< 100 nm) and electrical sensitivity (< 10 mV). Cylindrical (rather than conical) conductive AFM tips are also needed to probe micron-sized structures with densely populated features. Lastly, conductive AFM tips of unknown or ill-defined composition are difficult to calibrate, preventing quantitative analysis of electrical characteristic (capacitance, charge, current, surface potential). In particular, for high level quantitative work, conductive AFM tips

Table 1 Summary of SPM Techniques

SPM Technique	Mode	Probe	Measured Quantity
TUNA or C-AFM	Contact AFM	Metal-coated Si or Metallic; CNT	# of Doping Atoms
			I-V Spectra
SCM	Contact AFM	Metal-coated Si or Metallic; CNT	Depletion Capacitance
			C-V Spectra
SSRM	Contact AFM	Diamond-coated Si; CNT	Electrical Resistance
			I-V Spectra
SSPM or KFM	Intermittent Contact AFM	Metal-coated Si or Metallic; CNT	Electrostatic Potential
			Workfunction

must have well defined geometry, composition, and electrical properties that do not wear or degrade during use. Consequently, carbon nanotube (CNT)-based AFM probes for AFM-based electrical measurements are desirable.

This second phase of work with conductive CNT tips for dopant profiling sought to do the following:

- Evaluate e-beam assisted deposition and welding and conductive CNT tips for electrical scanning probe microscope measurements
- Demonstrate the use of conductive CNT tips for measuring
  - Workfunction
  - 2D dopant concentration
  - Dielectric damage metrology
- Use conductive CNT tips for
  - TUNA measurements
  - SSPM measurements
  - SCM measurements

Xidex-manufactured CNT tips supported on AFM cantilevers are suitable for nanometer scale measurement of carrier concentration profiles. Testing requires the availability of scanning surface potential microscopy (SSPM) and SCM AFM modules.

3 EXPERIMENT

3.1 CNT Tip Fabrication

Xidex fabricated CNT tips supported on Si based cantilevers. In earlier work, Xidex the manual mounting and direct-growth of CNT tips were investigated; manufacturing techniques were to be improved later using electron-beam induced deposition (EBID). Manual mounting of CNT tips was a better short-term solution that allowed different cantilever substrates to be studied, such as Si-based cantilevers coated with different metals. Direct growth of CNT tips is more scaleable but requires research into direct growth of CNTs on a metal-coated Si base. The CNT tips had diameters of 7–20 nm and lengths from 56–750 nm.

3.1.1 Manually Mounted CNT Tips

Conductive CNT tips provided to NIST at the start of the project were fabricated by manually mounting a CNT on the apex of a Si AFM tip, as illustrated in Figure 1, using Xidex's commercially available NanoBot nanomanipulator installed in the sample chamber of Xidex's Hitachi S4000 SEM. The manually mounted CNTs were initially held in place by van der Waals attraction and then welded to the AFM tip using e-beam induced deposition of carbon. The attachment strength, and hence longevity of manually mounted CNT tips can approach that of grown CNTs; however, manual mounting is a less scaleable process. CNT tips of this kind are shown in Figure 2a.

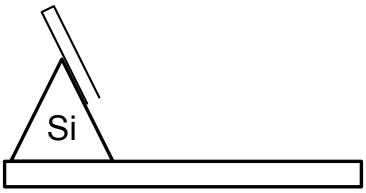
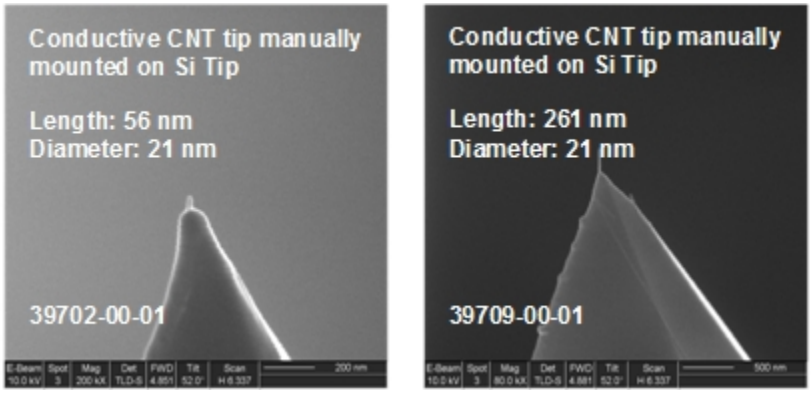
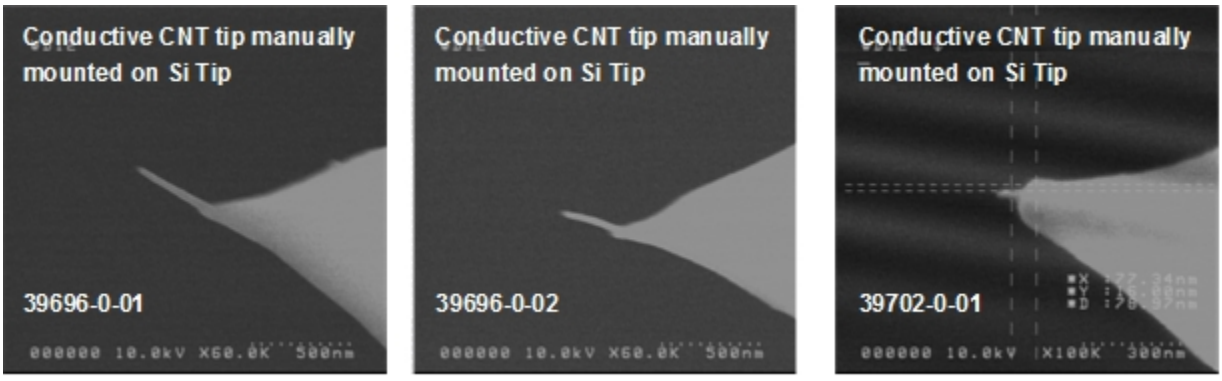


Figure 1 Conductive CNT Tips Provided to NIST



a)



b)

Figure 2 Manually Mounted CNT Tips Provided to NIST

3.1.2 CNT Tips Grown on Si Tips

Another method of CNT tip fabrication was to grow the CNT tip on a Si tip without modifying the conductivity of the probe. The Si tip was coated with Xidex's proprietary catalyst mix, as illustrated in Figure 3. Afterward, the CNT was grown directly from the Si tip using Xidex's thermal chemical vapor deposition (CVD) system.

Examples of conductive CNT tips grown on Si tips are shown in Figure 4a. Additional examples of conductive CNT tips grown on Si tips are shown in Figure 4b.

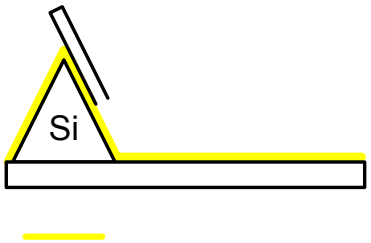
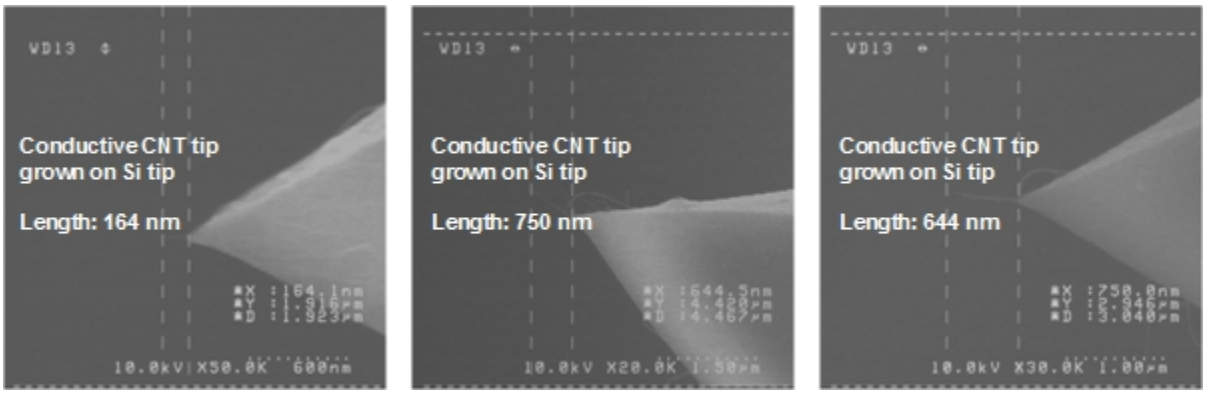
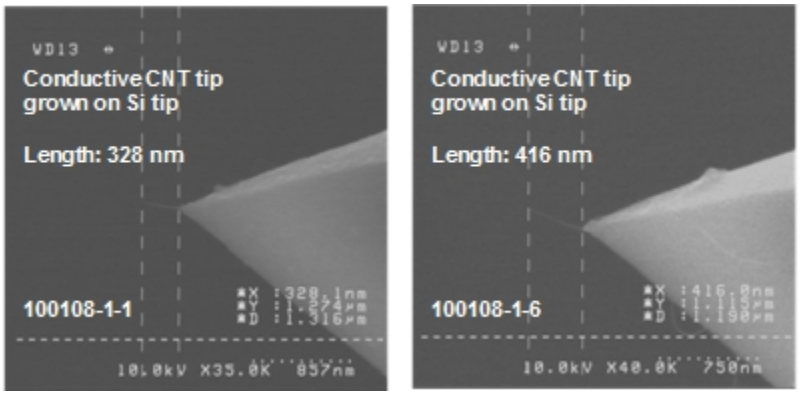


Figure 3 CNT Tip Grown on Si Top



a) UTK



b) NIST

Figure 4 Examples of Conductive CNT Tips Grown on Si Tips Provided to a) UTK and b) NIST

3.1.3 Improved Conductivity for CNT Tips

The differences in contact the resistance of Xidex-fabricated CNT tips on a doped Si substrate and on a Si substrate coated with metal (Pt, Pt-Ir, or Au) were evaluated by NIST. Total tip + probe + cantilever contact resistance is a critical factor in electrical AFM measurements. Enhanced electrical contact between the CNT and the substrate is needed. E-beam assisted welding of the CNT to the substrate to enhance the electrical contact was investigated along with coating the CNT tip with a thin metal layer after the CNT tip is manufactured. The coating was

created by evaporation (thermal or beam) or sputtering. For this work, coating metals were Ag and Al.

3.1.3.1 Contact Resistance in CNT-based Devices

CNT-metal contact resistance is caused by three major factors: 1) constriction of current due to geometry, 2) local chemistry between the CNT and contact, and 3) alignment of the CNT and contact Fermi levels. Each of these factors is difficult to control [1]. Metal-contacts used by other investigators include Al [2], Ti [2] [5], Pt [5] [6], Rh [3], Au [7], and Pd [2] [4]. Pd is widely considered the best Ohmic contact for CNT-based hole conducting devices [2]. Hydrogen saturation increases electron conductivity while decreasing hole conductivity for Pd contacts [4]. Schottky barriers are minimized for CNTs above 2 nm in diameter [3] [4]. Rh has been shown to have similar Ohmic characteristics, comparable to Pd [3]. Pt forms non-ohmic contacts to CNTs [5] [6]. The geometry of contact (side or end) has been shown to give similar device performance [6]. Additional details are in Ref. [8].

3.1.3.2 CNT Tips Grown on Si Tips Coated with Ag

The Si tip must be made more conductive before growing a CNT tip on it. A typical AFM probe is made of doped Si, which is not very conductive. Hence, the Si tip was coated with an Ag layer, as shown n Figure 5, to make the CNT tip suitable for electrical measurements. The following process for fabricating CNT tips was successful: 30 nm of Ag by was deposited thermal evaporation, followed by Xidex's standard proprietary catalyst mix layer; upon chemical vapor deposition (CVD), the CNT tip was grown on the Si tip coated with Ag. Subsequent electrical testing showed that the addition of the Ag layer improved overall probe conductivity.

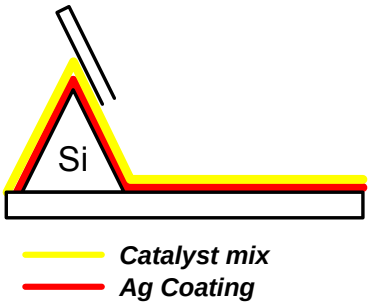
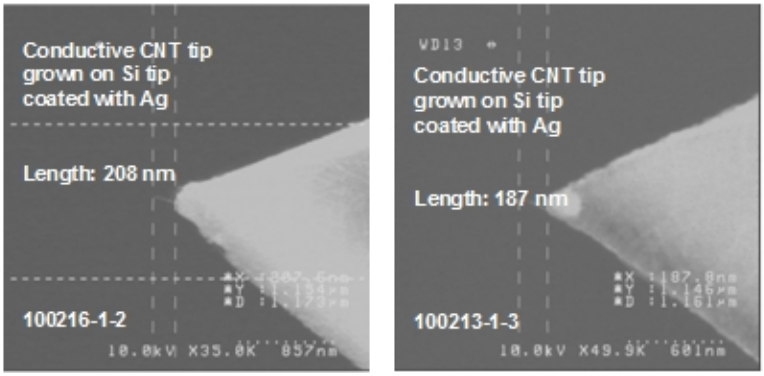


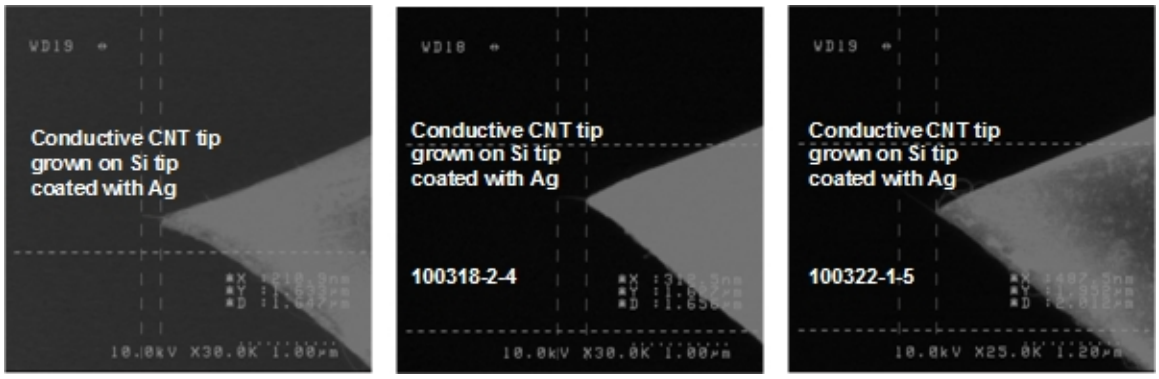
Figure 5 CNT Tip Grown on Si Tip Coated with Ag

The criterion for a coating was that the metal had to be deposited by thermal evaporation because that particular tool was available. This therefore precluded Pt and similar metals that must be sputtered. Pd can thermally evaporate, obtaining a good electrical connection between the Pd and the CNTs, but Pd also promotes the growth of curved (not straight) CNTs. However, Pd has not been tested for growth of a single CNT tip, just many CNTs. In short, the choice of Ag was driven by cost, tool availability, and CNT growth considerations.

Examples of conductive CNT tips grown on Si tips coated with Ag are shown in Figure 6a. Additional examples of such tips are shown in Figure 6b.



a) NIST



b) UTK

Figure 6 Examples of Conductive CNT Tips Grown on Si Tips Coated with Ag Provided to a) NIST and b) UTK

3.1.3.3 Fabricated CNT Tips

Thirty-nine CNT tips were fabricated during the course of the project. These are summarized in Appendix A.

3.1.3.4 Welding to Improve Conductivity

Electron-beam induced deposition (EBID) of metal was used to weld the CNT to the tip, shown in Figure 7, to improve the electrical conductivity between the CNT and the AFM tip (whether coated with Ag or not). The EBID process at UTK was used for welding CNT tips. The approach was evaluated by electrical tests.

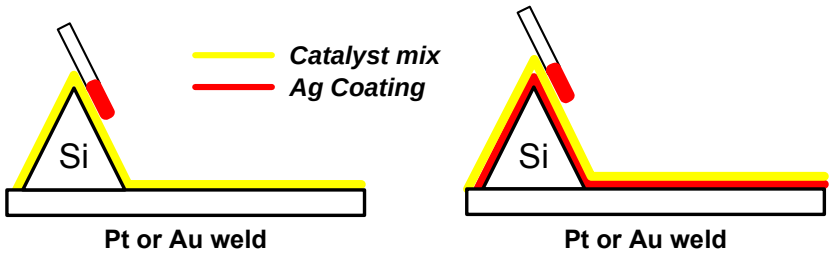


Figure 7 Welding to Improve Conductivity

3.1.3.5 Metal Coating

An alternative way to fabricate CNT tips was also investigated. The CNT was grown first and then the electrical connectivity between the CNT and the substrate was improved by coating the entire CNT and the substrate with a layer of metal. This approach offered the potential to be more scaleable (large-scale manufacturability) than electron beam welding.

First, a Si tip was coated with an Ag layer to make the Si more conductive, followed by coating the tip with Xidex's proprietary catalyst mix. The CNT tip was then grown directly from the tip, as shown in Figure 8. Figure 9a shows a sample CNT tip at this stage of fabrication. Next, a 30 nm thick layer of Ag was deposited, covering the CNT uniformly, as shown in Figure 9b. Since the Ag covering appeared to have cracks, the effects of the thermal annealing on the coating were tested. The Ag-coated CNT was annealed at 400°C for 30 minutes under Ar atmosphere; however, the annealing condensed the Ag into balls at equal spaces on the CNT, as shown in Figure 9c. This tip was not electrically tested only one was made.

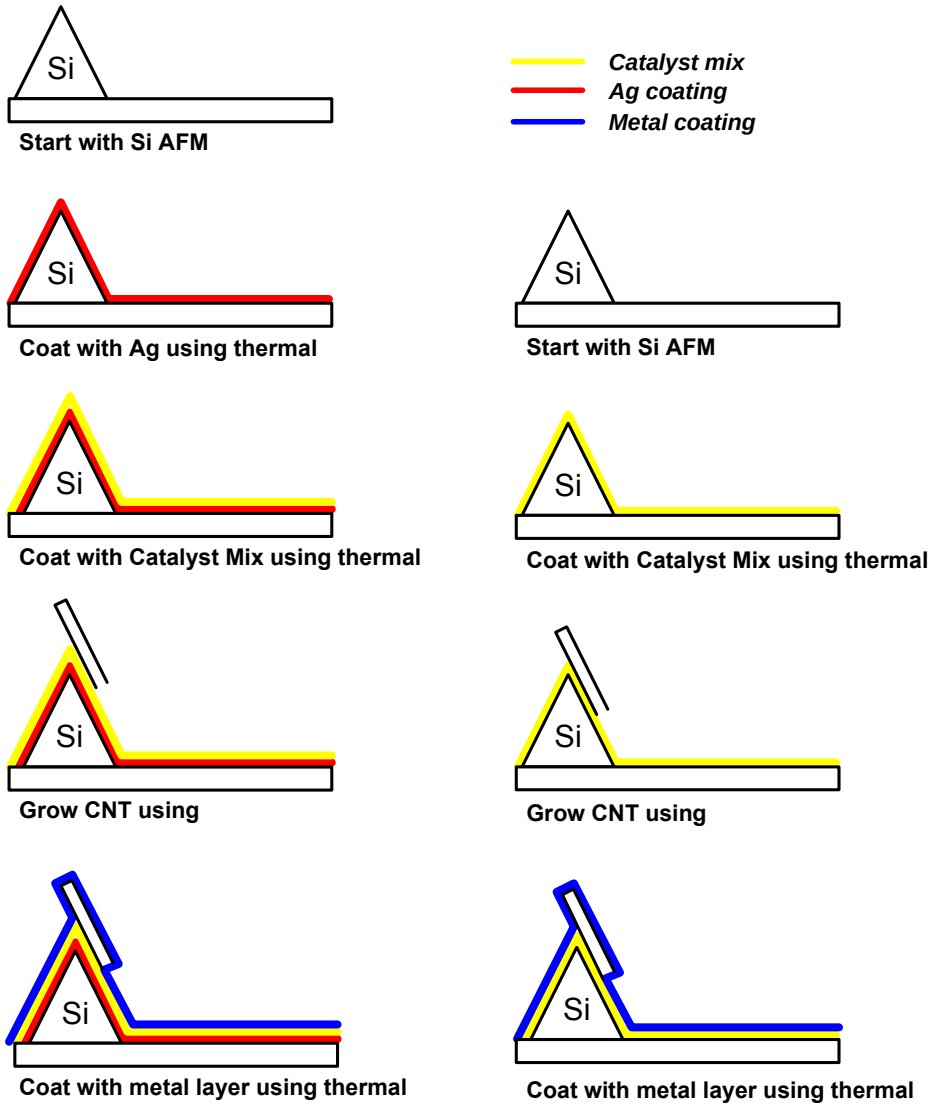


Figure 8 Metal Coating to Improve Conductivity

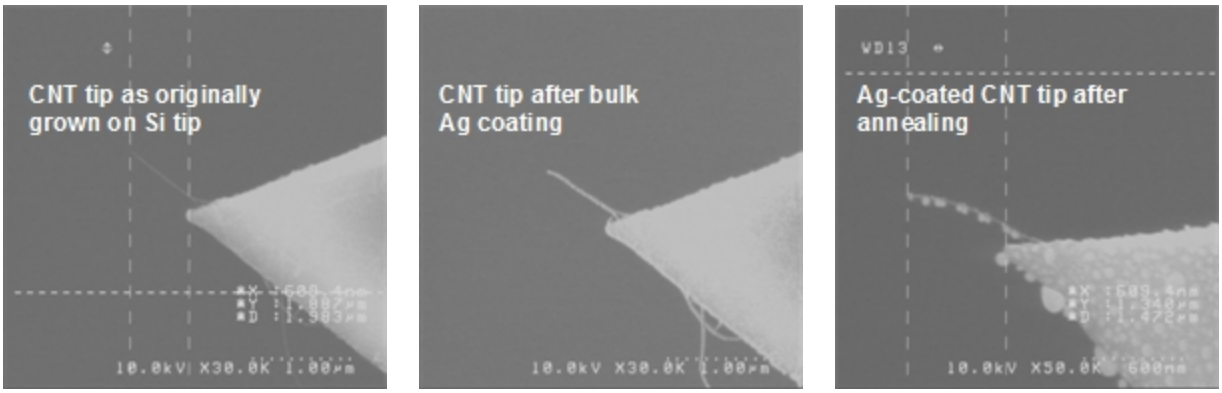


Figure 9 Example of Metal Coating: a) Original CNT Grown on Si; b) After Coating with Ag, and c) Ag-coated CNT Tip after Annealing

3.1.4 e-Beam Assisted Deposition and Etching

E-beam assisted deposition is illustrated in Figure 10, in which e-beam assisted metal deposition was used to weld the CNT to the substrate. As shown in Figure 10a, a gaseous precursor flows through a gas injection system (GIS) and subsequently adsorbs on the substrate. Electrons break precursor bonds near the beam (~10 nm deposit resolution), resulting in decomposition (Figure 10b). Target and impurity atoms incorporate into the film, while volatile byproducts desorb and are removed by the pumping system (Figure 10c). If the precursor gas is an etchant, the decomposition products form reactive radicals that volatilize the surface, resulting in material etching.

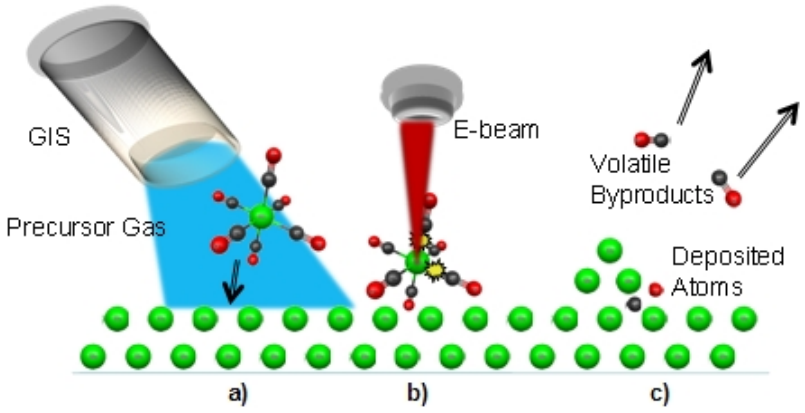


Figure 10 e-Beam Assisted Welding

e-Beam assisted dielectric deposition onto the CNT tip (except the apex) was investigated to reduce the parasitic capacitance of the tip with respect to the sample. Platinum was deposited by the College of Nanoscale Science and Engineering (CNSE) (~40 nm diameter) between the tip and the cantilever to reduce the contact resistance as shown in Figure 11. Local contact was good, with no perceptible deposition on the CNT. Ion milling was also investigated to support the manufacturing of aligned CNT tips. Xidex also investigated the use of e-beam assisted etching to clean carbon contamination from the CNTs. In addition Xidex investigated approaches to replace the expensive ion mill drilling with e-beam assisted etching of metal, silicon, or metal-coated silicon.

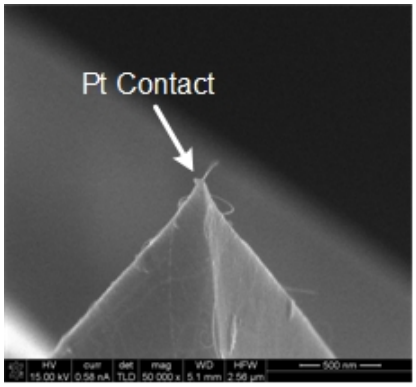


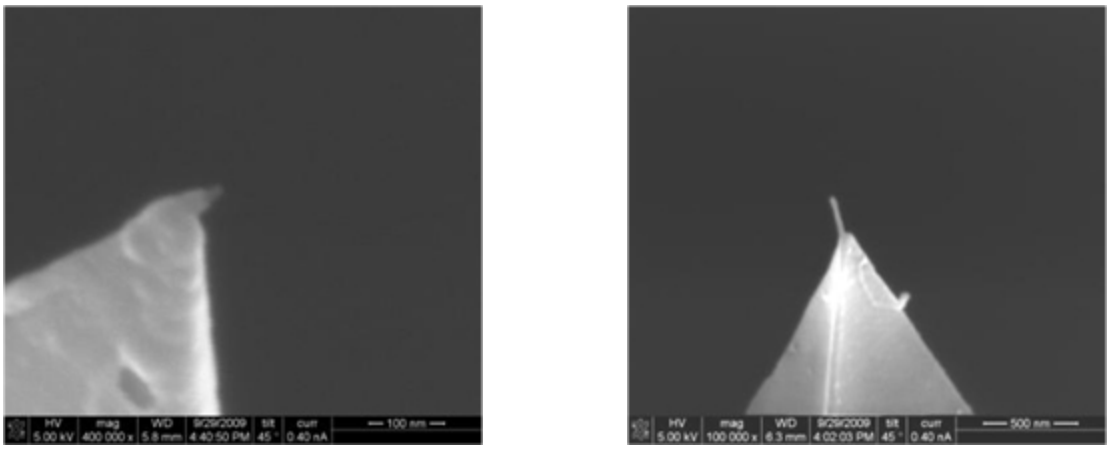
Figure 11 Pt Contact (~40 nm) Deposited Between CNT Tip and Si Cantilever to Reduce Contact Resistance

3.1.5 Demonstration of Electrically Shielded CNT Tips

The feasibility of making electrically shielded CNT tips as proposed above and co-developed with NSF support [9] was also demonstrated. First, a CNT was grown on a Si tip. Next, a SiO layer was deposited that uniformly coated the CNT and the Si tip. The SiO was deposited using thermal evaporation. Next, using the FIB tool at UTK, only the apex of the CNT tip was etched, making the apex electrically conductive while the rest of the CNT and the Si tip were shielded with the dielectric layer. Figure 12 shows the results of etching to expose the apex of a conductive CNT tip coated with SiO. Additionally, three different candidate fabrication techniques involving the use of a dielectric layer to shield a CNT tip and etching to expose the tip apex were proposed [8].

Since the dielectric constant of SiO_2 and SiNx are an order of magnitude better than the SiO, CVD of SiNx onto CNTs was investigated along with etching. Because of the CVD, better dielectric coverage than the evaporation process was expected.

Bundles of CNTs were used instead of individual CNTs on an Si tip, as shown in Figure 13. The recopies for SiNx deposition are discussed in [10], which demonstrates that SiNx deposited on the CNT can be selectively etched without damaging the CNT.



a) As-received AFM tip with CNT and SiO coating

b) Post XeF_2 etch to expose CNT

Figure 12 Conductive CNT Tip Provided to the University of Tennessee at Knoxville

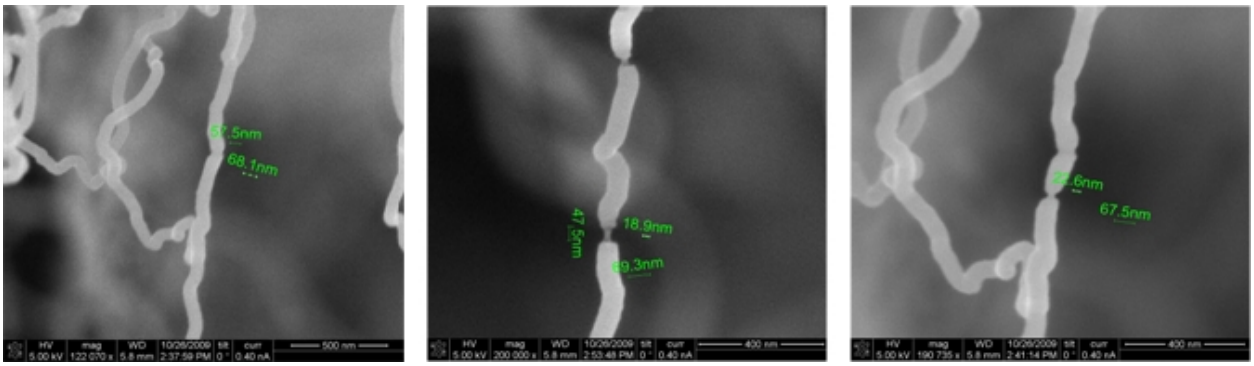
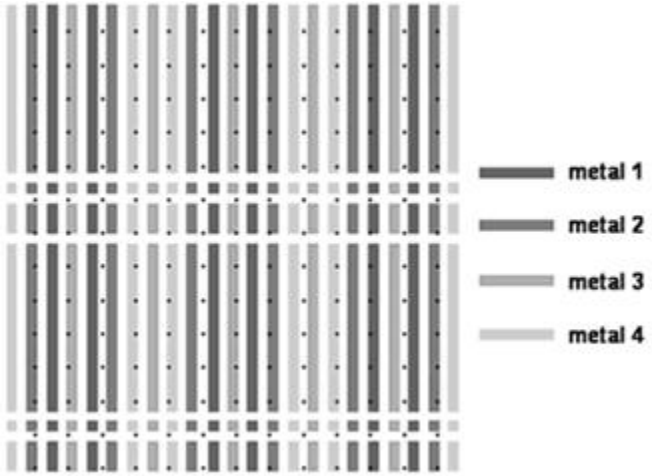


Figure 13 Bundles of CNTs on an Si Tip

3.1.6 Comparison of CNT Tips to Current Best Generation Tips

A variety of tip structures was studied using scanning Kelvin force microscope (SKFM) and intermittent contact scanning capacitance microscope (IC-SCM) measurements using Xidex CNT tips, solid Pt tips (e.g., available from Rocky Mountain Nanotechnology), and PtIr-coated doped silicon tips available from several sources. Test structures included dopant staircase structures, the NIST Kelvin force test structure (Figure 14) and a variety of structures with natural work function variations. Differences in spatial resolution should be apparent from qualitative measurements.



Note: Mask design of a series of broken lines in four different metals, depicted here as four different shades of gray. Various repeat patterns of the four metals are available on the test chip to determine the effect of the neighboring lines on the CPD measured at the tip location. Line width and spacing here is 3 μm; grid dot spacing is 10 μm.

Figure 14 NIST Kelvin Force Test Structure

Available test structures include dopant staircase structures from IMEC, which contain a series of 5-micrometer-wide doped epilayers with dopant concentrations varying from 1E+15 at/cm^{-3} to 1E+20 at/cm^{-3}, the NIST Kelvin force test structure with Au, Cr, and Al lines, and structures with natural work function variations, such as a metal film with segregated domains or crystals with different composition. Theoretical simulations and experimental results show that the CNT improves spatial resolution by greatly reducing the effect of the tip sidewall.

CPD is defined as:

$$CPD = \phi_{tip} - \phi_{sample} \qquad \textbf{Eq. [1]}$$

where ϕ_{tip} is the work function of the tip and ϕ_{sample} is the work function of the sample.

3.1.6.1 Preliminary I-V Characterization of CNT Terminated SPM Tips

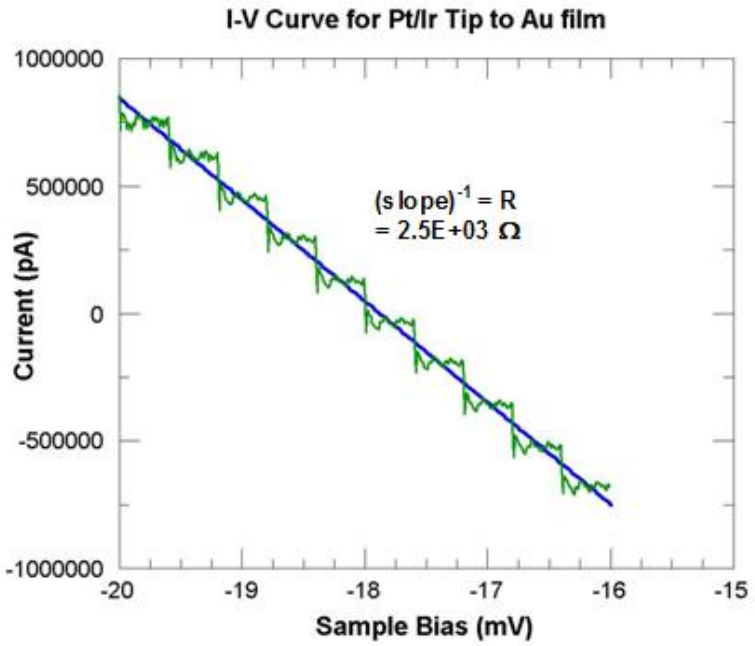
Initial measurements were made to determine the current-voltage (I-V) through the CNT tip using the Veeco extended-TUNA module, which has a current meter integrated in series with the AFM tip. Four current ranges are available: ±10 pA, ±100 pA, ±10 nA, or ±1000 nA. The AFM maintains constant force contact, while the TUNA module conducts an independent I-V measurement. The AFM was engaged with a minimal setpoint difference and is not scanned once contact is made. Samples were either thin Au films or Al films deposited on silicon. The silicon is not in the circuit, because electrical contact is made directly from the film to the conductive sample puck using conducting silver epoxy. The CNT-to-film contact is only part of a series of resistances measured by the TUNA. These resistances are all in series and cannot be separated from each other. From the tip contact, the following resistances were found:

1. CNT-to-sample contact resistance
2. CNT resistance

3. CNT-to-SPM tip contact resistance
4. SPM cantilever sheet resistance
5. Internal AFM wiring resistance
6. Return connection to sample resistance
7. Puck-to-silver epoxy-to-film resistance
8. Film sheet resistance

The resistances of items 5 to 8 can be measured by placing one ohmmeter probe to the surface of the film and the second to the output connection of the cable connected to the puck holder. This total resistance is no more than a few ohms, which is insignificant for these measurements.

To determine the resistance with a typical SPM tip, the I-V between the Au film and a PtIr-coated tip was measured. The resulting I-V curve, shown in Figure 15, is linear with a resistance of 2.5E+03 Ω. It also shows the limitations of the voltage source on the TUNA. The minimum voltage step of the D/A is 0.04 mV. When acquiring the I-V curve, the voltage is not changed until a change of greater than 0.4 mV is requested, hence the steps in the I-V curve. A small offset in the voltage source leads to the I-V crossing the 0 current point at around -18 mV.



Note: Showing artifacts from TUNA data acquisition limitations.

Figure 15 TUNA Measured I-V Curve for PtIr Tip to Au Film Contact

Similar measurements were made using a CNT terminated tip. These are shown using both Au and Al film in Figure 16. The I-V curve characteristic of a CNT-terminated tip was rectifying (highly asymmetric between positive and negative voltages) when contacting the Au film. The I-V curve, when contacting the Al film, was ohmic (symmetric), although slightly S-shaped. This implies that the rectification is at the CNT-to-film contact, since this is the only parameter that changed between the two I-V curves.. The CNT-Au film diode has about a -0.5 V turn-on

voltage and a forward resistance of 9E+05 Ω. The CNT-Al contact has a resistance of about 3E+05 Ω. It is unclear how much of this resistance is due to the CNT, the CNT-tip contact, and the spreading resistance in the silicon cantilever. For these initial measurements, priority was placed on preserving the CNT tip; therefore, the amount of force and of current passing through the tips was critical. The measurements will be repeated at a higher force and higher currents to ensure that the resistance is not being dominated by contact effects, specifically dirt, oxide, or moisture at the CNT-to-film interface.

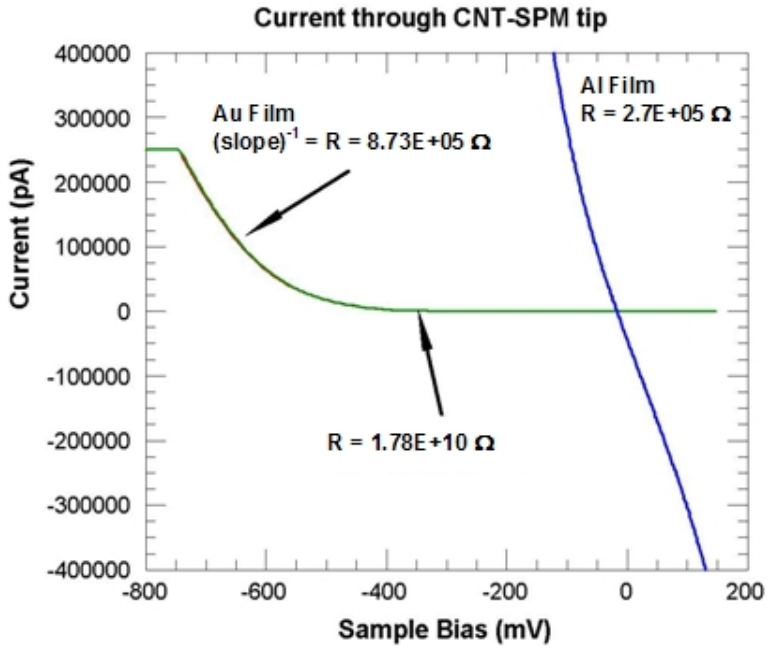


Figure 16 TUNA Measured I-V Curve for CNT Tip to Au Film and CNT to Al Film

3.1.6.2 Initial Scanning Kelvin Force Microscopy Measurements with CNT Tips

Kelvin force microscopy (SKFM) measurements were also made with the same batch of four tips. Again, initial contact was made with minimal engage force. However these tips were scanned (in tapping mode) over a region of about 40 µm. Scanning was performed at slow speeds and with a small contact force setpoint. The setpoint determines the contact force between the tip and sample (the minimum setpoint needed to keep the tip in contact with the sample was used). All tips required several scans for their I-V curves to stabilize. A topography image and the corresponding SKFM images using a conventional PtIr tip and a CNT tip are shown in Figure 17. This structure consists of alternating Au and Al lines, each 5 µm wide, separated by region of p-type silicon with a 5 nm top oxide. Details of an average line scan of both images are shown in Figure 17. In the SKFM images, the contact potential difference of the Au and Al lines is expected to differ by the difference in their work functions. For Au, φ_{au} = 5.1 eV, and for Al, φ_{al} = 4.28 eV, for a difference of 0.82 eV. For the PtIr, a difference in contact potential difference (CPD) of 0.63 eV is observed, in line with previous measurements of this structure. The CNT tip has a much greater difference in CPD, possibly related to the high series resistance of these tips. The width of the lines in the SKFM images was slightly sharper (about 0.2 µm)

(Figure 18). Initial SKFM images with CNT tips showed a dramatic improvement in spatial resolution, but a similar difference in CPD (compared to a PtIr tip) [11].

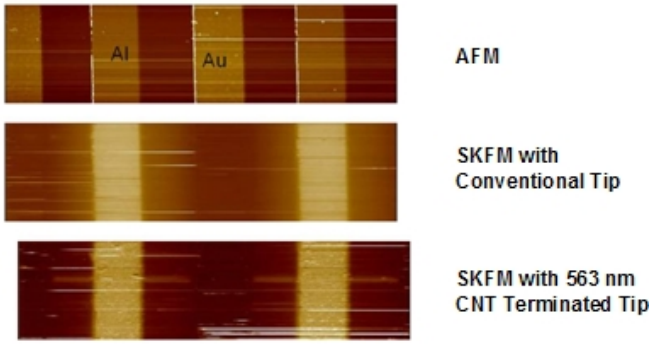


Figure 17 Comparison PtIr and CNT Tips

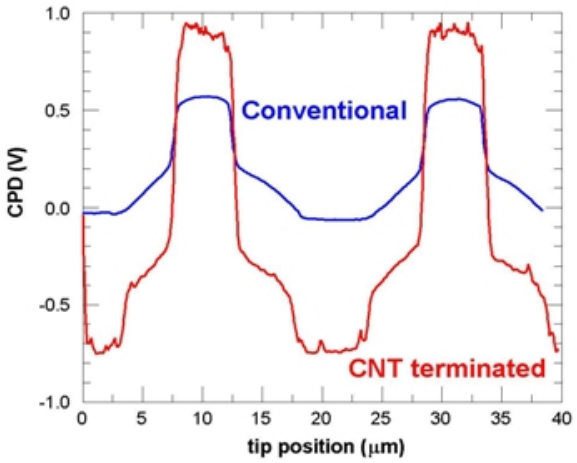


Figure 18 Line Scans Extracted from Figure 17 for a PtIr Tip (blue line) and a CNT Terminated Tip (red line)

3.1.7 Measurement of Tip Work Function Using the NIST Kelvin Force Test Structure

Conductive CNT tip workfunction was studied using a structure consisting of adjacent Al, Cr, or Au lines. Plotting the measured CPD against the known work function of these three metals allows the tip workfunction to be deduced. Repeating the measurement with Pt-, Au-, or Cr-coated tips could increase the certainty with which the workfunction of unknown tips can be deduced.

Knowledge of the resistivity (and total resistance of the CNT-tip assembly) is important for understanding SCM and SKFM electrical measurements. Ideally, the resistance should be low (~1k Ω), but both SKFM and SCM should work with substantial series resistance. It is unclear at what value of series resistance SCM or SKFM would start to deviate substantially from the ideal case. Preliminary measurements showed that the behavior of the CNT-to-metal film was complex, varying with the history of the voltage scan range used to measure the current. Hence, an understanding the behavior of the CNT-to-metal contact emerged as a secondary goal of this work.

3.1.7.1 Theory

The resistivity of the CNTs in this study could be deduced from the simple equation

$$R = \frac{pL}{A} \qquad \textbf{Eq. [2]}$$

where R is the measured resistance in Ω, ρ the resistivity in Ω-cm, A the cross-sectional area, and L the length of the CNT. For reference, typical values of resistivity are 2.2E-08 Ω-cm for Au, 2.2E-02 Ω-cm for silicon doped at 1E+18 cm^{-3}, 4E+0 Ω-cm for silicon doped at 1E+15 cm^{-3}, and 1E+15 Ω-cm for SiO_2. The typical CNT measured here was around 500 nm long with a cross-sectional area of 100 nm^2, suggesting that the measured resistance would be rather high (i.e., $R \approx \rho \times$ 5E+07). A CNT as conducting as gold should have a resistance of around 1E+0 Ω, while one as conducting as highly doped silicon should have a resistance of 1E+04 Ω. A CNT as conducting as lightly-doped silicon should have a resistance of 1E+06 Ω.

In the same manner, another parameter that can be easily calculated is the current density (i.e., the measured current divided by the cross-sectional area of the CNT). For reference, Cu interconnects in integrated circuits carry currents on the order of 10^3 A/cm^2 and are predicted to have problems when current densities exceed 1E+05 A/cm^2. CNTs have been suggested as an alternative to Cu interconnects with the ability to support current densities to 1E+10 A/cm^2 (or as low as 1E+07 A/cm^2, depending on the reference).

3.1.7.2 Evolution of I-V Characteristics in TUNA Measurements of CNT-Terminated Tips

The CNT-terminated tips did not, in general, have linear I-V characteristics; they also changed behavior as progressively larger voltages were applied between the tip and sample. To preserve the tips from possible damage due to excess current flow, initial measurements were made with small applied voltages (± 100 mV). Many, but not all, tips initially showed a capacitive I-V (i.e., a constant current proportional to dV/dt that changed signs when the voltage sweep direction was reversed), as in Figure 19. Applying a higher voltage (± 1V) usually produced a more resistive I-V curve characteristic with a high resistance, on the order of 1E+09 Ω, as in Figure 20. Finally, extending the voltage range to ± 5 V or higher usually caused a contact to "form," resulting in more current flowing, as in Figure 21. This I-V curve characteristic was usually slightly asymmetrical, with the resistance in the forward region as low as 1E+05 Ω. Its magnitude decreased over time or suddenly if the maximum voltage range was decreased. At high enough applied voltages, a diode-like I-V behavior is formed. The effect of "forming" the contact was repeatable when the probe was withdrawn and then re-engaged to contact.

The diode-like behavior is not expected of a CNT-to-Au contact. The workfunction of Au is 5.1 eV; the workfunction of CNTs has been reported between 4.95 and 5.10 eV [12]. However, because the diode is not strongly asymmetrical, the rectification (larger current flow for one voltage polarity versus the opposite polarity) may be due to organic contamination at the CNT-Au junction limiting current flow at low voltages. The I-V curves of at least one of the CNT-to-Al contacts exhibited more S-shaped behavior than diode behavior. This implies that rectification is at the CNT-to-film contact, since this is all that changed between the two IV curves.

The evolution of IV characteristics is not unusual. It is commonly observed with TUNA using small area contacts and surfaces exposed to atmosphere. The high electric fields present at the tip terminus can result in local rapid oxidation or the rapid deposition of organic films. These would

tend to increase the measured resistance. The formation of a better contact at higher applied voltages is the result of the higher current temporarily overcoming this layer of dirt/oxide/moisture.

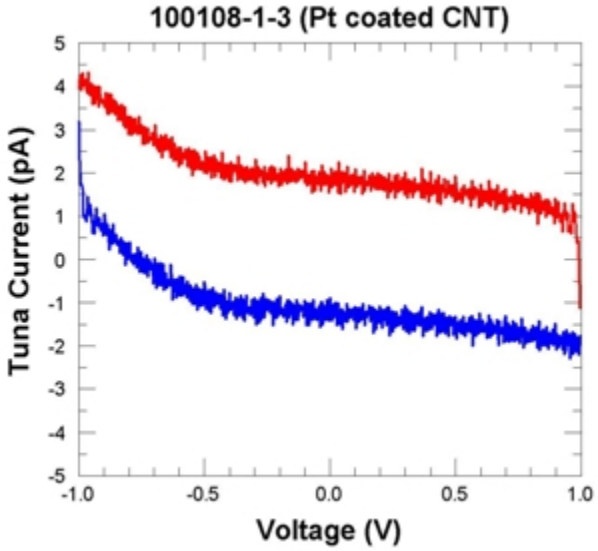


Figure 19 **Typical TUNA I-V Curve "Capacitive" Contact Obtained When First Making Contact and with Low Applied Voltages**

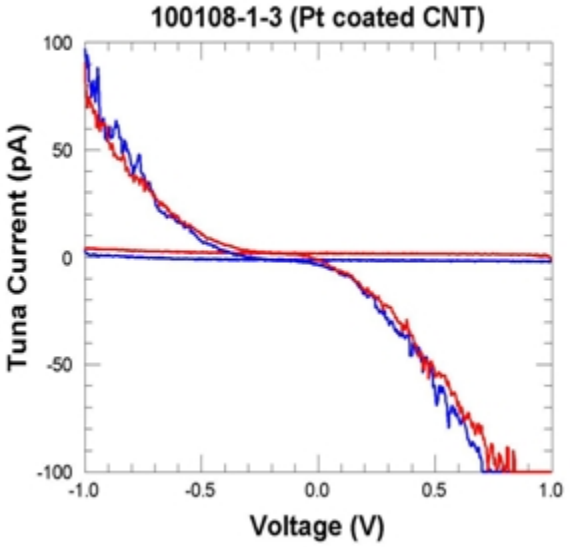
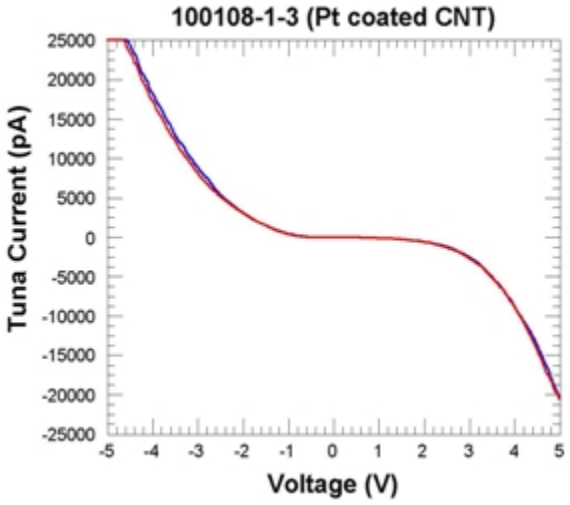


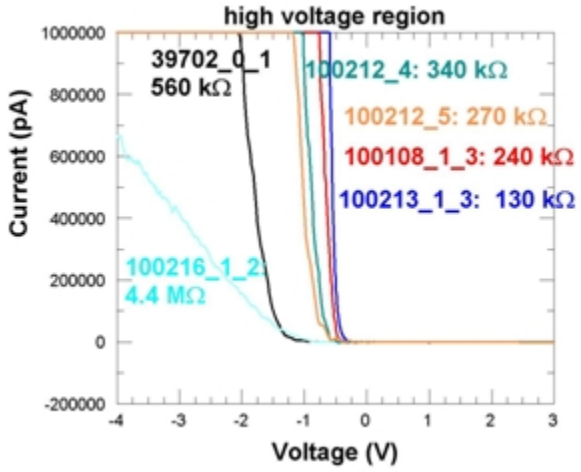
Figure 20 **TUNA I-V Curve Obtained After "Forming" Contact by Briefly Applying -5 V**



Note: IV is diode like, with negative voltages slightly more conductive than positive voltages.

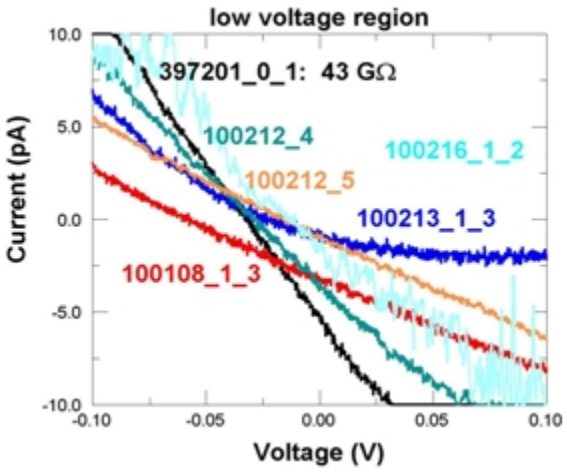
Figure 21 **TUNA I-V Curve Obtained After Applying and Scanning a Larger Voltage (-7 V in this case)**

Figure 22 shows stable diode-like characteristics at higher applied voltages. The turn-on voltage decreases with time at stress, and forward resistance is relatively low at 100–500 kΩ. Figure 23 shows I-V of CNT tips at low applied voltages. This is in the reverse bias region of the diodes and little current flows.



Note: Turn on voltage decreases with time at stress, forward resistance relatively low 100 KΩ to 500 KΩ.

Figure 22 Stable Diode-like Characteristics at Higher Applied Voltages



Note: This is in the reverse bias region of the diodes and low current flows.

Figure 23 TUNA I-V Curve of CNT Tips at Low Applied Voltages

3.1.7.3 Summary of IV Measurements and Extracted Resistivities

Table 2 summarizes tips whose I-V curves were generated using TUNA. Since these I-V curves are diode-like, the resistance near 0 V may essentially be the reverse bias resistance of the diode and more dependent on the Schottky rectification at the contact rather than the intrinsic resistance of the CNT. The resistances near zero applied voltage range from 0.1–43 GΩ. In the forward bias region after the contact "forms," resistance is much less, around 0.5–1 MΩ. Calculating the CNT resistivity from the forward resistance, the CNT length, and an assumed area of 100 nm^2 yields values from 0.6E-02 to 9E-02 Ω-cm. This resistivity is equivalent to silicon doped around 1E+18 at/cm^{-3} (i.e., a moderately doped semiconductor). Because the resistivity calculation is directly proportional to the CNT area, if the CNT area were actually smaller, the resistivity would be proportionally less. The 100 nm^2 value is equivalent to a CNT radius of 6 nm (for a solid tube) or an outer radius of 9 nm (if the tube is hollow with 60% empty space).

Maximum current applied to these CNTs was ~ 1 μA, leading to a current density of 1E+06 A/cm^2 without apparent damage to the CNT. The second number reported in the minimum resistance column is the value for an independent, repeated measurement.

Table 2 Summary of All Tips with I-V Curves Measured with TUNA

Tip ID	Date Rcved	Length	Resistance Near 0V	Minimum Resistance (Ω)	Minimum Resistivity (Ω-cm)
39702-00-01	11-08	56 nm	Not measured		
39709-00-01	11-08	261 nm	Not measured		
39696-0-01	07-09	460 nm	7.8E+09 (@ +1.6 V)		
39696-0-02	07-09	310 nm	2.3E+10 (± 100 mV)		
39702-0-01 (Au substrate)	07-09	56 nm	8.2E+08 (-20 mV)	850 kΩ, 560 kΩ	1.8E-02
39702-01-01 (Al substrate)		56 nm	6.2^{E}+09 (± 500 mV)	540 kΩ	9.6E-02
100108-1-1	02-10	328 nm	1.2E+08		
100108-1-6	02-10	416 nm	2.7E+05 (Al substrate) (±100 mV)		6.5E-03
100212-1-1	02-10	516 nm			
100212-1-3	02-10	563 nm			
100108-1-3	03-10	742 nm (Pt-welded & covered)	9.8E+08	2.3 MΩ, 240 kΩ	3.1E-02
100212-1-4	03-10	484 nm (Pt-welded)	5.4E+10	550 kΩ, 340 kΩ	1.1E-02
100212-1-5	03-10	477 nm (Pt-welded)	9.3E=09	270 kΩ	
100216-1-2	03-10	208 nm (Ag Dep.)	3.2E+09	4.4 MΩ	
100213-1-3	03-10	187 nm (Ag Dep.)	4.1E+09	130 kΩ	

3.1.7.4 Conclusions from TUNA Measurements of CNT-Terminated SPM Tips

The TUNA measured I-V characteristics of CNT-terminated SPM tips depend on the history of the contact and the voltage ramp ranges applied between the sample and the CNT. Only very small currents flow at low (<1 V) applied voltages. At higher voltages, currents are greater. Measurements to date indicate that the CNTs on these tips have a resistivity on the order of 2E-02 Ω-cm, about the same as a moderately doped semiconductor. This should be sufficient for SPM-based electrical measurements.

Pt-welded tips have lower total resistance, as indicated by the minimum resistance shown for tips 100108-1-3 (2.3 MΩ, 240 kΩ), 100212-1-4 (550 kΩ, 340 kΩ), and 100212-1-5 (270 kΩ) in Table 2. Additional experimental evidence is needed to verify this observation. It is not certain that the CNTs always stay on the tips. Some data may be from tips that have fallen off the Si cantilever tips.

It is not certain that the CNTs always stay on the tips. Some data may be from tips that have fallen off the Si cantilever tips.

3.1.8 Evaluation of CNT Tips in SPM Applications for Semiconductor Metrology

3.1.8.1 Measurement of 2d Active Dopant Concentrations

Ultra-shallow junctions are essential for better short-channel performance due to their higher lateral electric fields and lower threshold voltage (V_T) roll-off. Dopant distribution as a result of thermal processing is an important criterion for device performance, and metrology is needed with high sensitivity and spatial resolution.

While device scaling has aggressively shortened the channel length, junction depth has not been reduced as aggressively. Manufacturing issues due to dopant diffusion have limited the use of ultra-shallow junctions. However, parasitic resistance increases as the junction becomes shallower. Device-scale dopant metrology is desirable because it would allow the actual dopant distribution to be determined at the device level, not on a test pad,. However, nanometer-scale probes would be required to access the S/D implant regions
(Figure 24).

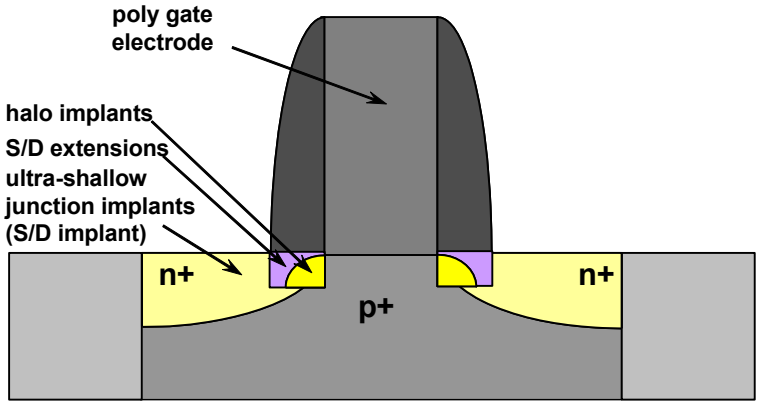


Figure 24 n-Type Transistor Showing Implant Regions

Two-dimensional dopant concentration profiles, important when optimizing transistor performance, were measured using CNTs on patterned substrates provided by SEMATECH.

An SCM system is similar to a MOS capacitor, which is formed by the tip and the sample with an oxide layer on top and a metal layer on the back and biased under depletion conditions, as shown in Figure 25. The SCM signal is seen as the change in capacitance (depletion) per unit of change in the applied AC voltage, dC/dV. Since AC is a voltage waveform, dV is the peak-to-peak voltage [13]. Ohmic contact is made between the sample and sample holder using Al as a backside contact; oxidation of the surface sample is accelerated by ozone. The mathematical calculations of the data obtained by the SCM system is thus similar to a MOS capacitor structure, which is formed by the tip and the sample with an oxide layer on top and biased under depletion conditions [14] [15].

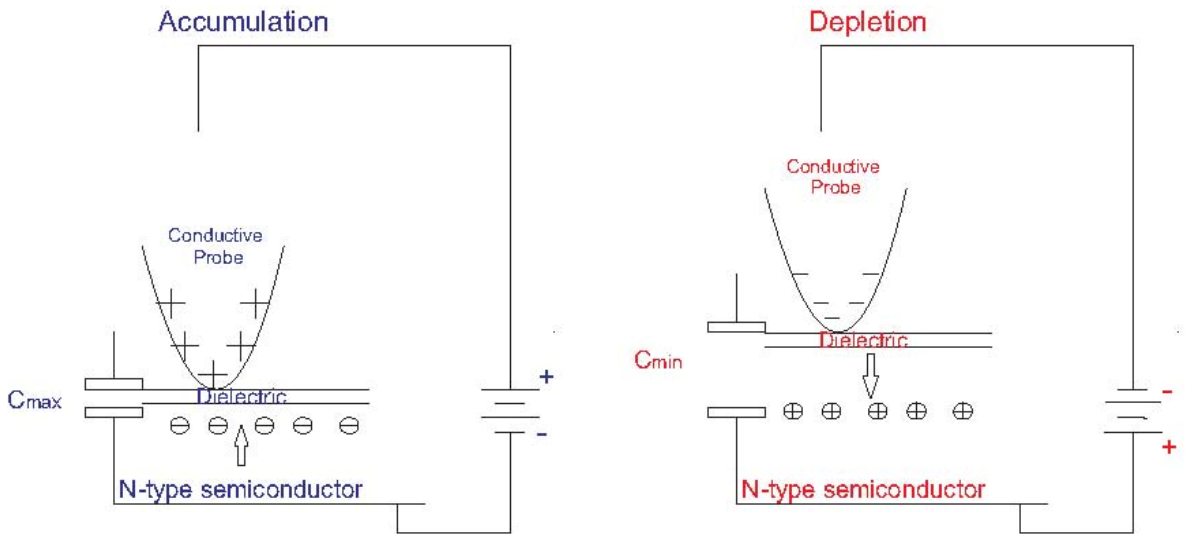
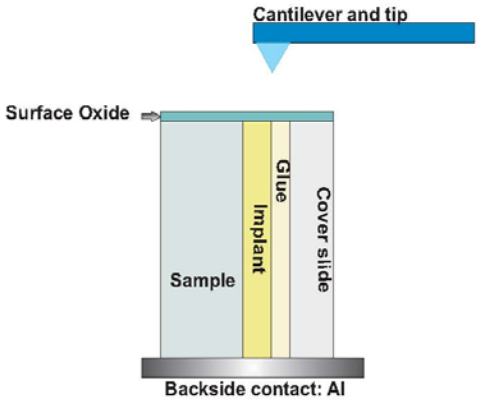


Figure 25 Accumulation and Depletion Regions for an n-Type Semiconductor

3.1.8.1.1 SCM Sample Preparation

As SCM is a surface sensitive technique, sample preparation is important to ensure the quality of SCM measurements. The sample surface can be damaged by polishing, producing surface roughness and surface charges that can affect the capacitance sensor, with the result that tip physical properties are not ideal. Sample preparation is also a critical part in achieving high resolution measurements in SCM. It took several years since the first application of SCM to obtain a cross-sectional 2D SCM image of the P+P implant [16]. Originally, the polishing techniques that were applied in scanning electron microscopy (SEM) were used for SCM samples [17] [18]. The sample preparation technique must satisfy several requirements including having good oxide quality, a surface free of artifacts, and good surface morphology repeatability, as well as being cost effective [19]. Furthermore, the sample polishing finishing procedure using colloidal silica is critical, because it produces a thin insulating layer on the sample, as a reaction between hydroxide and silicon [17] [18] [20]. The final stage in sample preparation is the oxidation of the surface using UV-generated ozone, as capacitance measurements are impossible without an oxide layer above and a metal layer, such as aluminum, below (forming the MOS capacitor).

Three sample preparation techniques are used in SCM: cross-section, plain view, and angle beveling [20]. Only cross-section sample preparation was used in this work. The cross-section of the sample after preparation is illustrated in Figure 26.

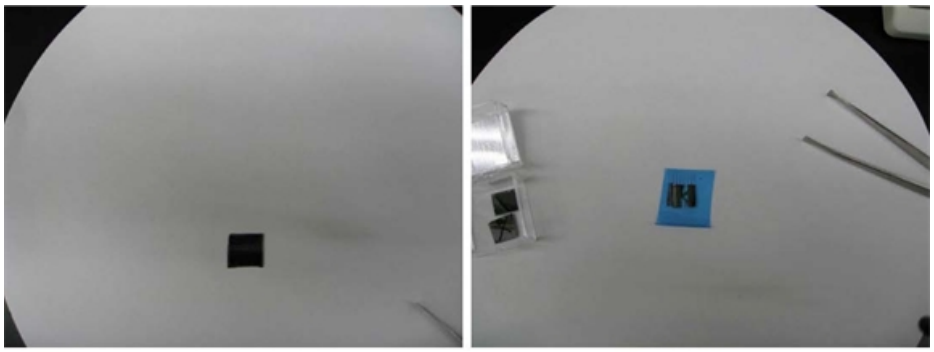


Note: To minimize stray light from AFM laser and stray capacitance, cover slide was contacted on the top surface of the sample and Al was deposited to make good backside contact.

Figure 26 Cross-Section of Sample after Preparation

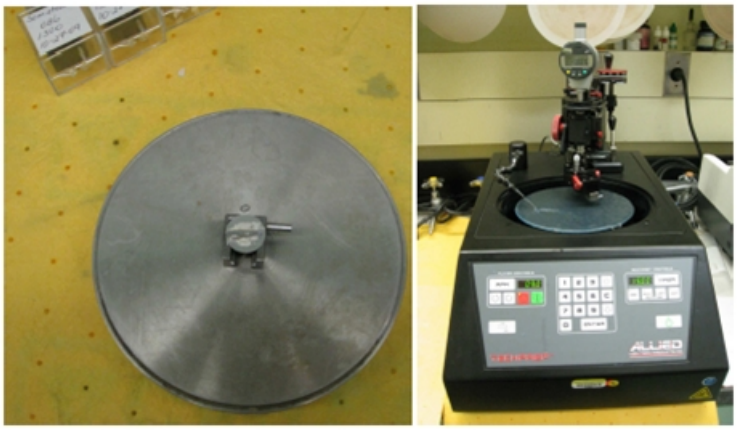
The preparation of SEMATECH samples was as follows:

1. **Cleaving the selected region:** The 300 mm wafers were cleaved into 1 cm × 30 cm strips, producing a 1 cm × 1 cm slice as seen in Figure 27a.
2. **Gluing cover slide on the slice:** A cover slide was glued on top of the sample surface using epoxy bond 110 (Allied High Tech Products, Inc.) and cured at 150°C to reduce stray light from AFM laser and stray capacitance as shown in Figure 26.
3. **Dicing saw:** This slice was diced approximately into a 1 mm × 1 cm strip as shown in Figure 27b.
4. **Backside contact:** Al was deposited using a thermal evaporator on one side of the sample to produce a backside contact. The sample was then mounted on a round puck (a sample holder) using epoxy glue.
5. **Sample polishing-grit paper:** Several grit papers were used: a 9 µm grit was used to remove the dicing saw marks, followed by 3 µm, 1 µm, 0.5 µm, and 0.1 µm grit papers to flatten the surface (see Figure 28a).
6. **Sample polishing-polycrystalline solution**: This step, as shown in Figure 30 on the right, involved polishing the samples with polycrystalline solutions of 1 µm, 0.5 µm, 0.25 µm, 0.1 µm, and 0.05 µm to smooth the surface and residual polishing particles.
7. **Sample polishing-colloidal silica:** The surface was finished by removing final scratches to produce a thin insulating layer, with 0.02 µm of colloidal silica followed by rinsing in microsoap and deionized (DI) water and drying the surface with nitrogen, as shown in Figure 28b.
8. **Oxidation of the surface:** An ultraviolet-generated ozone accelerated the production of native oxide on the sample surface. A capacitance measurement is possible after this step. The final product is seen in Figure 29a, with all stages shown in Figure 29b.



a) Wafer Processing b) Dicing Saw

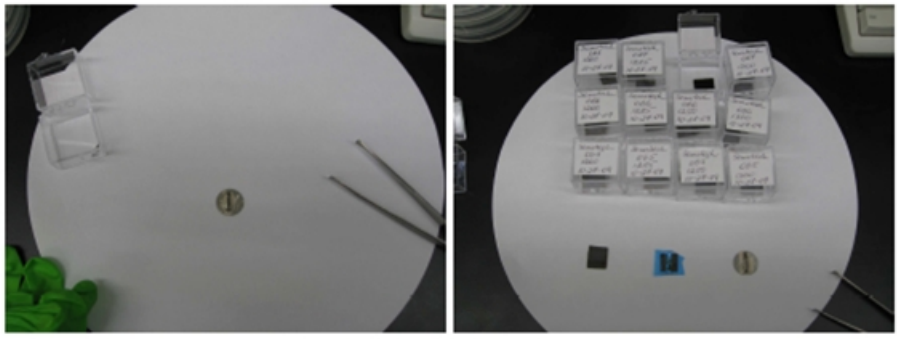
Figure 27 Sample Preparation: a) Wafer Processing and b) Dicing Saw



a) b)

a) Sample is mounted on the polish holder. b) Polishing sample with grit paper; for steps 6 and 7, a pad was mounted on the polish surface and either polycrystalline or colloidal silica was poured instead of water as shown.

Figure 28 a) Sample Polishing-Grit Paper and b) Sample Polishing-Polycrystalline Solution and Polishing-Colloidal Silica



a) b)

a) Final stage of the sample preparation. b) All stages of sample preparation.

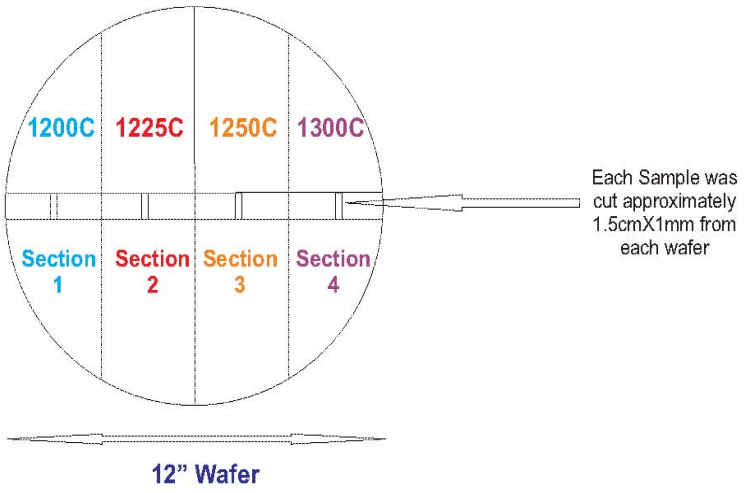
Figure 29 Oxidation of Surface

3.1.8.1.2 SCM Measurement

The data extracted from SCM measurements consist of five SEMATECH ultrashallow junction (USJ) wafers. Wafers OG5, OB6, and OA7 were laser-annealed at four different temperatures. Wafers OA6 and OF2 did not undergo laser annealing, but were analyzed at four different sections of the wafer. Samples from wafer OG5 were compared with samples from wafer OA6, as both have the same n-type implant (phosphorous) with a p-type Si substrate (N+ in P). Samples from wafer OB6 and OA7 had a BF_2 implant on a p-type Si substrate (P+ in P). Hence, a p-n junction was observed in samples from wafers OG5 and OA6. Table 3 summarizes the wafers and Figure 30 shows the sample locations.

Table 3 Wafers Selected for SCM Measurements and Analysis (OA7, OB6, OG5, OA6, and OF2 [highlighted in blue])

Slot	Wafer ID	Implant Species	Dopant Dose (at/cm^2)	Ge PAI (keV)	LAT (C)
1	46K3IGQ1KOA6	BF_2	5.00E+14	20	1030
2	46K3IGPZK**OA7**	BF_2	5.00E+14	50	1030
3	46K3IGPYKOE0	BF_2	5.00E+14	50	1030
4	46K3IGPXKOH1	BF_2	5.00E+14	80	1030
5	46K3IGPVKOG0	BF_2	2.00E+15	20	1100
6	46K3IGPUK**OB6**	BF_2	2.00E+15	50	1100
7	46K3IGPSKOA5	BF_2	2.00E+15	20	1030
8	46K3IGPQKOG7	BF_2	2.00E+15	80	1100
9	46K3IGPKKOD4	P	2.00E+14	20	1030
10	46K3IGPJK**OG5**	P	2.00E+14	50	1030
11	46K3IGPHKOF4	P	2.00E+14	50	1030
14	46K3IGPBKOC1	P	1.00E+15	50	1100
15	46K3IGPAK**OF2**	P	1.00E+15	50	1100
16	46K3IGPBK**OA6**	P	1.00E+15	80	1100

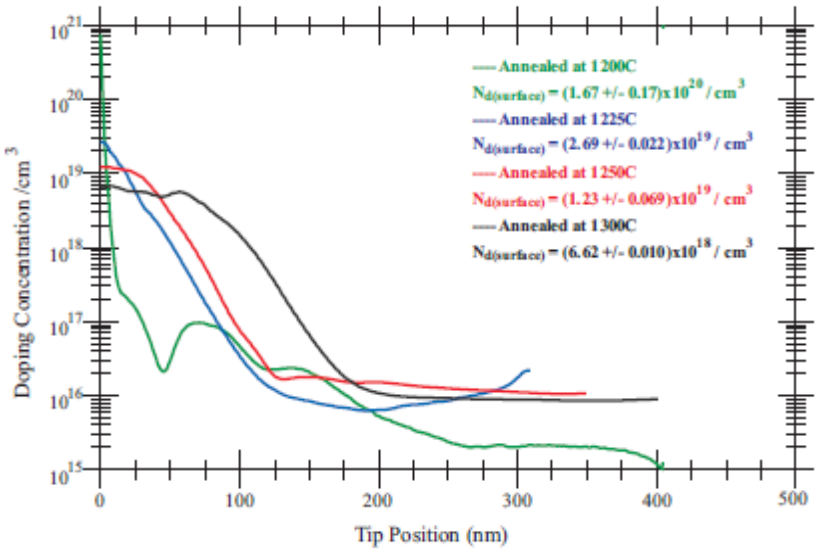


Note: Samples were prepared from 5 wafers. Wafers OA7, OB6, and OG5 were annealed at different temperatures at different sections of each wafer. Samples prepared from wafers OA6 and OF2 were not annealed, hence produced the same results from all four sections.

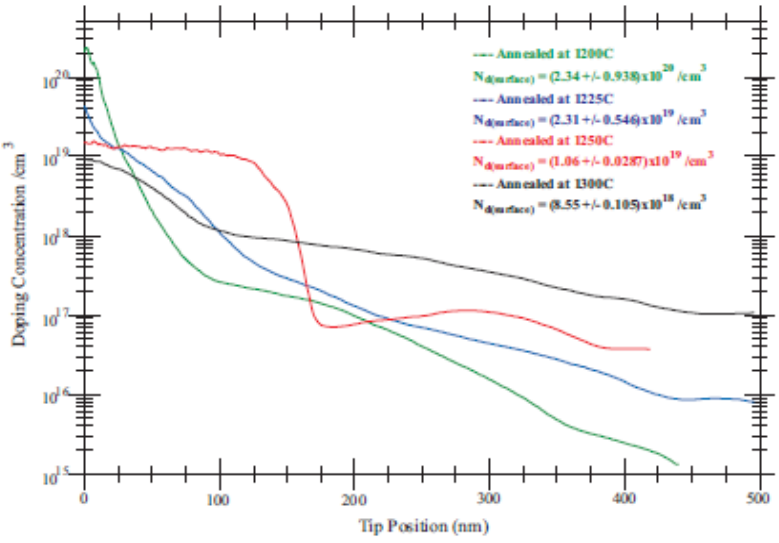
Figure 30 Wafers OA7, OB6, and OG5 Sample Locations

3.1.8.1.2.1 Data and Analysis of SEMATECH Wafer OB6

Wafer OB6 was analyzed using two different commercially available tips: an RMN tip—a solid Pt wire tip (from Rocky Mountain Nanotechnology LLC) and a CSC17/Ti-Pt tip—a conventional metal-coated Si cantilever tip (from MikroMasch). Figure 31a shows data obtained with the CSC17/Ti-Pt tip; Figure 31b shows data taken with the RMN tip. Both data sets were measured at a 512 nm scan size.



a)

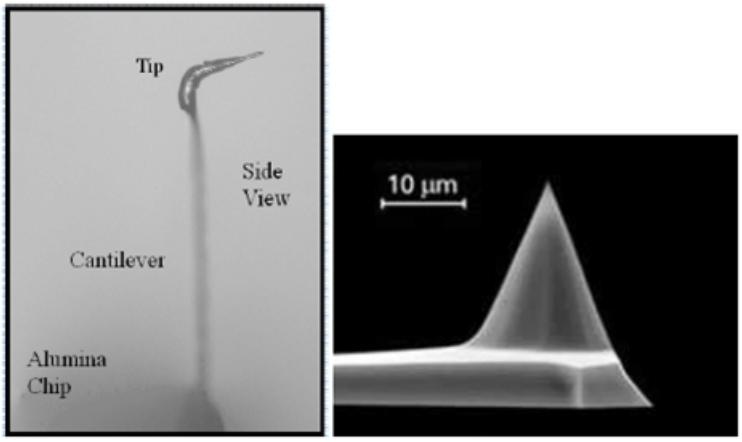


b)

Note: SEMATECH wafer OB6 (P+ in P), scan size 512 nm with a) CSC and b) RMN tip. Laser anneal at four different temperatures. Spike anneal at 1100°C, Ge PAI at 50 keV, dopant dose 2.00E+15 (at/cm^2), implant species BF_2.

Figure 31 Wafer OB6 Data Analysis with a) CSC17/Ti-Pt Tip and b) RMN Tip

This wafer was laser-annealed at temperatures of 1200°C, 1225°C, 1250°C, and 1300°C at four sections of the wafer (see Figure 30). SCM analysis showed that the section of the wafer that was annealed at 1200°C had a higher surface doping concentration than the section annealed at 1300°C [20] [21]. This observation suggests that dopants diffused less at lower laser annealing temperatures. Another set of data was obtained on the same samples with RMN tip for comparison, as shown in Figure 31b. Results were similar, but using two different tips did produce a slight difference in data, ranging from 13 to 28%. The spatial resolution and accuracy of both tips depend on the shape of the terminus of the tip and the stray capacitance between the sample and the cantilever. Tip diameter and aspect ratio (length/width) are used to describe the shape when analyzing the SCM data with the FAST2CD program. As seen in Figure 32, the parameters of these two probe tips varied.



Note: a) Optical view of RMN tip (courtesy of RMN LLC): Rtip ~ 10 nm, spring constant 1 Nt/m, cantilever length ~ 300 µm, width ~ 60 µm, resonant frequency ~ 9 KHz, solid probe has no adhesion problems. b) SEM view of CSC17/Ti-Pt tip (courtesy of MikroMasch): Rtip < 35 nm, spring constant 0.15 Nt/m, cantilever length ~ 460 µm, width ~ 50 µm resonant frequency 12 KHz.

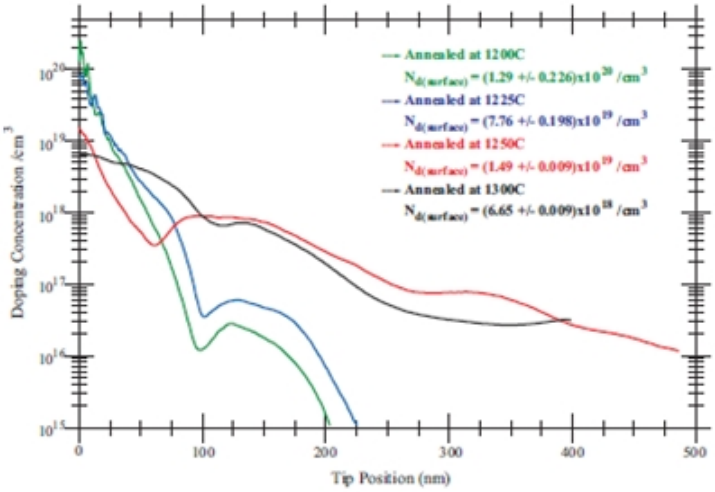
Figure 32 Wafer OB6 Tip Diameter and Aspect Ratio Variations

Interpreting SCM images as quantitative dopant profiles encounters two difficulties. The first is the location of the true surface (tip position = 0 point). The SCM signal should be zero in the glue layer above the sample and very low for high dopant levels. However, an offset in the SCM signal often makes it difficult to determine the point where the SCM tip begins interacting with the silicon. In practice, the z = 0 point is estimated from hints in the surface topography as well as the behavior of the SCM signal introducing some uncertainty in the profile depth scale. The second difficulty is determining the calibration point of the SCM. The dopant concentration must be known at one level of the SCM signal to align the calculated calibration curve with the measured SCM signal. Exact calibration points for these series of samples were not available. To compare the extracted dopant profiles, NIST estimated an expected peak dopant concentration from the dose, energy, and annealing conditions.

To improve the quality of the dopant profiles extracted from SCM images, a more careful calibration procedure of a known dopant level is required. This can be done using a well-known standard prepared simultaneously with the unknown, an independent SIMS measurement of one or more dopant profiles, or a precision computer simulation of expected dopant profiles to determine the known dopant level.

3.1.8.1.2.2 Data and Analysis of SEMATECH Wafer OA7

SEMATECH wafer OA7 was similar to wafer OB6. Both had the same implant species, BF_2 (P+ in P) and underwent four different laser annealing temperatures, but dopant doses and spike annealing temperatures were different. Wafer OA7 was analyzed with CSC17/Ti-Pt, a conventional metal-coated Si cantilever tip, with a 512 nm scan size (Figure 33). Similar to wafer OB6, SCM analysis showed that the section of the wafer annealed at 1200ºC had a higher surface doping concentration than the section annealed at 1300ºC. This observation also suggests dopants diffused less at lower laser annealing temperatures.

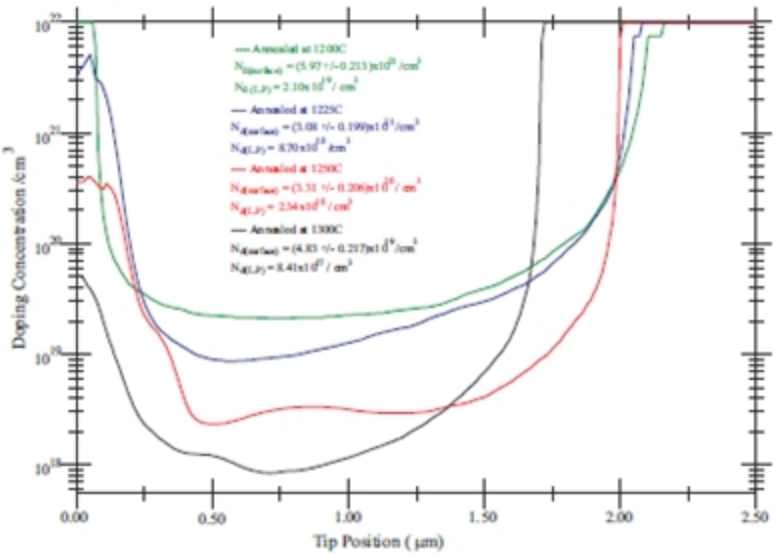


Note: SEMATECH wafer OA7 (P+ in P), scan size 512 nm. Laser anneal at four different temperatures. Spike anneal at 1030°C, Ge PAI at 50 keV, dopant dose 5.00E+14 (at/cm^2), implant species BF_2.

Figure 33 Wafer OA7 Data Analysis with CSC17/Ti-Pt Tip

3.1.8.1.2.3 Data and Analysis of SEMATECH Wafer OG5

SEMATECH wafer OG5 was analyzed with a CSC17/Ti-Pt tip (see Figure 34). As with the previous wafer, OG5 was laser-annealed at 1200ºC, 1225ºC, 1250ºC, and 1300ºC at four sections of the wafer (see Figure 30). SCM showed that the section of the wafer annealed at 1200ºC also had a higher surface doping concentration than the section annealed at 1300ºC, which suggests a conclusion similar to that of wafers OB6 and OA7. Since wafer OG5 had an n-type implant, phosphorous, on a p-type Si substrate (N+ in P), a p-n junction was observed. The width of the junction was controlled by the applied DC bias. To observe the junction, a micron-scale scan size was selected at 2.5 µm. An exact junction depth doping concentration was not measured, but was estimated by the lowest point doping concentration ($N_{d(L:P)}$). To measure an exact junction depth doping concentration, more analysis is needed, e.g., applying different DC biases on each sample, as well as various AC biases on the tips [20].



Note: SEMATECH wafer OG5 (N+ in P), scan size 2.5 µm. Laser anneal at four different temperatures. Spike anneal at 1030°C, Ge PAI at 50 keV, dopant dose 2.00E+14 (at/cm^2), implant species phosphorus.

Figure 34 Wafer OG5 Data Analysis with CSC17/Ti-Pt Tip

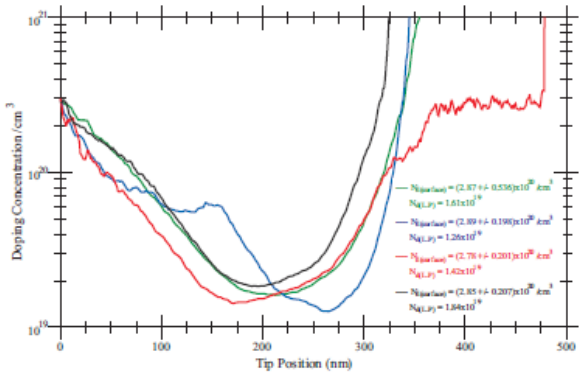
3.1.8.1.2.4 Data and Analysis of SEMATECH Wafers OA6 and OF2

SEMATECH wafers OA6 and OF2 were also analyzed with the CSC17/Ti-Pt tip (see Figure 35a and Figure 35b). Unlike the previous wafers, OA6 and OF2 were not laser-annealed, but four sections of each wafer were analyzed. As is shown in both Figure 35a and Figure 35b, each wafer had the same surface doping concentration, obtained from all four sections. This implies that the doping concentration throughout the wafer should be homogeneous. Furthermore, as in wafer OG5, an exact junction depth doping concentration was not measured, but was estimated by the lowest point doping concentration ($N_{d(L.P)}$). To measure an exact concentration, more analysis is needed, e.g., applying different DC biases on each sample and improved modeling of the accumulation, recombination, and depletion regions with flatband voltage [2].

3.1.8.1.2.5 Comparison of SEMATECH Wafers OG5 and OA6

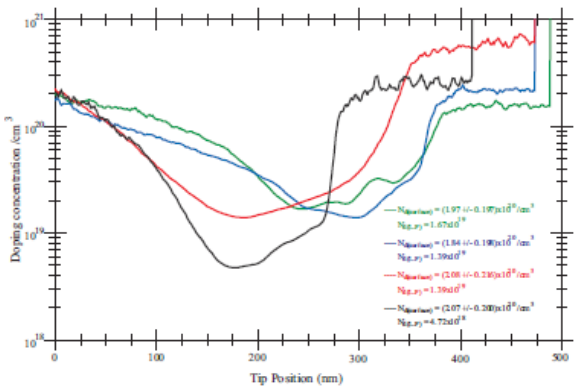
Due to the laser annealing process, wafer OG5 required a higher scan size than wafer OA6, which was not laser-annealed (Figure 36a and Figure 36b). Additionally, no DC bias had to be applied to observe the junction with wafer OA6. According to previous studies, diffusion of dopants during MeV Si implantation procedures may produce a vacancy at the near surface and interstitial regions at the projected ion range [20]. Furthermore, the MeV Si implant was shown to have smaller diffusion by a factor of 10 than a MeV Si+ implant [20]. The capping layer may have an effect on junction motion and loss of dopant atoms (out-diffusion) [21].

SCM images of samples with p-n junctions are not as easily interpreted as unipolar samples. The SCM signal changes signs between p-type and n-type material and hence has a singularity at a p-n junction. Additionally, the built-in depletion layer at the junction can extend into the more lightly doped side, where SCM data does not directly relate to dopant concentration. Dopant profiles extracted from samples containing p-n junctions, like those in Figure 34–Figure 36, display artifacts that are not related to the true dopant concentration. In these figures, near the



SEMATECH wafer OA6 (N+ in P), scan size 512 nm. No laser anneal. Spike anneal at 1100°C, Ge PAI at 80 keV, dopant dose 1.00E+15 (at/cm^2), implant species, phosphorus.

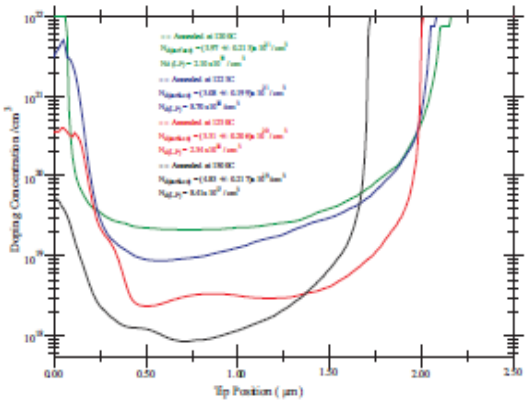
a) Wafer OA6



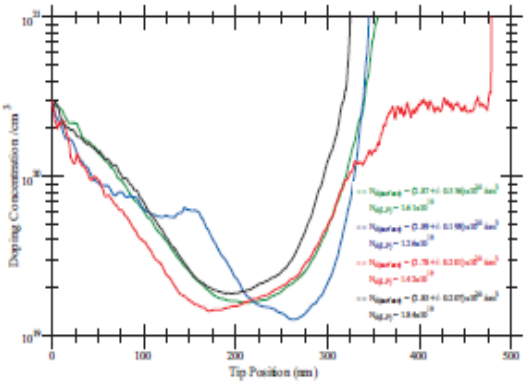
SEMATECH wafer OF2 (N+ in P), scan size 512 nm. No laser anneal. Spike anneal at 1100°C, Ge PAI at 50 keV, dopant dose 1.00E+15 (at/cm^2), implant species, phosphorus.

b) Wafer OF2

Figure 35 a) Wafer OA6 and b) Wafer OF2 Data Analysis with CSC17/Ti-Pt Tip



a) Laser Anneal



b) No Laser Anneal

Figure 36 Wafer OG5 (N+ in P): a) Laser Anneal and b) No Laser Anneal

surface where the n-type dopant concentration is high, the extracted dopant profile is accurate. At depths beyond where the extracted dopant concentration reaches a minimum, the probe is in a depletion region and the extracted dopant concentration is not valid. As the probe enters the opposite type material deeper in the sample, the signal changes sign and the apparent dopant concentration rapidly increases. This is an artifact and not indicative of the true dopant concentration.

3.1.8.1.2.6 Conclusion

These results demonstrate that the SCM technique can measure dopant distributions of USJ wafers. This was demonstrated by measurements of five SEMATECH wafers. When samples from wafer OB6 were measured with two different scanning probes, a slight difference in doping concentrations was observed. This observation suggests that the SCM technique depends upon the shape of the terminus of the tip and the stray capacitance between the sample and the cantilever. Furthermore, wafer OG5, the laser-annealed wafer, required a higher scan size than

wafer OA6, the non laser-annealed wafer, to observe and measure the pn-junction. Additionally, no DC bias was needed to observe the pn junction with wafer OA6.

These results point to several important observations. First, in SCM a correct bias needs to be applied to achieve a signal that changes in proportion to dopant concentration, and without changing sign, over the complete range of dopant concentrations, that is, a signal that changes monotonically with dopant concentration. Second, implantation procedures and capping layers may affect the diffusion of dopants and junction diffusion and loss of dopant atoms by the out-diffusion process [21]. Finally, SCM spatial resolution depends upon the tip shape, and can be improved with a sharper tip such as a carbon nanotube based tip (CNT). Other techniques such as SSRM or SIMS have better sub-nanometer resolution and easier quantification techniques, but they are destructive; hence repetition is impossible and SSRM and SIMS measure only metallurgical junctions (MJs). SCM measurements, while destructive to the sample, can be preformed repeatedly on the same area of the same sample. SCM also measures the profile of electrically active dopants and the electrical junction, rather than the chemical profile and junction obtained with SIMS. Although SCM has limitations in spatial resolution, it can be improved with sharper tips and better sample preparation techniques.

3.1.8.2 Measurement of Doped FinFET Structures

NIST will also use SCM to measure FinFET structures. The die layout is shown in Figure 37. One set of samples will be cross-sectioned parallel to the fins and a second set will be cross-sectioned perpendicular to the fins. An SEM of the 65 nm fins after boron implant is shown in Figure 38.

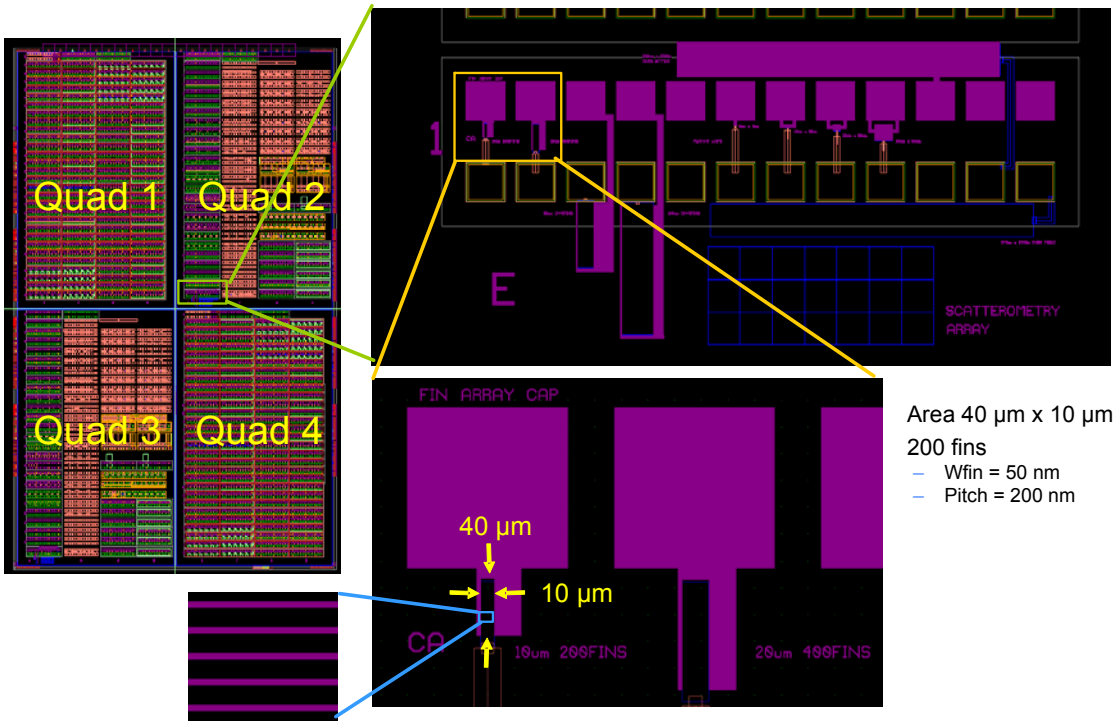


Figure 37 SEMATECH FinFet Die Layout

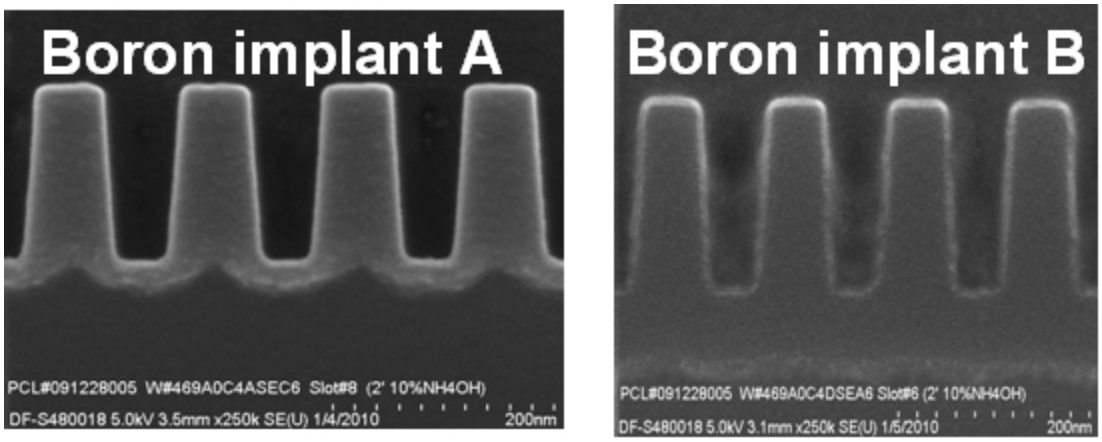


Figure 38 SEMs of 65 nm FinFET Arrays after Two Boron Implants

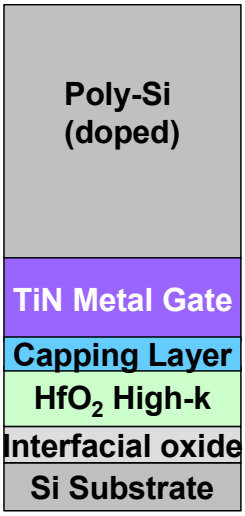
3.1.8.3 Measurement of Work Functions in High-k/Metal Gate Film Stacks

ISMI fabricated high-k metal gate (HKMG) samples of substrates having varied work functions, which are relevant for threshold voltage tuning of N and P-type transistors. The stack is shown in Figure 39. The difference in work function between tips and sample can be used to determine the work function of the sample. NIST will use SKFM to perform the work function measurements. SKFM measures the contact potential difference (CPD) between the tip and sample. Sample preparation will consist of a cross-section first, but as layers are very thin, a very low angle bevel will be used to magnify the layers by a factor of 200. Measurements will occur at NIST in July, 2010, after new students are trained in sample preparation.

The die layout is shown in Figure 40 and Figure 41, showing the capacitor structures. The capacitor structures ranged from 3.5 mm to 10 μm diameter. The wafer splits are shown in Table 4.

Table 4 Splits for Work Function Wafers

Wafer	TiN Thickness (nm)	Capping Layer Thickness (nm)
1	10	0.7
2	20	0.0
3	10	0.7
4	20	0.0



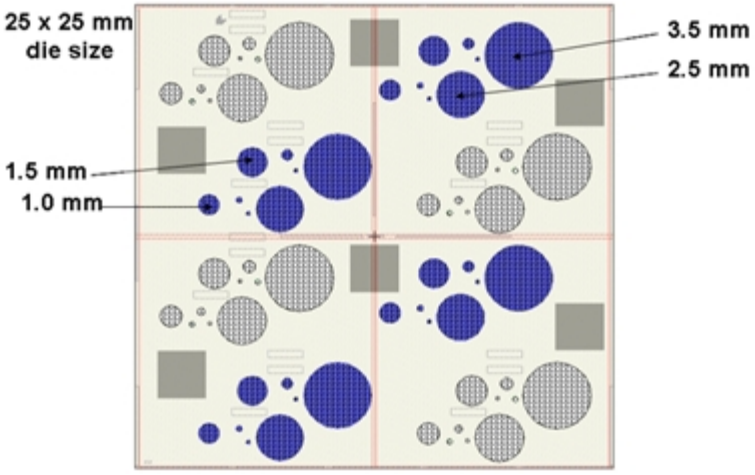


Figure 39 Film Stack for Work Function Wafers

Figure 40 Capacitor Structures for Work Function Wafers

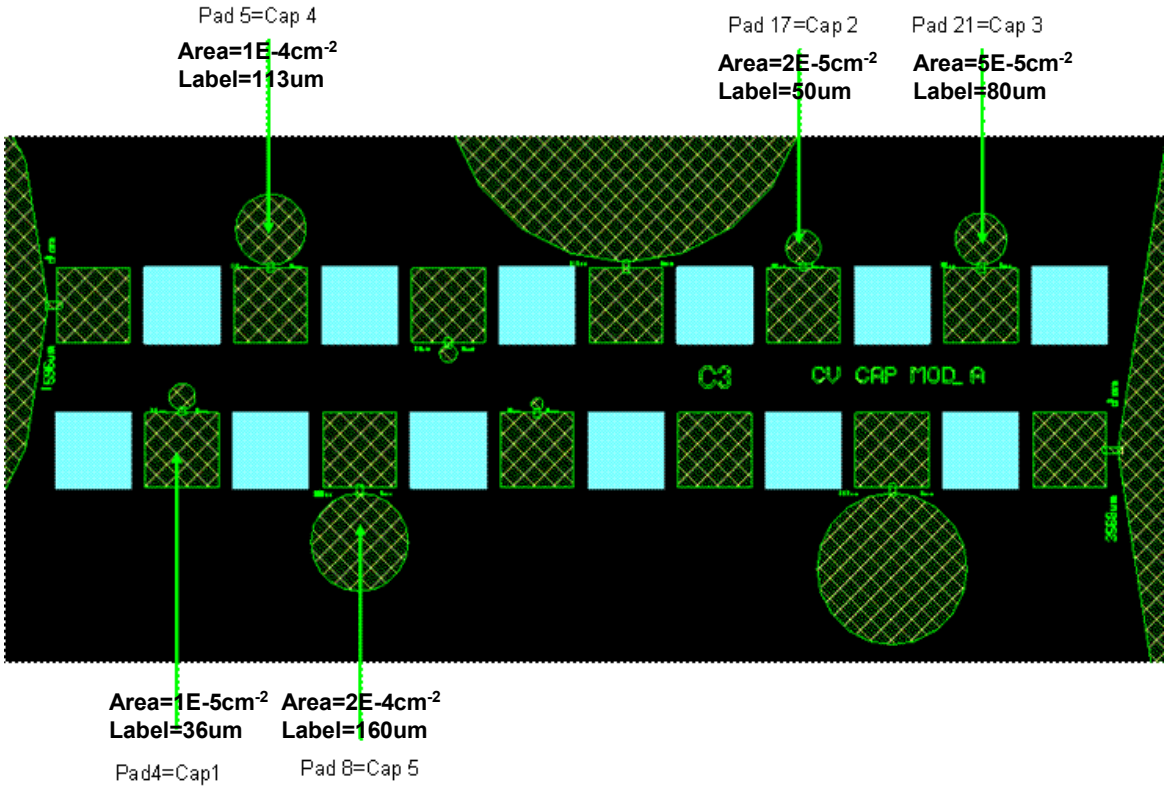


Figure 41 Capacitor Detail from GDS

3.1.8.4 Measurement of Etch Damage to Low-k Dielectrics

ISMI also fabricated low-k dielectric samples of substrates having amounts of plasma damage. The film cross section is shown in Figure 42, and the reticle layout is shown in Figure 43. NIST will use SCM to measure dielectric constant variation in the dielectric regions. Low-k dielectrics can suffer etch damage when vias are opened leading to local increase in dielectric constant. Variations of a few percent over a few nanometers are expected. SCM has the potential to resolve this magnitude of variation, but a sharp, high-aspect ratio tip is required. A modification of the sample preparation technique will be required to measure low-k dielectric constant variation. Both SKFM and intermittent contact SCM (IC-SCM) measurements and modeling can be compared. A specialized module is included in the SEMATECH 800AZ reticle (Figure 43).

The low-k module of special interest has a large area of exposed low-k dielectric adjacent to metal (Figure 44 and Figure 45). The experimental splits are shown in Table 5 and Table 6, with variations in plasma chemistry (O_2 and forming gas, N_2/H_2), power, and time.

Table 5 Ash Process Variation Used for the Ten Wafers

Split	Wafer	Gas	% OE	Power	Process Time
1	5	N_2/H_2	50%	Med	106 sec + 50 sec OE
2	6	O2	30%	Med	19.6 sec + 7.2 sec OE
3	7	N_2/H_2	70%	Med	106 sec + 32 sec OE
4	8	N_2/H_2	30%	Med	108 sec + 76 sec OE
5	9	O_2	50%	Med	21 sec + 10.5 sec OE
6	10	O_2	70%	Med	21 sec + 14.5 sec OE
7	11	O_2	50%	Low	30 + 30 sec OE (missed endpoint)
8	12	O_2	50%	High	18 sec + 9 sec OE
9	13	N_2/H_2	50%	Low	148 sec + 74 sec OE
10	14	N_2/H_2	50%	High	87 sec + 43 sec OE

Table 6 Recipes Used for the Ten Wafers

Step	N_2H_2 Ash	O_2 Ash
Electrode Gap	37 mm	37 mm
Pressure	40 mTorr	40 mTorr
RF power	500 W	400 W
N_2 Flow	500 sccm	
H_2 Flow	125 sccm	
O_2 Flow		400 sccm
He Cool	40/7 Torr	40/7 Torr
Temp (U/W/L)	60/60/10°C	60/60/10°C
Default OE	50%	50%

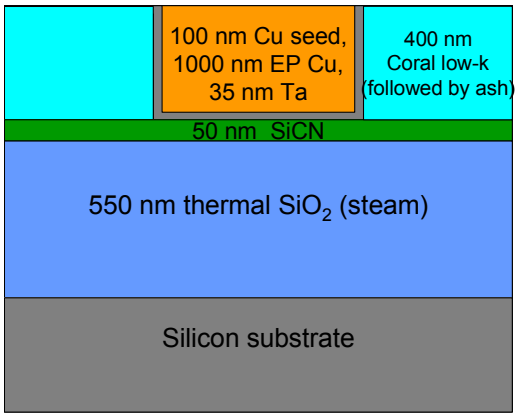


Figure 42 800AZ Cu Interconnect Wafer Showing Coral Low-k Dielectric

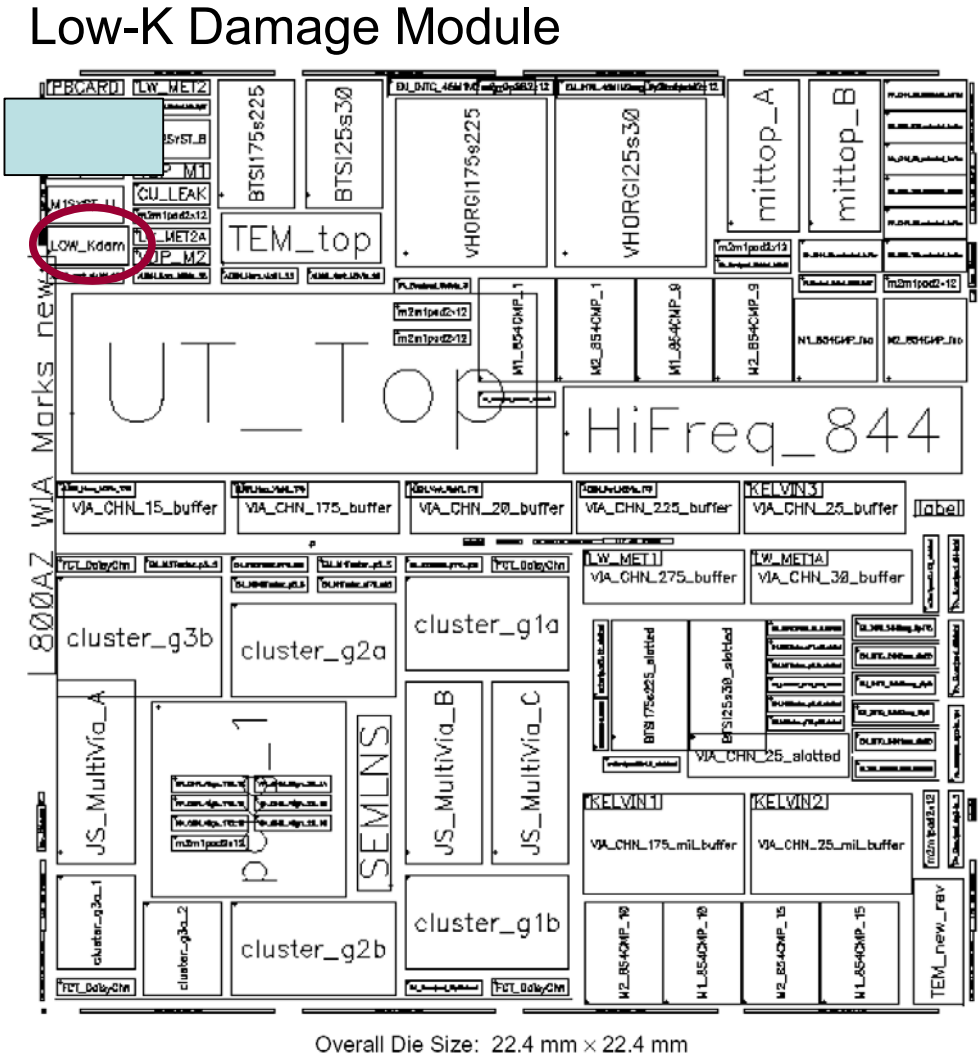


Figure 43 LOW_K_DAM Module in the SEMATECH 800AZ Reticle

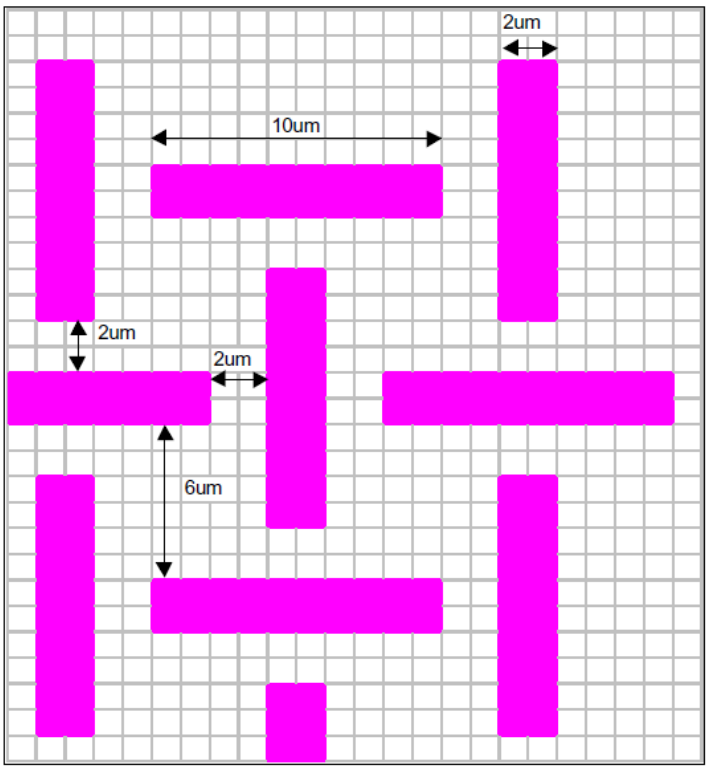


Figure 44 LOW_K_DAM Module Diagram in the SEMATECH 800AZ Reticle

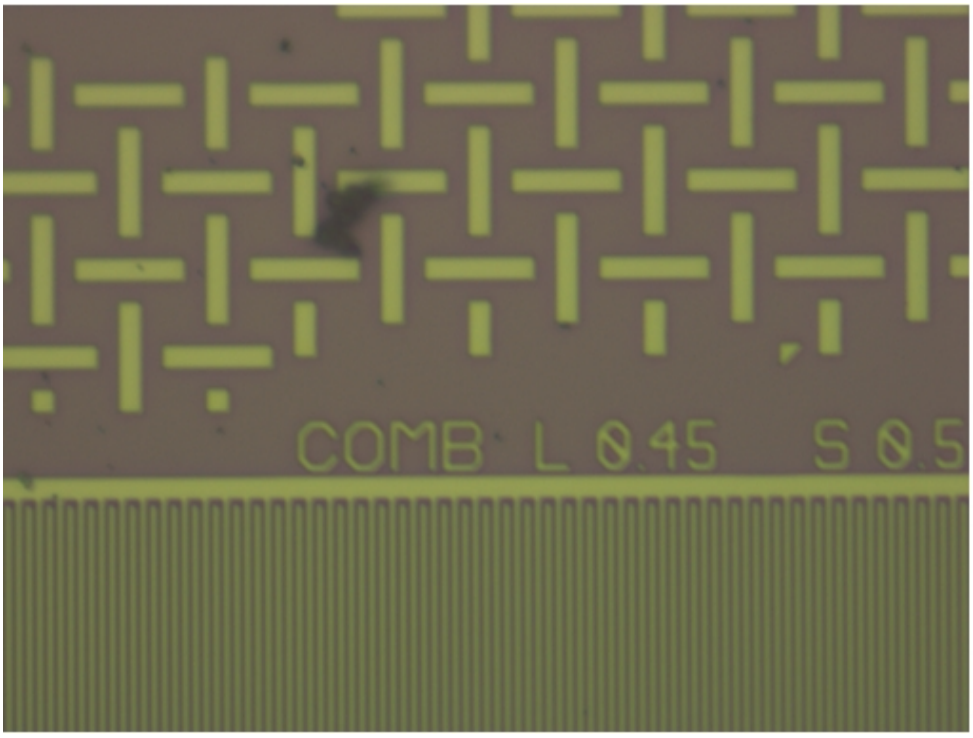


Figure 45 LOW_K_DAM cell in the SEMATECH 800AZ Reticle

RC time constant parametric measurements were made on serpentine comb structures. The variation in RC time constants falls into two sets of data, separated by about 10%, with the O_2 splits showing a 10% lower RC time constant (and corresponding dielectric constant compared to the N_2/H_2 splits [see Figure 46]).

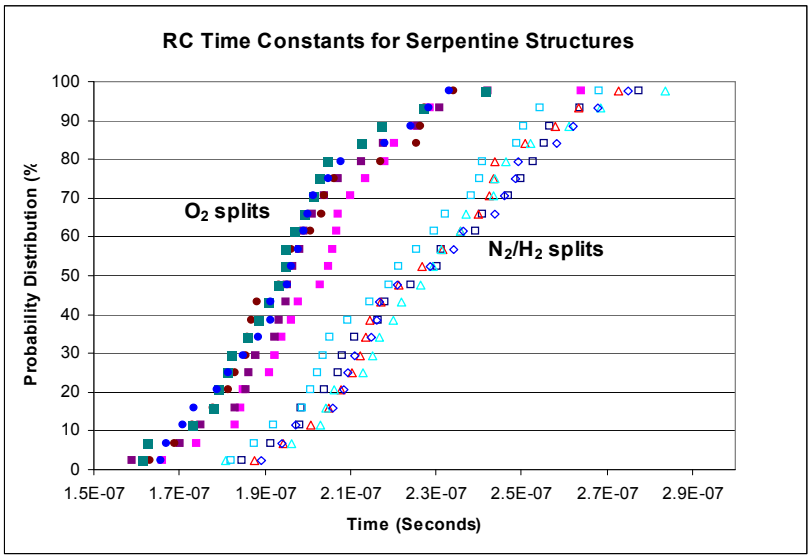


Figure 46 RC Time Constants for Serpentine Structures

Low resolution SCM images of the low-k test structures (Figure 47 and Figure 48) show that the silicon beneath the metal bars is inverted by the metal, while the silicon beneath the low-k has accumulated. The low-k between the metal bars produced an unexpectedly large SCM signal. This may be due to trapped charge in the dielectric or at the interface. This preliminary result demonstrates the ability of SCM to detect the charge dynamics of the silicon, low-k, and metal structures. Either intermittent contact SCM or SKFM should display additional sensitivity to variations in dielectric constant and charge within the low-k and near the dielectric-silicon interface. Detailed high spatial resolution measurements are planned.

3.1.9 Determination of Probe Tip Parameters and Their Effect on SKFM and IC-SCM Measurements

Aggregate tip-plus-probe-plus-cantilever resistance affects the measurement sensitivity in both SKFM and IC-SCM. Tip-to-metal resistance and I-V characteristics can be quantified as a function of contact force using the TUNA module of the Veeco nanoscope. NIST plans to compare tip-to-metal resistance and I-V characteristics of commercially available tips to determine a performance baseline. Tip-to-metal resistance and I-V characteristics will also be measured inside an SEM, as performed in earlier work sponsored by SEMATECH [23], and compared with AFM measurements. Simple models of SKFM and IC-SCM will be extended to include the effect of tip resistance to determine performance limits for CNT tips.

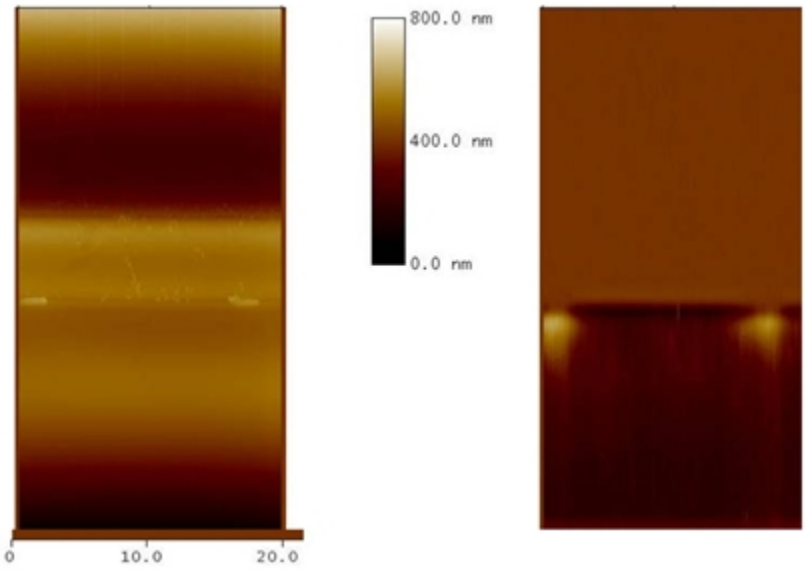


Figure 47 Low resolution AFM and SCM image of cross-sectioned low-k sample showing two of the metal cross-hatch bars shown in Figure 43

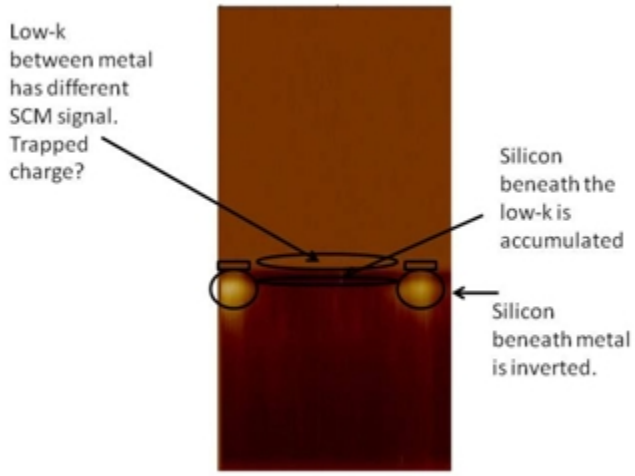


Figure 48 Details of SCM image of low-k cross-section shown in Figure 46

3.1.10 Improvement in Probe Tip Performance by Engineering Refinements

Lessons learned during this project will be used to refine the existing conductive CNT tip fabrication processes targeted towards a future scaleable manufacturing process for electrically conductive CNT tips.

1. Xidex and NIST have shown that the SPM probe must be coated with metal to improve the conductivity of the entire probe. The metal coating improves the electrical conductivity between the CNT and the SPM tip and provides a conductive path from the SPM tip to the probe holder of the SPM instrument. An uncoated doped-Si substrate is not adequate for electrical probing. This is consistent with current commercial electrical

probes, which are also metal-coated. The deposition of metal on the Si by thermal evaporation or sputtering is scaleable.

2. Xidex has demonstrated that a CNT tip can be grown directly from a Ag-coated probe. This represents a major advance in CNT tip manufacturing by direct growth. This project revealed that Ag may not be the best metal for coating the probe since the Ag-to-CNT contact is non-Ohmic. This is also true for Au. Xidex also evaluated Al as a coating layer, but the morphology of the Al layer changes and becomes cracked and less conductive when it is subjected to CVD growth of CNTs. Therefore, another metal is suggested for future work, such as Pd or Pt, both of which have an Ohmic connection to the CNT and can support CNT growth.
3. UTK and CNSE have demonstrated that electron beam-assisted welding of the CNT to the SPM tip improves the electrical contact between the CNT and the SPM tip, as shown in [10], as opposed to a CNT that was just grown on the SPM tip. However, the magnitude of conductivity improvement may not be worth the cost required to do this operation in a scaleable, cost-effective manufacturing process. Therefore, the recommendation is to not use electron beam-assisted welding for a manufacturing process, but use it instead when special CNT tips are required and cost is not a barrier.
4. UTK and CNSE have demonstrated the fabrication of a CNT tip coated with dielectric and exposed at its apex. The intent is to reduce the parasitic capacitances of the CNT-based probe. This approach requires further testing and investigation. Xidex, in collaboration with UTK, is executing a funded National Science Foundation project [9] that will further study this approach.
5. Xidex demonstrated alternative methods of improving the CNT contact to the SPM tip, such as coating the entire CNT and SPM probe with a metal layer that can be deposited in a scaleable way by thermal evaporation or sputtering. The CNT can be uniformly coated with a metal layer. This approach requires further investigation in a future project.

3.1.11 Integration of Improved Xidex Tips to Veeco AFM

NIST plans to integrate CNT tips in an in-house Veeco AFM for in-line electrical metrology in 2010.

3.1.12 Future NIST Work

NIST expects to complete the following in Q3 2010:

- Low-k damage wafer measurements: Several polished cross-sections are available. The SKFM at high resolution and intermittent contact SCM will be used.
- FinFET measurements: The first set of cross-sections have been completed; a second set of samples is being polished. Images should be available in July.
- Workfunction measurements: Samples are ready for polishing; they will be measured in August.

The external Kelvin probe has been tuned; NIST is working on demonstrating enhanced spatial resolution and measurement of CNT tip workfunctions.

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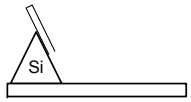
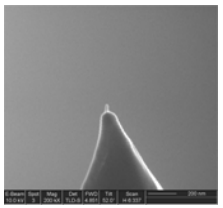
Appendix A – CNT Tip Tracking

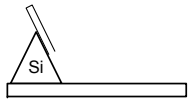
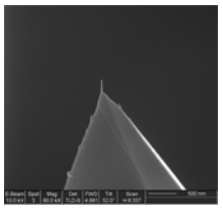
CNT Tip Tracking Status: 06-15-2010

Icons and images provide a visual reference for each tip. The icons are defined in a legend below the table.
The images are high resolution, so they can be expanded to show more detail if needed.

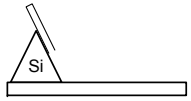
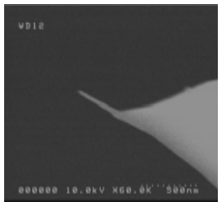
1

TIP NUMBER	DESCRIPTION	IMAGES	
39702-00-01	Conductive CNT tip. Manually mounted on Si Tip Length: 56 nm Diameter: 21 nm		
14-Nov-08	1 of 2 Sent to NIST		

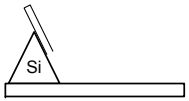
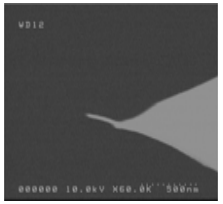
2

TIP NUMBER	DESCRIPTION	IMAGES	
39709-00-01	Conductive CNT tip. Manually mounted on Si Tip Length: 261 nm Diameter: 21 nm		
14-Nov-08	1 of 2 Sent to NIST		
In measurements performed by NIST, these CNT-terminated tips were shown to resolve an abrupt boundary between Au and silicon to within less than a micrometer, while a conventional Au-coated tip smeared the transition between the two materials over tens of micrometers. These results were summarized in a presentation to the SEMATECH AMAG-FMAG Presentation on February 19, 2009 and were also described in a paper presented at the 2009 Frontiers of Characterization and Metrology for Nanoelectronics, in Albany NY.			

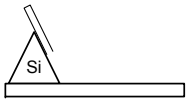
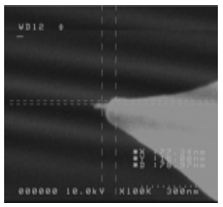
3

TIP NUMBER	DESCRIPTION	IMAGES	
39696-0-01	Conductive CNT tip. Manually mounted on Si Tip		
1-Jul-09	1 of 3 Sent to NIST		

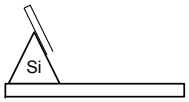
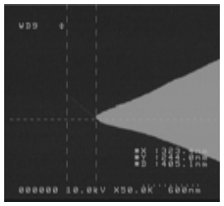
4

TIP NUMBER	DESCRIPTION	IMAGES	
39696-0-02	Conductive CNT tip. Manually mounted on Si Tip		
1-Jul-09	2 of 3 Sent to NIST		

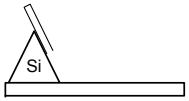
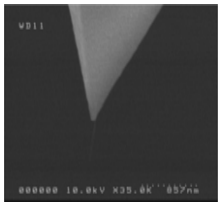
5

TIP NUMBER	DESCRIPTION	IMAGES	
39702-0-01	Conductive CNT tip. Manually mounted on Si Tip		
1-Jul-09	3 of 3 Sent to NIST		
Two of these will be characterized by generating current voltage curves using NIST's TUNA module, and will then be provided to The University of Tennessee for welding. One of the tips will be used at NIST for electrical characterization of samples.			

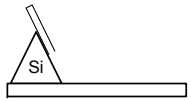
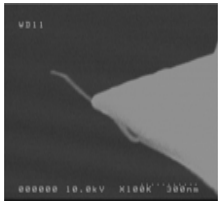
6

TIP NUMBER	DESCRIPTION	IMAGES	
081104-1-1	Conductive CNT tip - grown on Si tip. CNT tip coated with 30 nm of SiO, remove some SiO and leave cnt		
5-Oct-09	1 of 2 Sent to UTK		

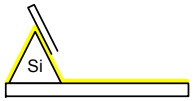
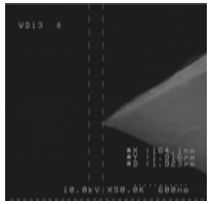
7

TIP NUMBER	DESCRIPTION	IMAGES	
081104-1-2	Conductive CNT tip - grown on Si tip. CNT tip, to be coated with SiO_2 and uncapped		
5-Oct-09	2 of 2 Sent to UTK		
Two conductive CNT tips were provided to Dr. Philip Rack at The University of Tennessee on October 5, 2009.			

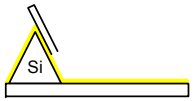
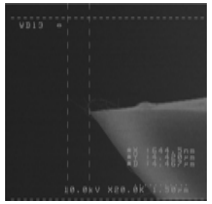
8

TIP NUMBER	DESCRIPTION	IMAGES	
080919-0-1	Conductive CNT tip. Grown on Si tip		
28-Sep-09	1 of 1 Hand delivered to UTK		
Vladimir Mancevski, visited Dr. Rack during September 28-October 1, 2009 and personally delivered one additional conductive CNT tip. Results to date of work performed with the tips provided by Xidex are included the accompanying report by Matthew Bresin, entitled “UTK-CNSE-Xidex Project Update: Lit Review and SiO Etching,” October 11, 2009.			

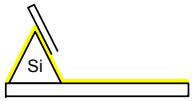
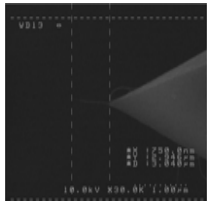
9

TIP NUMBER	DESCRIPTION	IMAGES	
100129-1-1	Conductive CNT tip. Gown on Si tip. Tip is 164 nm long. Can be used as is for scanning.		
1-Feb-10	1 of 3 Sent to UTK		

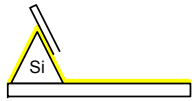
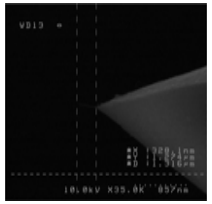
10

TIP NUMBER	DESCRIPTION	IMAGES	
100129-1-3	Conductive CNT tip. Grown on Si tip. Tip is 750 nm long. This CNT is not very conductive, so it is a great candidate to coat the entire CNT tip and Si base with metal. Maybe deposit metal with e-beam. Length of the CNT tip is long, need to scan with less surface interaction.		
1-Feb-10	2 of 3 Sent to UTK		

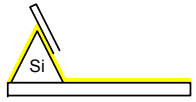
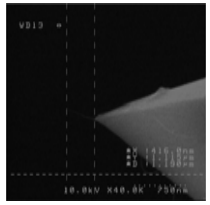
11

TIP NUMBER	DESCRIPTION	IMAGES	
100129-1-4	Conductive CNT tip. Grown on Si tip. Tip is 750 nm long. This CNT is not very conductive, so it is a great candidate to coat the entire CNT tip and Si base with metal. Maybe deposit metal with e-beam. Length of the CNT tip is long, need to scan with less surface interaction.		
1-Feb-10	3 of 3 Sent to UTK		

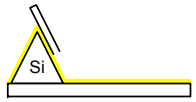
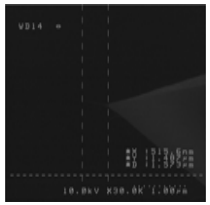
12

TIP NUMBER	DESCRIPTION	IMAGES	
100108-1-1	Conductive CNT tip. Grown on Si tip. Tip is 328 nm long. Can be used as is for scanning.		
15-Feb-10	1 of 4 Sent to NIST		

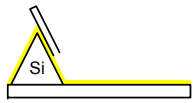
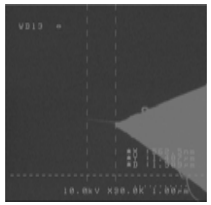
13

TIP NUMBER	DESCRIPTION	IMAGES	
100108-1-6	Conductive CNT tip. Grown on Si tip. Tip is 416 nm long. Can be used as is for scanning.		
15-Feb-10	2 of 4 Sent to NIST		

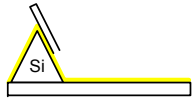
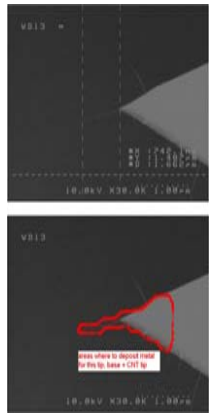
14

TIP NUMBER	DESCRIPTION	IMAGES	
100212-1-1	Conductive CNT tip. Grown on Si tip. Tip is 516 nm long. Can be used as is for scanning.		
15-Feb-10	3 of 4 Sent to NIST		

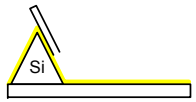
15

TIP NUMBER	DESCRIPTION	IMAGES	
100212-1-3	Conductive CNT tip. Grown on Si tip. Tip is 563 nm long. Can be used as is for scanning.		
15-Feb-10	4 of 4 Sent to NIST		
Note: Joe, please use these tips for electrical measurements.			

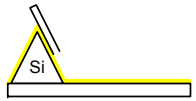
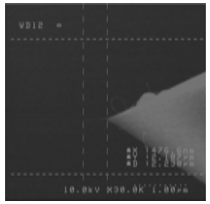
16

TIP NUMBER	DESCRIPTION	IMAGES	
100108-1-3	Conductive CNT tip. Grown on Si tip. Tip is 742 nm long. Too long to scan as is but e-beam deposition should help its reinforcement. Since it has few other CNTs at the base of the CNT tip, I recommend we e-beam deposit metal to the CNT tip and base.		
15-Feb-10	1 of 3 Sent to SUNY Albany		

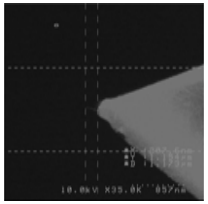
17

TIP NUMBER	DESCRIPTION	IMAGES	
100212-1-4	Conductive CNT tip. Grown on Si tip. Tip is 484 nm long. Can be used as is for scanning. Can be used to e-beam deposit metal to the CNT tip base.		
15-Feb-10	2 of 3 Sent to SUNY Albany		

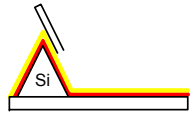
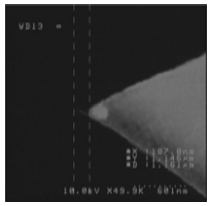
18

TIP NUMBER	DESCRIPTION	IMAGES	
100212-1-5	Conductive CNT tip. Grown on Si tip. Tip is 477 nm long. Can be used as is for scanning. Can be used to e-beam deposit metal to the CNT tip base.		
15-Feb-10	3 of 3 Sent to SUNY Albany		
Note: We typically have e-beam deposited at the area where the CNT is in contact to to base. Do not have the CNT in the field of view when depositing the metal to the base.			

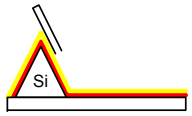
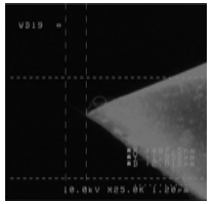
19

TIP NUMBER	DESCRIPTION	IMAGES	
100216-1-2	Conductive CNT tip. Grown on Si tip. The AFM tip was coated with Ag prior to the CNT growth. Tip is imaged from the side. Tip is 208 nm long		
12-Mar-10	1 of 2 Sent to NIST		
For electrical characterization. Can be used as is for scanning.			

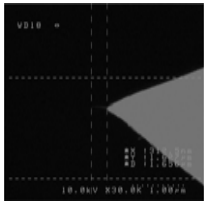
20

TIP NUMBER	DESCRIPTION	IMAGES	
100213-1-3	Conductive CNT tip. Grown on Si tip. The AFM tip was coated with Ag prior to the CNT growth. Tip is imaged from the side. Tip is 187 nm long		
12-Mar-10	2 of 2 Sent to NIST		
For electrical characterization. Can be used as is for scanning.			

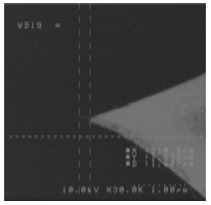
21

TIP NUMBER	DESCRIPTION	IMAGES	
100318-2-1	Conductive CNT tip. Grown on Si tip. The AFM tip was coated with Ag prior to the CNT growth. Tip is imaged from the side. Tip is 313 nm long		
23-Mar-10	1 of 3 Sent to UTK		
Can be used as is for scanning.			

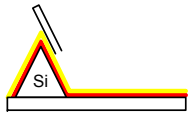
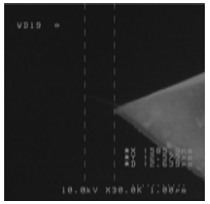
22

TIP NUMBER	DESCRIPTION	IMAGES	
100318-2-4	Conductive CNT tip. Grown on Si tip. The AFM tip was coated with Ag prior to the CNT growth. Tip is imaged from the side. Tip is 187 nm long		
23-Mar-10	2 of 3 Sent to UTK		
Can be used as is for scanning.			

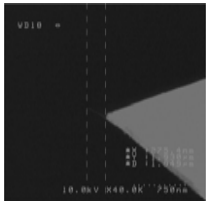
23

TIP NUMBER	DESCRIPTION	IMAGES	
100322-1-5	Conductive CNT tip. Grown on Si tip. The AFM tip was coated with Ag prior to the CNT growth. Tip is imaged from the side. Tip is 211 nm long		
23-Mar-10	3 of 3 Sent to UTK		
Can be used as is for scanning. Note: Do not SEM image these tips prior to scannng with AFM. They can be put into the SEm for review after the scanning.			

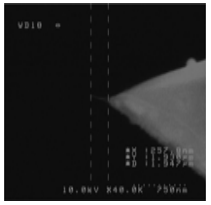
24

TIP NUMBER	DESCRIPTION	IMAGES	
100323-1-8	Conductive CNT tip. Grown on Si tip. The AFM tip was coated with Ag prior to the CNT growth. Tip is imaged from the side. Tip is 586 nm long		
26-Mar-10	1 of 3 Sent to UTK		
Tip can be scanned directly but with more care as it is longer then 500 nm.			

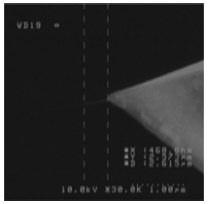
25

TIP NUMBER	DESCRIPTION	IMAGES	
100323-1-9	Conductive CNT tip. Grown on Si tip. The AFM tip was coated with Ag prior to the CNT growth. Tip is imaged from the side. Tip is 275 nm long		
26-Mar-10	2 of 3 Sent to UTK		
Good to weld at the base.			

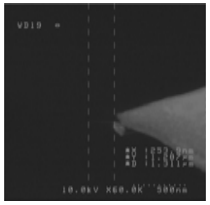
26

TIP NUMBER	DESCRIPTION	IMAGES	
100323-1-10	Conductive CNT tip. Grown on Si tip. The AFM tip was coated with Ag prior to the CNT growth. Tip is imaged from the side. Tip is 258 nm long		
26-Mar-10	3 of 3 Sent to UTK		
Good to weld at the base. Note: Do not SEM image these tips prior to scannng with AFM. If you put the tips into SEM then must weld the end. You can put them into the SEM for review after the scanning.			

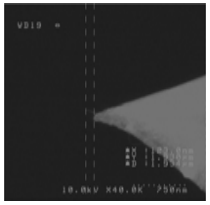
27

TIP NUMBER	DESCRIPTION	IMAGES	
100323-1-5	Conductive CNT tip. Grown on Si tip. The AFM tip was coated with Ag prior to the CNT growth. Tip is imaged from the side. Tip is 469 nm long		
26-Mar-10	1 of 3 Sent to SUNY Albany		
Can be used to e-beam deposit metal to the CNT tip base.			

28

TIP NUMBER	DESCRIPTION	IMAGES	
100323-1-11	Conductive CNT tip. Grown on Si tip. The AFM tip was coated with Ag prior to the CNT growth. Tip is imaged from the side. Tip is 254 nm long		
26-Mar-10	2 of 3 Sent to SUNY Albany		
Can be used to e-beam deposit metal to the CNT tip base.			

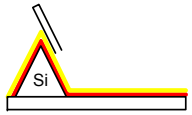
29

TIP NUMBER	DESCRIPTION	IMAGES	
100323-1-12	Conductive CNT tip. Grown on Si tip. The AFM tip was coated with Ag prior to the CNT growth. Tip is imaged from the side. Tip is 123 nm long		
26-Mar-10	3 of 3 Sent to SUNY Albany		
Can be used to e-beam deposit metal to the CNT tip base. Note: May be better if the weld is a line or small area rather then a spot. This will catch any drift in the e-beam. The weld can be as small as 10-20 nm, it does not have to be too large.			

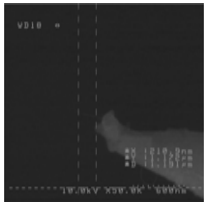
30

TIP NUMBER	DESCRIPTION	IMAGES	
100423-1-0	These are reference tips, fabricated to confirm that electrical measurements involve CNTs, not just the Si tip.		No SEM Image
30-Apr-10	1 of 2 Sent to NIST		

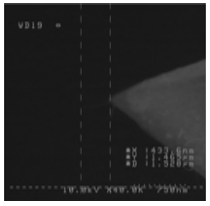
31

TIP NUMBER	DESCRIPTION	IMAGES	
100423-1-1	These are reference tips, fabricated to confirm that electrical measurements involve CNTs, not just the Si tip.		No SEM Image
30-Apr-10	2 of 2 Sent to NIST		

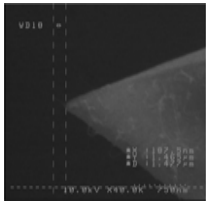
32

TIP NUMBER	DESCRIPTION	IMAGES	
100325-1-9	Ag coated base CNT tip. To be used as reference.		 211 nm – T15 Cantilever
4-Jun-10	1 of 8 Sent to NIST		

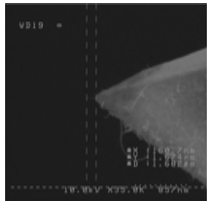
33

TIP NUMBER	DESCRIPTION	IMAGES	
100401-1-1	Ag coated base CNT tip. To be used as reference.		 434 nm – B300 Cantilever
4-Jun-10	2 of 8 Sent to NIST		

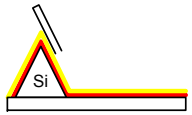
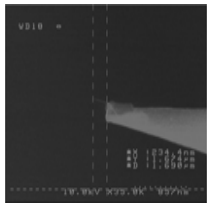
34

TIP NUMBER	DESCRIPTION	IMAGES	
100401-1-2	Ag coated base CNT tip. To be used as reference.		 188 nm – B300 Cantilever
4-Jun-10	3 of 8 Sent to NIST		

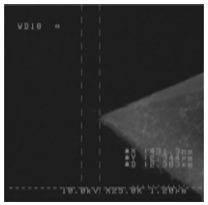
35

TIP NUMBER	DESCRIPTION	IMAGES	
100401-1-4	Ag coated base CNT tip. To be used as reference.		 161 nm – B300 Cantilever
4-Jun-10	4 of 8 Sent to NIST		

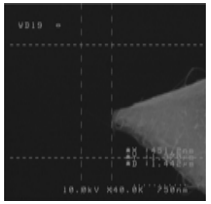
36

TIP NUMBER	DESCRIPTION	IMAGES	
100401-1-5	Ag coated base CNT tip. To be used as reference.		 234 nm – B300 Cantilever
4-Jun-10	5 of 8 Sent to NIST		

37

TIP NUMBER	DESCRIPTION	IMAGES	
100402-0-1	Ag coated base CNT tip. To be used as reference.		 431 nm – B300 Cantilever
4-Jun-10	6 of 8 Sent to NIST		

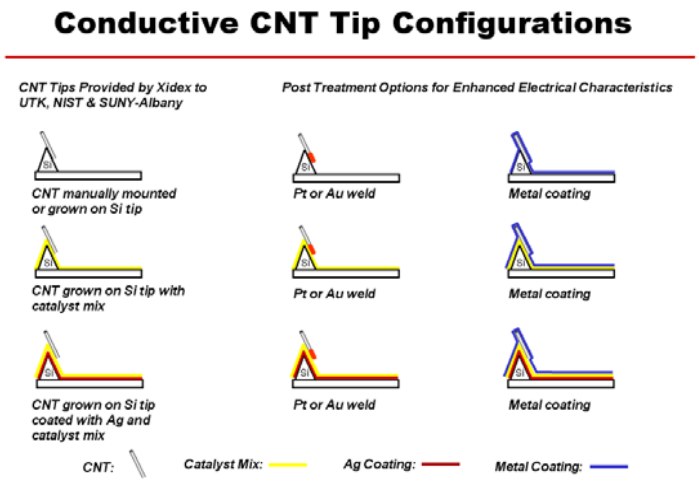
38

TIP NUMBER	DESCRIPTION	IMAGES	
100405-1-7	Ag coated base CNT tip. To be used as reference.		 451 nm – B300 Cantilever
4-Jun-10	7 of 8 Sent to NIST		

39

TIP NUMBER	DESCRIPTION	IMAGES	
100406-1-15	Ag coated base CNT tip. To be used as reference.		 523 nm – B300 Cantilever
4-Jun-10	8 of 8 Sent to NIST		

LEGEND



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