Graphene Nanoribbon Schottky-barrier FETs for End-of-the-roadmap CMOS: Challenges and Opportunities

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On the ITRS roadmap [1], the physical gate length, L_G, has been rapidly scaling down, and will reach values below ~ 10nm beyond 2020 (see Table I, shaded region). The single-gate (SG) extremely thin SOI (ETSOI) MOSFET, the double-gate (DG) FinFET, and the gate-all-around (GAA) Si nanowire (SiNW) MOSFET geometries may facilitate such scaling [2-4]. Nevertheless, sub-10nm L_G scaling will be a great challenge because of the significant mobility degradation [5] and channel thickness variations [2] in the aforementioned geometries with a few-nanometer body thicknesses as required by electrostatic short-channel considerations. Therefore, new device geometries and technologies are required that could simultaneously maintain the electrostatic integrity and the superior transport properties for sub-10nm L_G scaling. It has been recently shown that the *atomic-thin-body* (ATB) geometry can meet the electrostatic requirements for $L_G \leq 10$nm [6]. At the ATB limit, carbon electronics based on graphene nanoribbons (GNRs) with tunable band gaps [7] have been widely considered for high-performance digital electronics [8-10]. Here, ballistic transport of GNR Schottky-barrier (SB) FETs is simulated self-consistently [6], including both thermionic emission and tunneling. We show the better gate length scalability of GNRs compared to Si MOSFETs, even though *significant* material related challenges will have to be overcome. L_G scaling below 10nm is mainly limited by direct source-to-drain tunneling and the ambipolar effect in the off-state, which can be suppressed by narrower ribbon widths (of the order ~ 1nm), and larger effective masses obtained from bandstructure engineering. If a *negative* metal-graphene SB-height could be achieved, the GNR SB-FET could operate without significant series resistance effects, and deliver high on-current (I_{ON}) [11]. The performance of the *ultimate* GNR SB-FETs is comparable to the MOSFET targets of the ITRS roadmap [1].

Fig. 1 compares the electrostatic scaling length λ for SG, DG, and GAA-SiNW MOSFETs with a channel thickness of 5nm to SG and DG GNR SB-FETs. λ is obtained from the evanescent-mode analysis for Si MOSFETs [3], and the 2D Laplace solution for graphene [6]. To maintain a good short-channel control, $\lambda < L_G/1.5\pi$ is necessary [3]. For $L_G \leq 10$nm, only GAA-SiNW and GNR can meet this requirement (Fig.1, region below the dashed line), and furthermore, the GNR shows better scalability.

In order to work at the end-of-the-roadmap, however, GNR SB-FETs also need to meet the off-current (I_{OFF}) $\leq$ 100nA/µm requirement [1]. I_{OFF} vs. L_G is shown in Fig. 2. As L_G scales below 50nm, I_{OFF} starts to increase, and the *incremental degradation* rises faster at L_G = 10nm, which can be explained by the band diagrams and the current transmission plot for L_G = 10, 20, and 30nm, respectively, in Fig. 3. From L_G = 30nm down to 20nm, I_{OFF} increases due to the drain-induced-barrier-lowering (DIBL) effect. From L_G = 20nm down to 10nm, the DIBL becomes larger and the direct tunneling is also turned on. The latter increases faster and becomes the dominant off-state leakage mechanism at smaller L_G. Therefore, a low direct tunneling leakage requires larger band gaps, so that very narrow GNRs (~ 1nm) are necessary: a great material challenge. Fig. 4 shows the deviation of transfer characteristics as the ribbon width w varies from 0.8 to 1.6nm (edge roughness is not included in our model). I_{ON} is not very sensitive to w, but for L_G = 10nm, the 1.6nm ribbon has ~ 10x larger I_{OFF} than the other ribbons due to the ambipolar effect, Fig. 4(a). This effect is not significant for larger L_G, i.e. L_G = 20nm in Fig. 4(b).

In order to suppress the direct tunneling in the off-state, bandstructure engineering such as strain engineering can be utilized [12, 13]. Either larger effective masses, m^*, and/or larger band gaps, E_G, can reduce the tunneling transmission. Here, we define m^* of GNRs to be $\hbar^2 \left(d^2E/dk^2|_{k=0}\right)^{-1}$, and assume $E_C = \sqrt{(\hbar v_F k)^2 + (E_G/2)^2}$, and the imaginary bandstructure $E_C^{im} = \sqrt{-(\hbar v_F \kappa)^2 + (E_G/2)^2}$ [6]. If m^* is increased to $r \times m^*$ and E_G is kept the same, $E_C^{im} = \sqrt{-(\hbar v_F \kappa)^2 / r + (E_G/2)^2}$ and κ is increased to $\sqrt{r} \times \kappa$ in our model [6]. Also, the density of states DOS is changed to $\sqrt{r} \times DOS$. We stress that the above model is phenomenological, only intended to explore the influence of the tunneling mass, and will require appropriate bandstructure engineering for practical realization. Fig. 5(a) shows that for L_G = 7.4nm at the end of the 2009 roadmap, the original GNR *cannot* meet the I_{OFF} requirement, while with increased m^* (2.25x), the direct tunneling can be completely suppressed to meet the I_{OFF} target. For GNR SB-FETs, however, I_{ON} also depends on tunneling transmission, and reduces by larger m^*. Therefore, a *negative* metal-graphene SB height is required in order to obtain MOSFET like behavior in GNR SB-FETs [11] (Fig. 5(b)), with large I_{ON}. Fig. 6 shows the transfer characteristics with L_G = 7.4nm confirming that I_{OFF} of the original GNR SB-FET (dotted line) can be reduced to 100nA/µm by a larger m^* (dashed line), and subsequently, I_{ON} can be improved by a negative SB height (solid line). Table 1 summarizes the performance projections for GNR SB-FETs at the end of the roadmap, and it is recognized that Small contact resistances, in addition to the aforementioned requirements, will also be needed to meet the ITRS targets [1].

In summary, carbon electronics based on GNRs can potentially meet the ITRS performance requirements at the end-of-the-roadmap with $L_G \leq 10$nm. Nevertheless, significant challenges with regard to material engineering will have to be surmounted.

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Table 1 Performance projections for the GNR SB-FETs at the end of the roadmap. The influence of series resistance (values in red) in addition to Schottky-barrier injection is also indicated.

	Si MOSFET		GNR SB-FET (w = 1.2 nm)		
	2020	2024	Φ_B = 0.1 eV, m*	Φ_B = -0.25 eV, 3x m*	unit
Supply voltage V_{DD}	0.68	0.60	0.68	0.60	V
Gate length L_G	10.7	7.4	10	7.4	nm
Equivalent oxide thickness EOT	0.59	0.50	0.59	0.39	nm
Drive current I_D	1870	2170	1768 / 3268	2099 / 3577	µA/µm
Off-state leakage current I_{OFF}	100	100	100	100	nA/µm
Effective series S/D resistance R_{SD}	120	110	120 / 0	110 / 0	Ω-µm
Total gate capacitance C_G	0.55	0.46	0.76	0.83	fF/µm
Intrinsic delay ~ $C_G V_{DD} / I_D$	0.20	0.13	0.29 / 0.16	0.24 / 0.14	ps
	ITRS 2009				

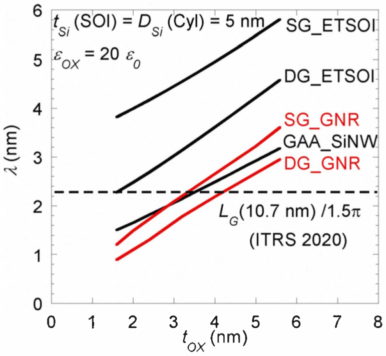


Fig. 1 Comparison of electrostatic scaling length λ for SG, DG, and GAA-SiNW FETs, and SG and DG GNR-FETs. λ is obtained from the evanescent-mode analysis for Si [2], and from the 2D Laplace solution for graphene [5]. λ should be below the dashed horizontal line in order to meet the electrostatic short-channel immunity at L_G = 10.7 nm.

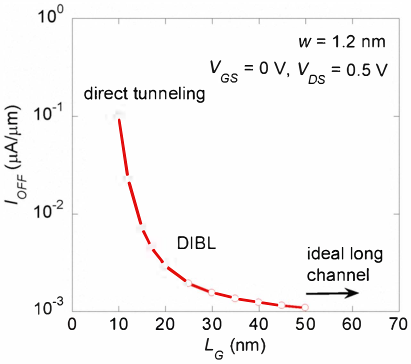
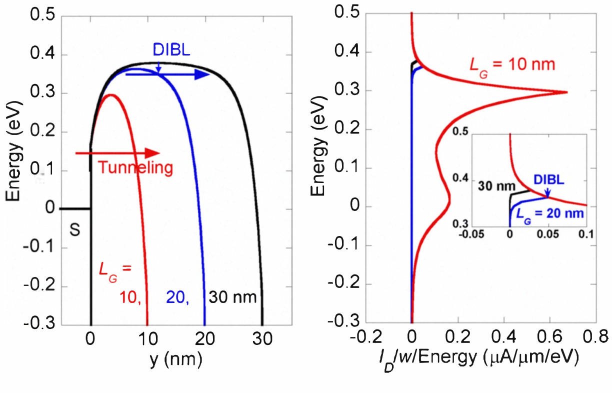


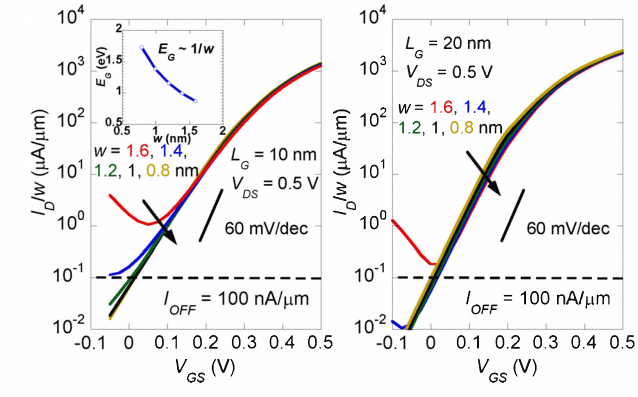
Fig. 2 Off-state current vs. gate length of a SG GNR SB-FET at V_{DS} = 0.5 V. The top gate oxide thickness is 3 nm and dielectric constant $\varepsilon_{OX} = 20\varepsilon_0$. The ribbon width is 1.2 nm, corresponding to an energy bandgap of 1.1 eV.



(a)

(b)

Fig. 3 (a) Band diagram and (b) current density per energy in the off-state for the SG GNR SB-FETs with L_G = 10, 20, 30 nm, respectively. The inset of (b) zooms in the transmission of L_G = 20 and 30 nm, showing the transmission peak shifts downward for L_G = 20 nm due to DIBL.



(a)

(b)

Fig. 4 Transfer characteristics of SG GNR SB-FETs with gate length of (a) 10 nm, and (b) 20 nm. The ribbon width varies from 0.8 to 1.6 nm, with corresponding $E_G \sim 1/w$ [6] shown in the inset of (a).

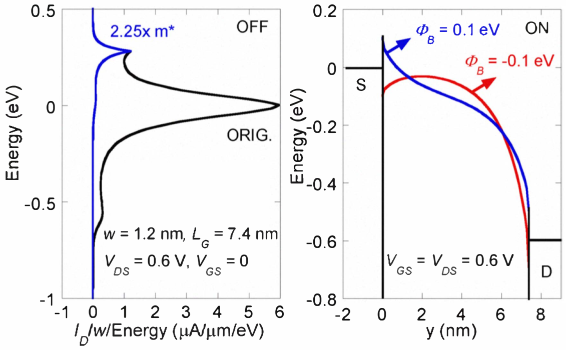
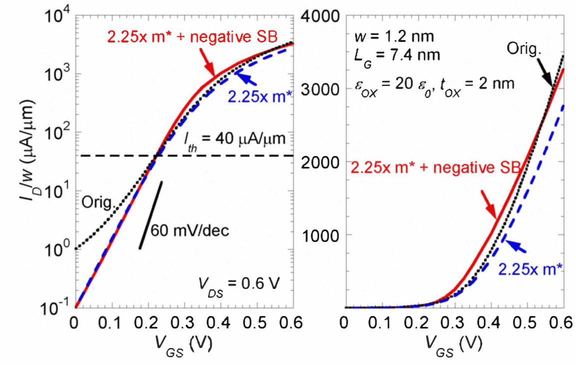


Fig. 5 (a) Current density per energy in the off-state for the SG GNR SB-FETs with L_G = 7.4 nm, showing larger effective mass can suppress direct tunneling at short channel lengths. (b) Band diagram in the on-state of GNR SB-FETs with SB height of 0.1eV and -0.1eV, respectively. t_{OX} = 2 nm, $\varepsilon_{OX} = 20\varepsilon_0$ have been used.



(a)

(b)

Fig. 6. (a) Log- and (b) linear-scale transfer characteristics of SG GNR SB-FETs at the end of the roadmap with L_G = 7.4nm, w = 1.2nm, V_{DD} = 0.6 V, t_{OX} = 2nm, $\varepsilon_{OX} = 20\varepsilon_0$. The dotted line shows the original GNR SB-FET cannot satisfy the 100nA/µm off-current requirement. But the off-current can be reduced by increasing the effective mass (dashed line) and at the same time a negative SB can help maintain the high on-current (solid line).