Nanoelectronics • Architectures

MIND

MIDWEST INSTITUTE FOR NANOELECTRONICS DISCOVERY

Graphene Nanoribbon Tunnel FETs

K. Tahy (Expt.) – with help from B. Raynal & J. Fleming
T. Fang, P. Zhao, Q. Zhang[†], S. Koswatta[*] (Theory),
M. Kelly, G. Xing, D. Jena

Notre Dame, Electrical Engineering
† also with NIST Gaithersburg
* IBM TJ Watson

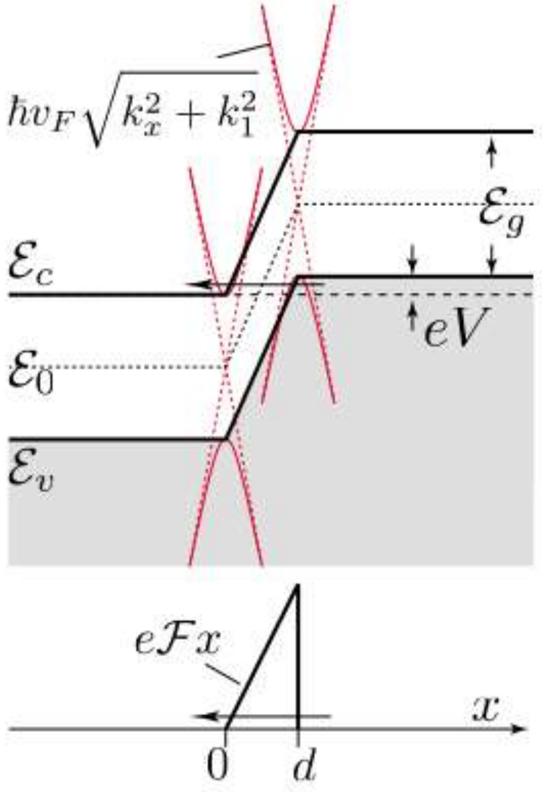
SRC Semiconductor Research Corporation
PIONEERS IN COLLABORATIVE RESEARCH

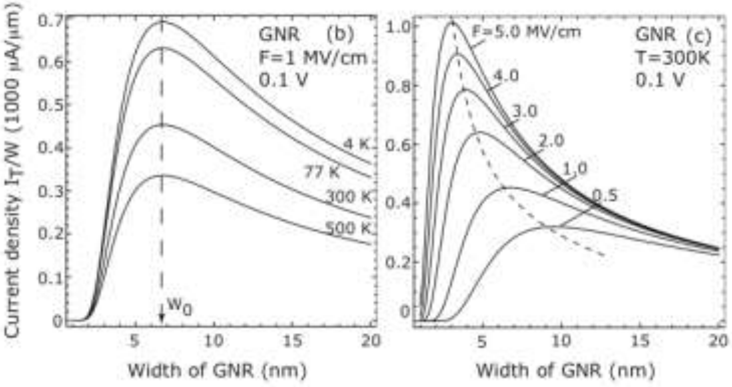
NRI Nanoelectronics RESEARCH INITIATIVE

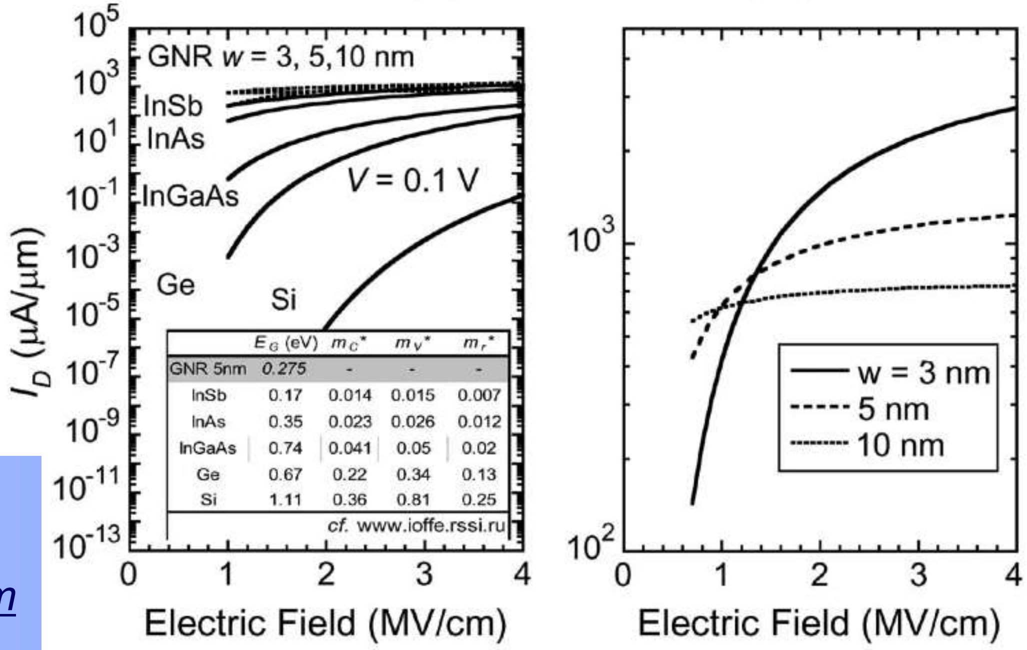
Outline

- *Introduction & Motivation*
- *Graphene Nanoribbons*
- *2D Graphene pn Junctions*
- *Contacts*
- *Summary*

High Tunneling Currents in GNR *pn* Junctions







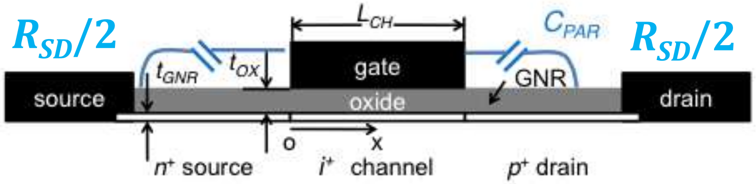
	E_G (eV)	m_C^*	m_V^*	m_r^*
GNR 5nm	*0.275*	-	-	-
InSb	0.17	0.014	0.015	0.007
InAs	0.35	0.023	0.026	0.012
InGaAs	0.74	0.041	0.05	0.02
Ge	0.67	0.22	0.34	0.13
Si	1.11	0.36	0.81	0.25

cf. www.ioffe.rssi.ru

- *GNRs capable of highest tunneling currents > 1 mA/μm @ 0.1 V*
- *Stems from <u>thin body</u> & <u>no lateral momentum</u>*
- *TFET approach: „Scale E_g up from 0 eV’*

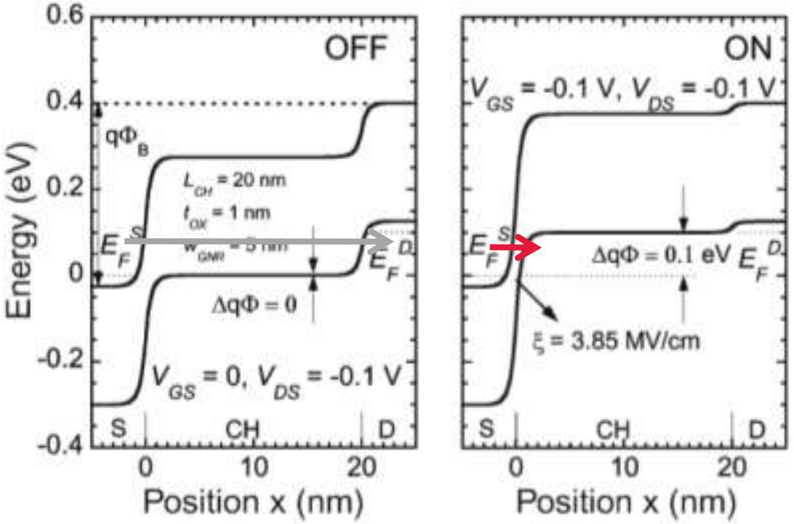
- *APL 93 112106 (2008.9)*

First GNR Tunnel FET Proposal



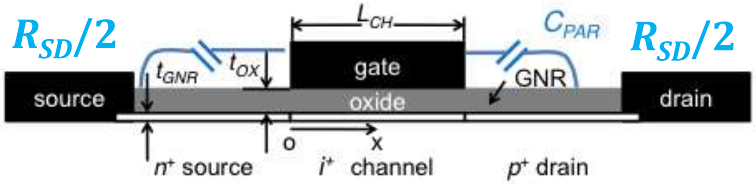
- *TFET: <60 mV/decade subthreshold swing*
- *GNR: high tunneling current*

Gate controlled interband tunneling



- *EDL 29 1344 (2008.12)*

First GNR Tunnel FET Proposal

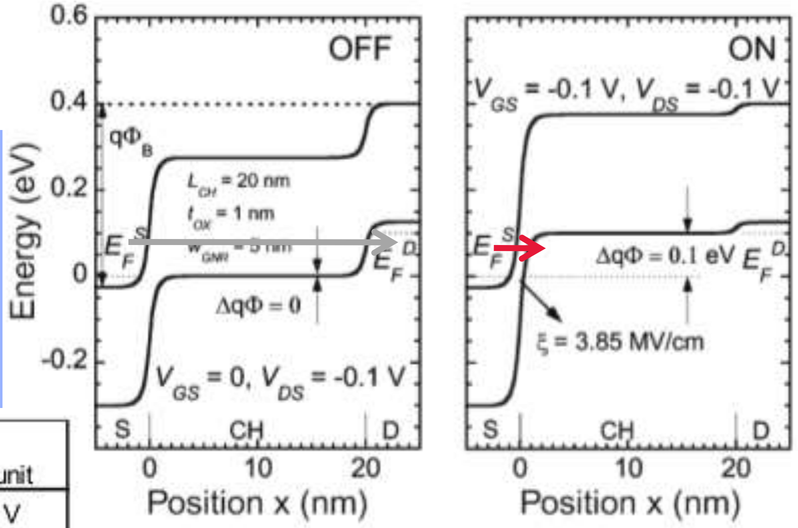


- *TFET: <60 mV/decade subthreshold swing*
- *GNR: high tunneling current*

<u>Compelling performance benefits at low supply voltage:</u>

- *Speed advantages over CMOS: 2x – 3x*
- *Power advantages over CMOS: 50 – 100x*

Gate controlled interband tunneling



	2015 *n*MOSFET		GNR TFET		unit
	single gate	double gate	3 nm single gate		
Supply voltage V_{DD}	0.925	0.95	0.1	0.15	V
Gate length L_G	15	15	20	20	nm
Equivalent oxide thickness *EOT*	0.53	0.77	0.5	0.5	nm
Drive current I_D	1793	1930	137-166	295-383	μA/μm
Off-state leakage current I_{OFF}	710	270	100	100	nA/μm
Effective series S/D resistance R_{SD}	180	180	200-100	200-100	Ω-μm
Total gate capacitance C_G	814	640	376-365	466-454	aF/μm
Intrinsic speed ~ $I_D / C_G V_{DD}$	2413	3195	3646-4545 (151-188%)	6334-8438 (262-350%)	GHz
Off-leakage power ~ $I_{OFF} V_{DD}$	43.8	17.1	0.5 (1.1%)	0.75 (1.7%)	μW/μm^2
Dynamic power ~ 1/2 $I_D V_{DD}$	5.7×10^4	6.0×10^4	$3.4\text{-}4.2 \times 10^2$ (0.6-0.7%)	$1.1\text{-}1.4 \times 10^3$ (1.9-2.5%)	μW/μm^2
	ITRS 2008 Updates				

- *E_G*
- *n^+/p^+* doping
- *R_{SD}*

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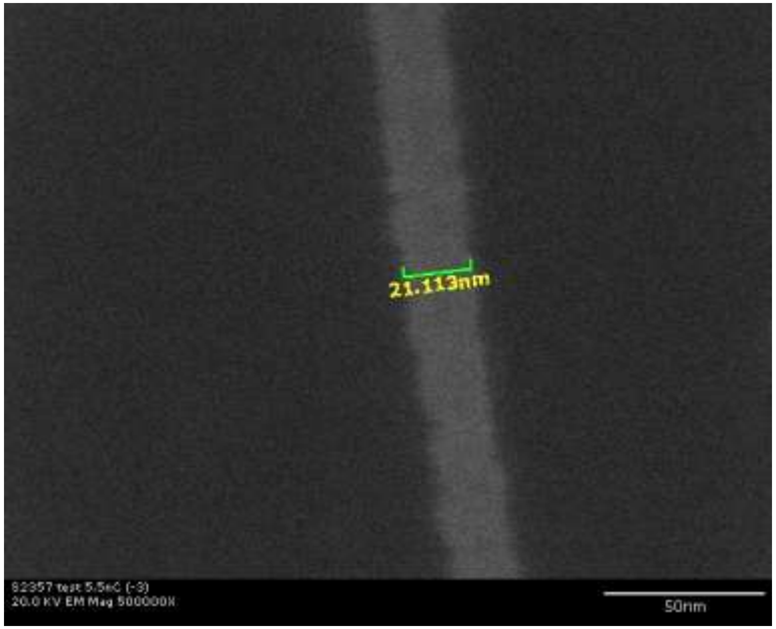
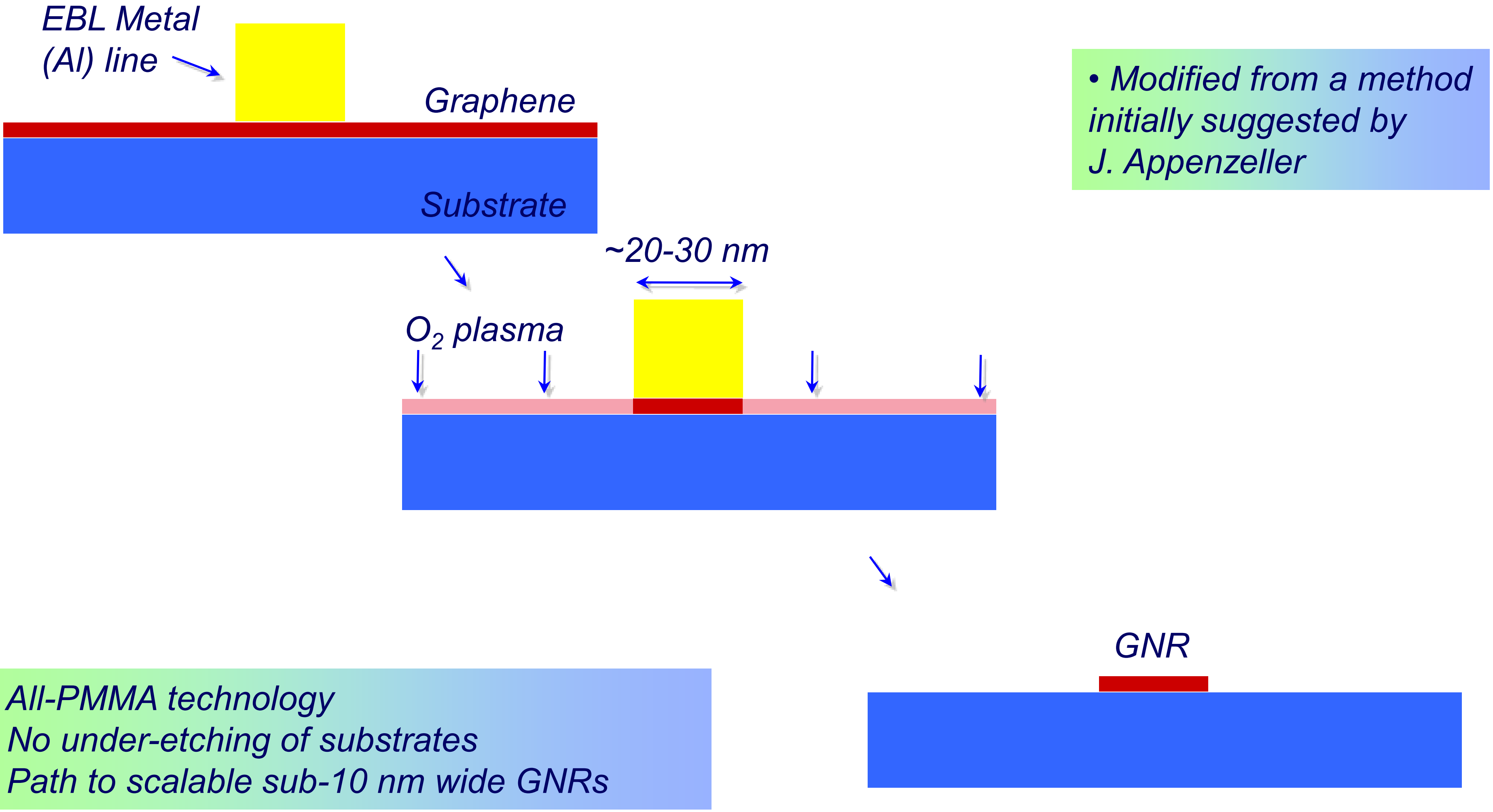


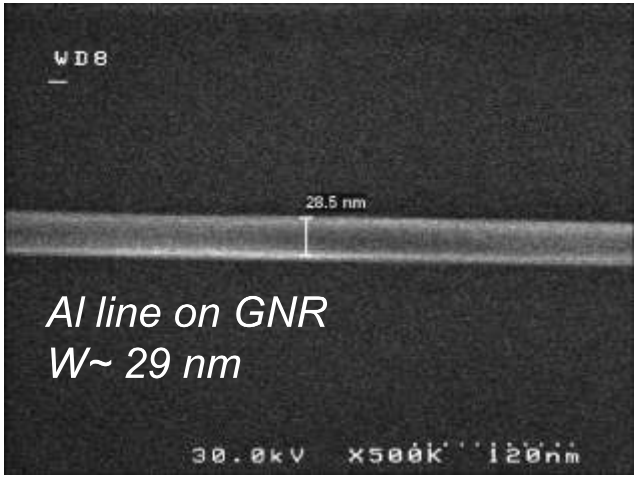
GNRs by Metal-Mask Lithography (MML)



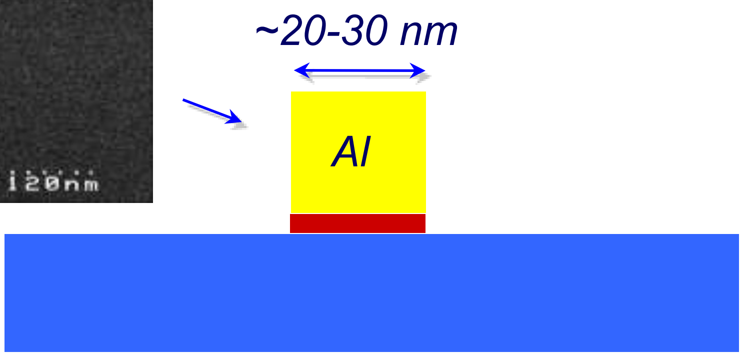
- *Modified from a method initially suggested by J. Appenzeller*

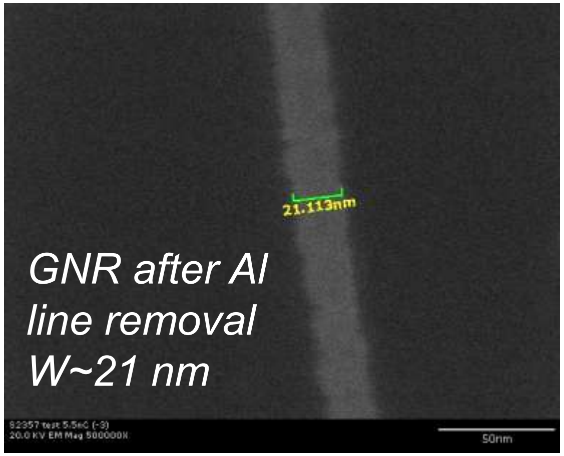
- *All-PMMA technology*
- *No under-etching of substrates*
- *Path to scalable sub-10 nm wide GNRs*

GNRs by Metal-Mask Lithography (MML)

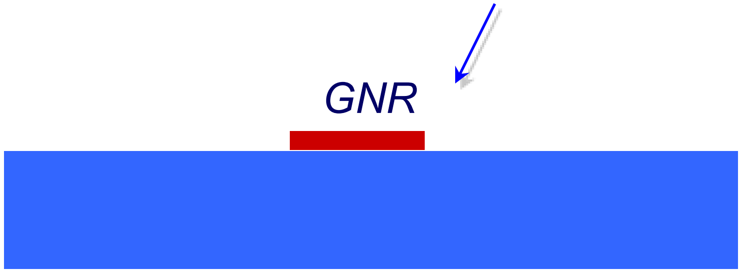


Al line on GNR
W~ 29 nm



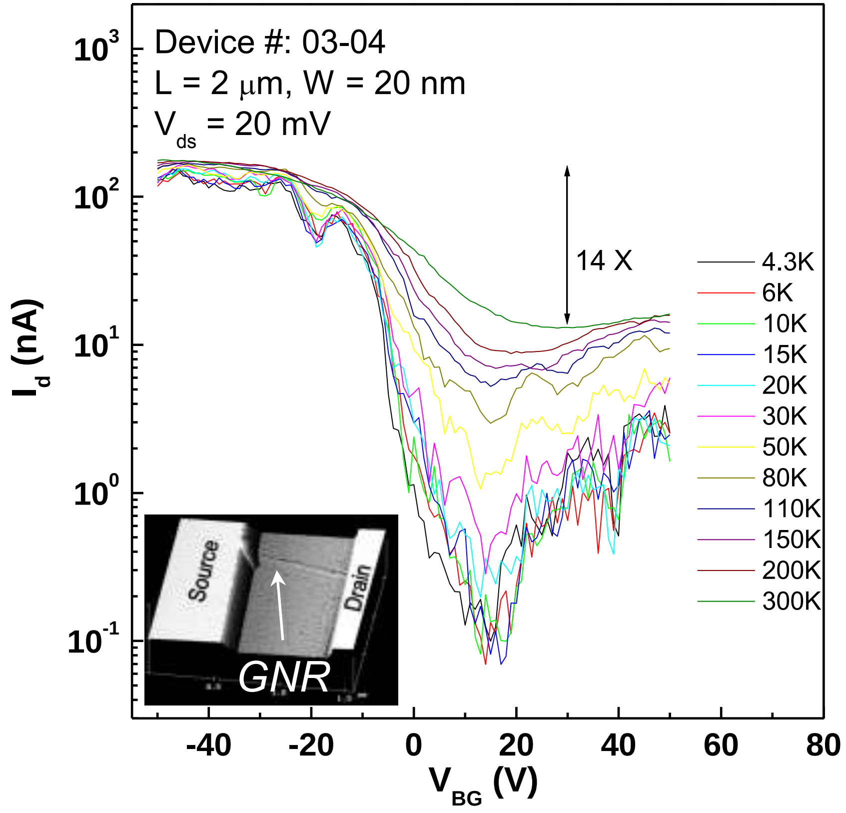


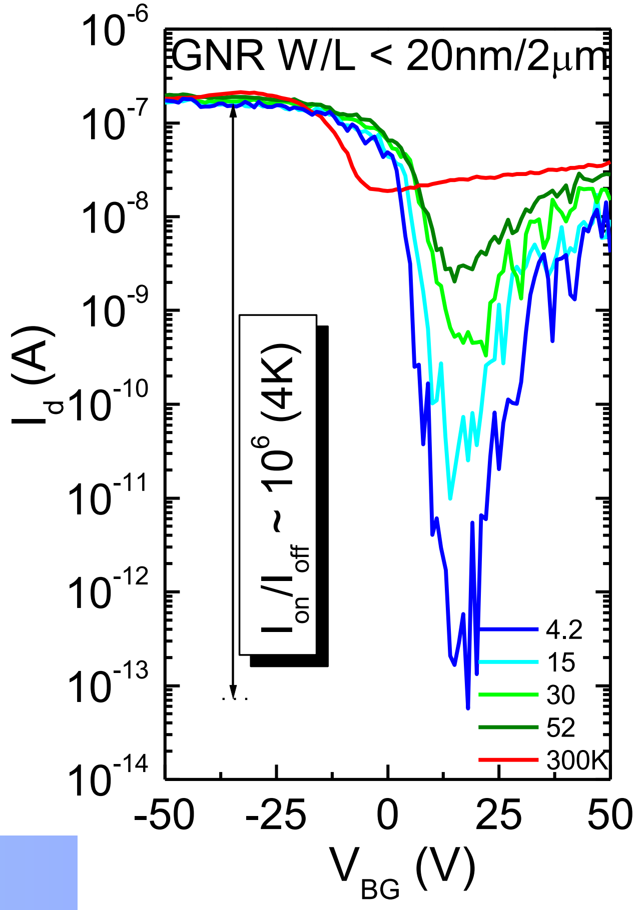
GNR after Al line removal
W~21 nm



- *All-PMMA technology*
- *No under-etching of substrates*
- *Path to scalable sub-10 nm wide GNRs*
- *Thanks to J. Appenzeller for suggestions.*

GNRs by MML: Electronic Properties

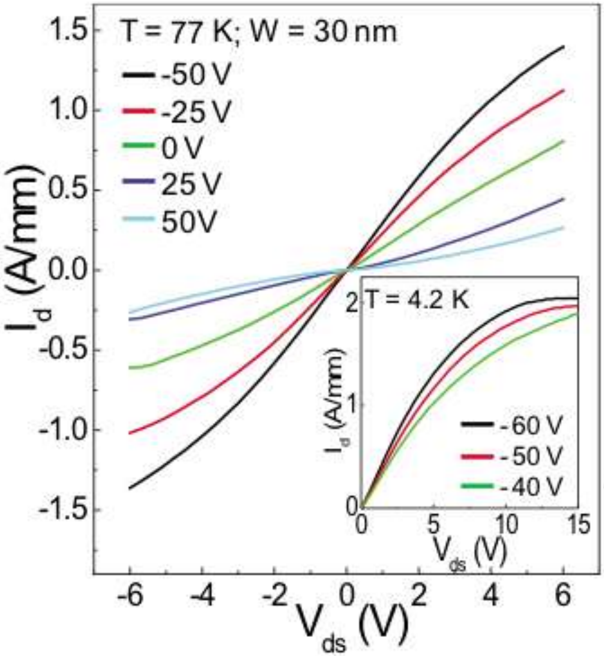


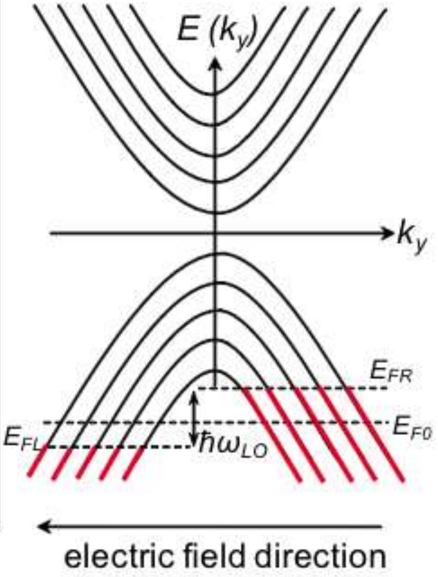


- *20 nm wide GNRs show clear semiconducting behavior*
- *300 K modulation is x10 to x20*
- *Successful processing: High yields of working GNR FETs*

- *APL 96 101309 (2010)*

GNR High-Field Current Drives





- *Modulation is better than 2D Graphene*
- *Back gate: poor electrostatic control*

- *GNRs capable of high current drives*
- *Current densities as high as 2 A/mm (W: 20 – 30 nm)*
- *Conduction enabled by multiple subbands*

→ Current drives are high enough to satisfy required TFET current drives

- *APL 96 101309 (2010)*

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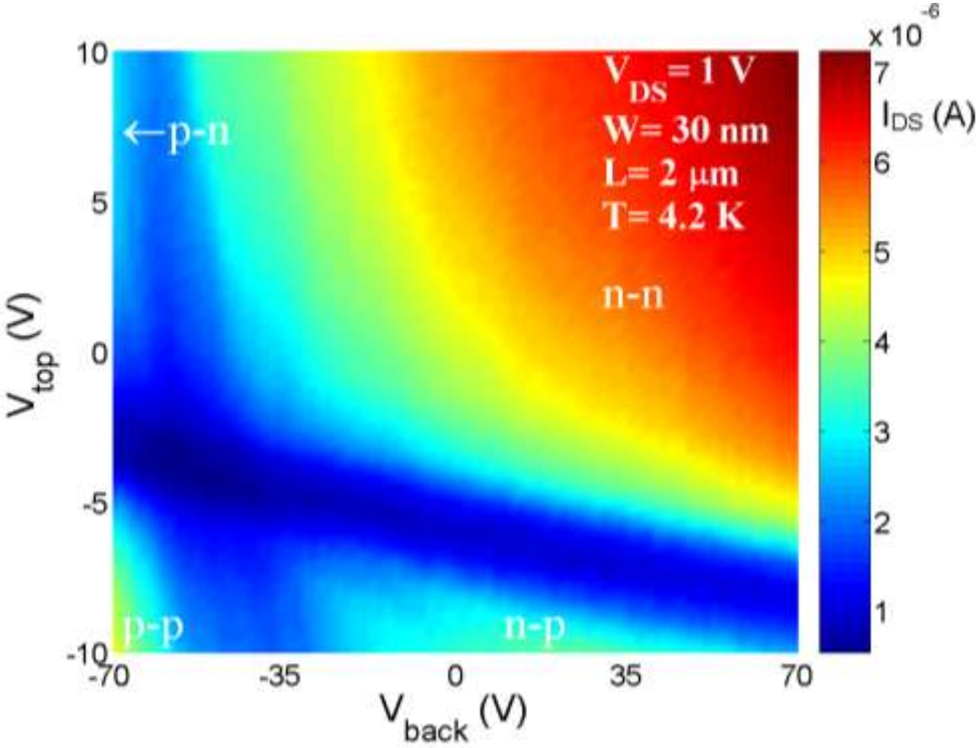
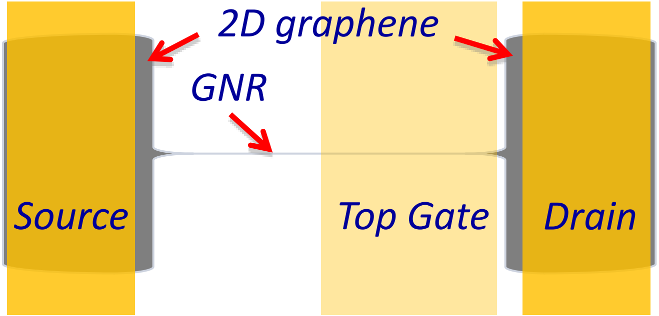


GNR p-n junctions for TFETs



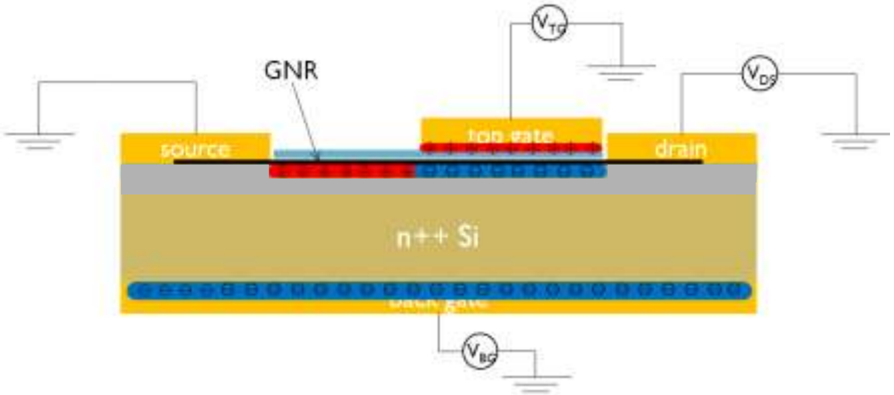
2D graphene

GNR

Source

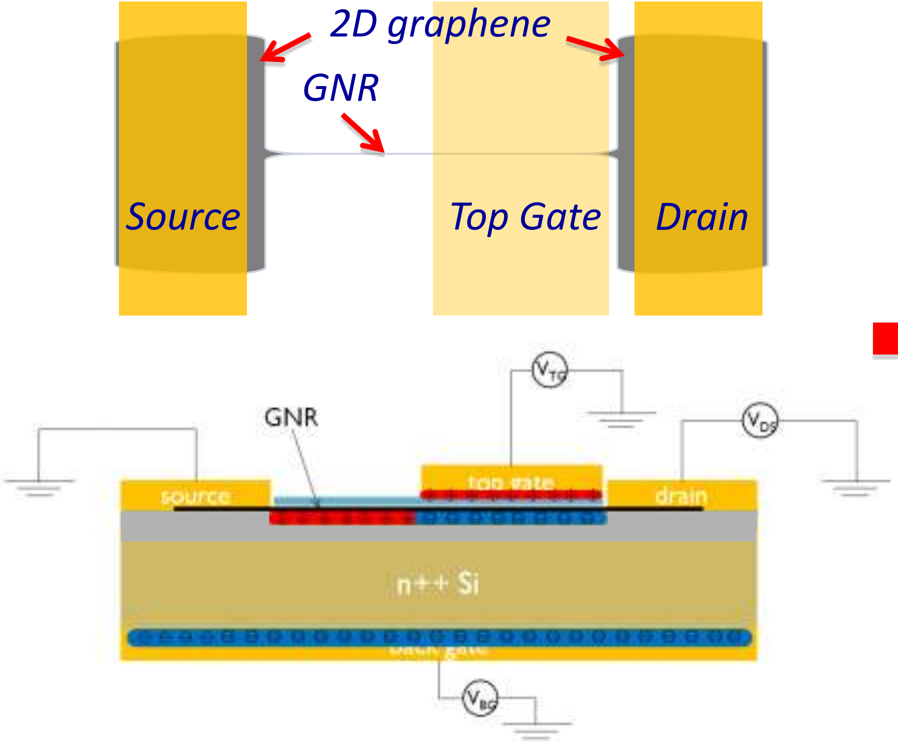
Top Gate

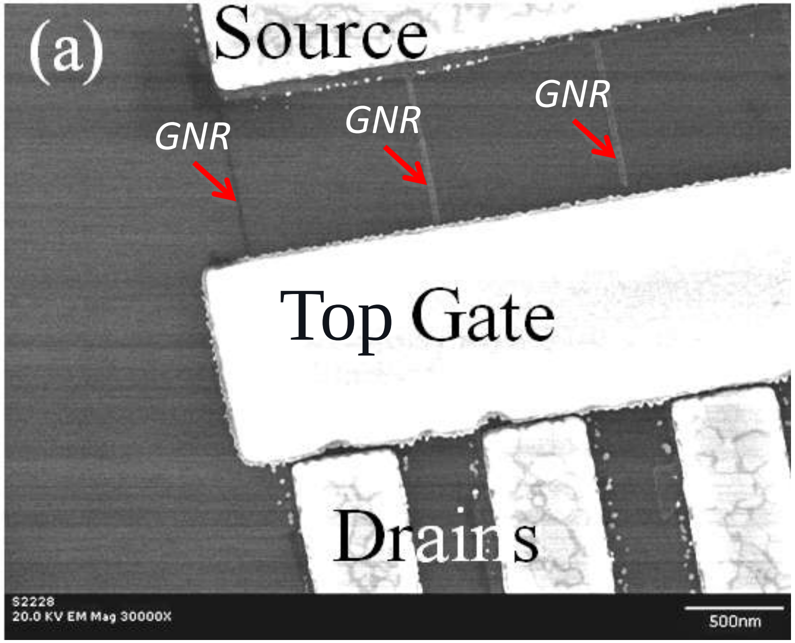
Drain



- *Current embodiment of GNR p-n junctions: Doping through electrostatics (gate bias)*

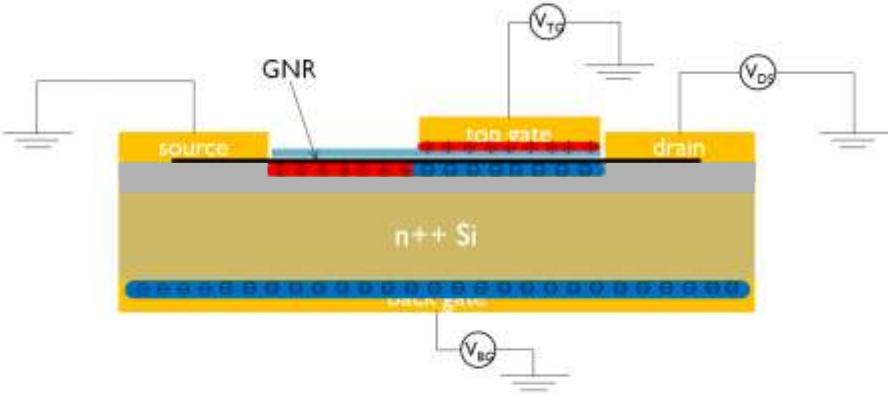
GNR p-n junctions for TFETs

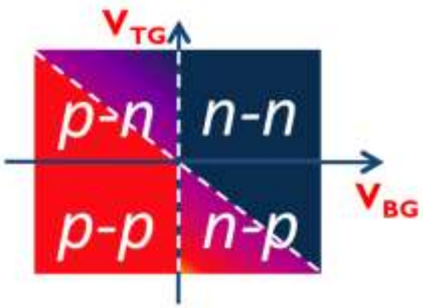




- *Current embodiment of GNR p-n junctions: Doping through electrostatics (gate bias)*
- *Double-gated GNRs used for fabricating arrays of GNR p-n junctions*
- *Fabrication on exfoliated graphene flakes*
- *To be ported to large-area CVD-grown graphene*

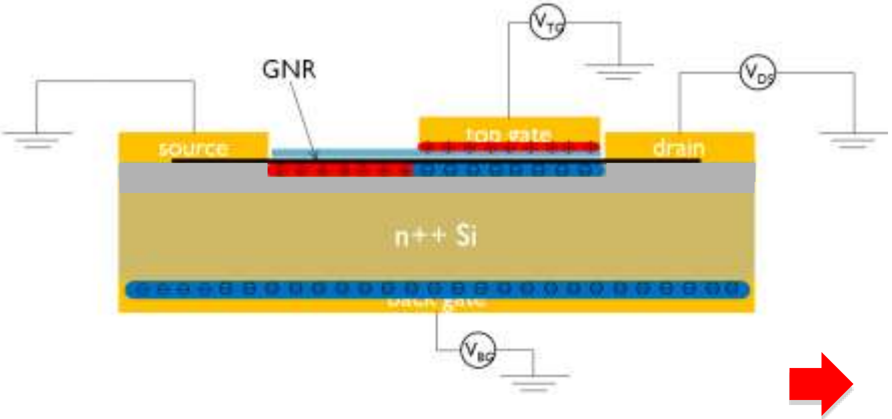
GNR p-n junctions for TFETs

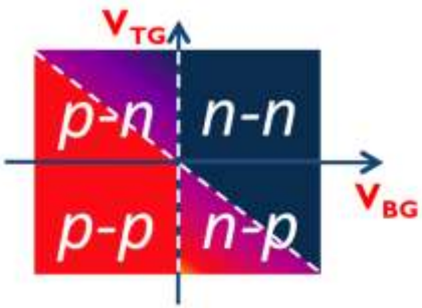


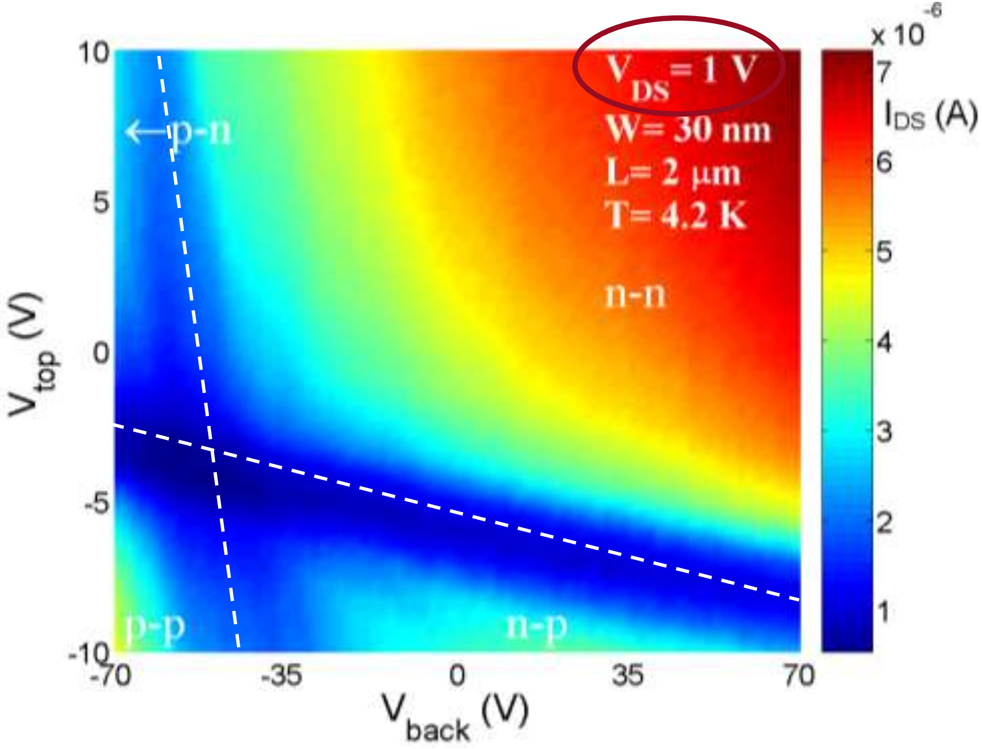


- *Conductivity maps are best indicators of junction types*
- *Note: Width of GNRs~20 nm → E_g~50 meV → Tunneling too high → Effectively 2D graphene*

GNR p-n junctions for TFETs



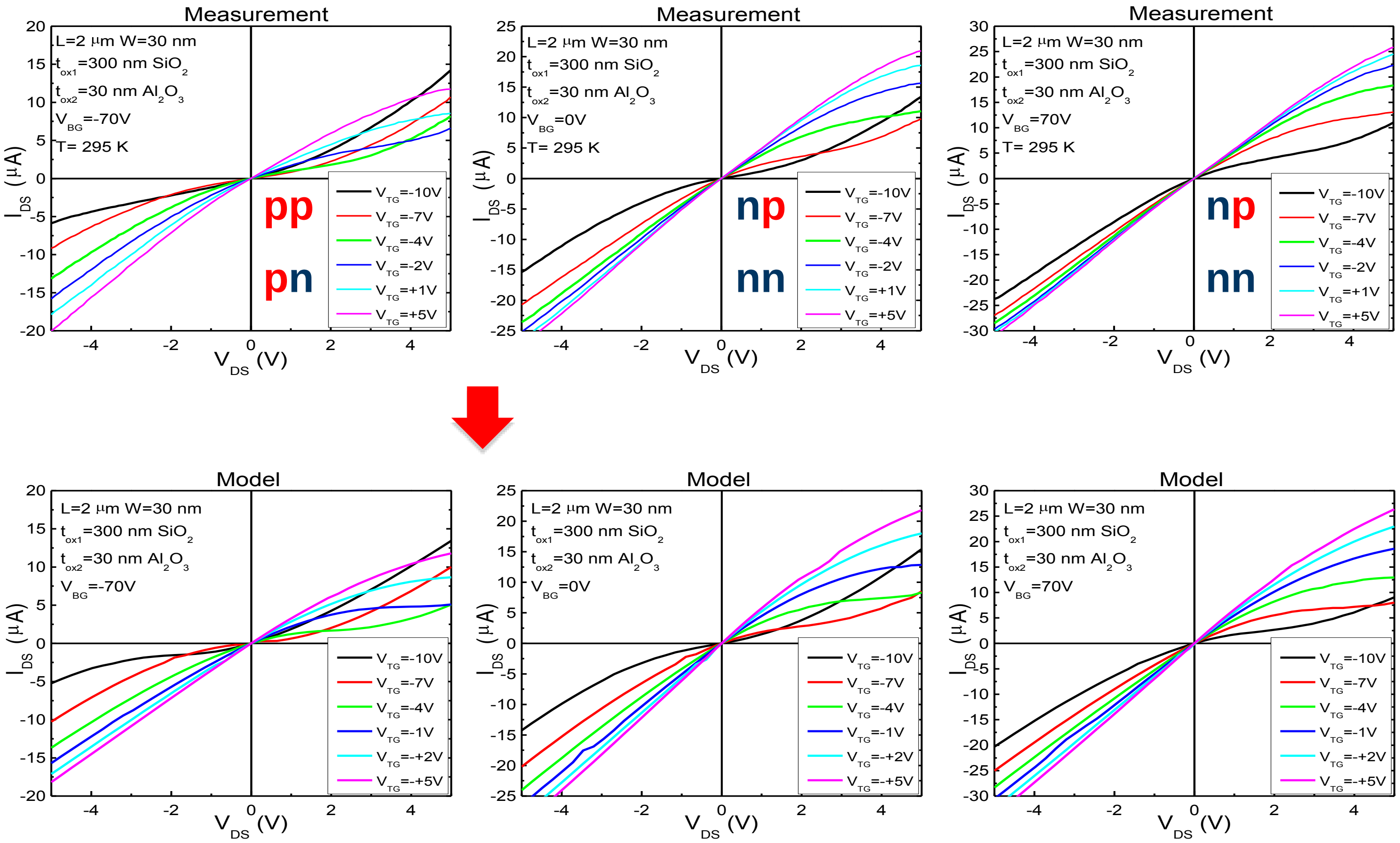


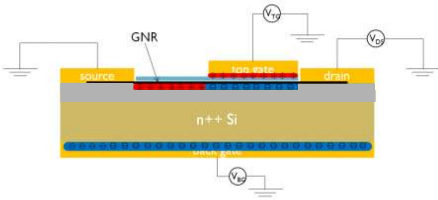


$$q(p-n) = C_{TG}(V_{TG} - V_{TG}^0) + C_{BG}(V_{BG} - V_{BG}^0)$$

- *GNR p-n Junctions realized*
- *Conductivity maps @ hi bias indicate effectively 2D graphene p-n junctions*

GNR p-n junctions for TFETs





- *Model of 2x 2D Graphene FETs in “series” captures entire device characteristics*
- *Conductivity maps @ hi bias indicate effectively 2D graphene p-n junctions*
- *→ Need to shrink GNRs to W<10 nm to get RT TFET behavior*

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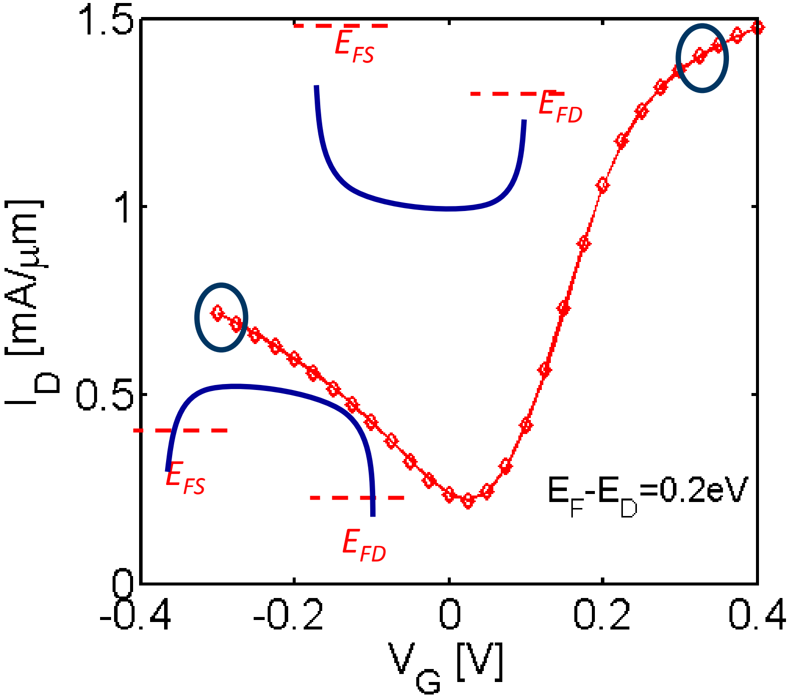
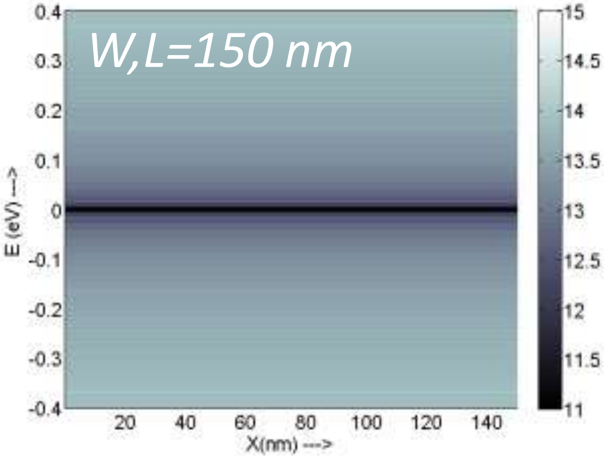
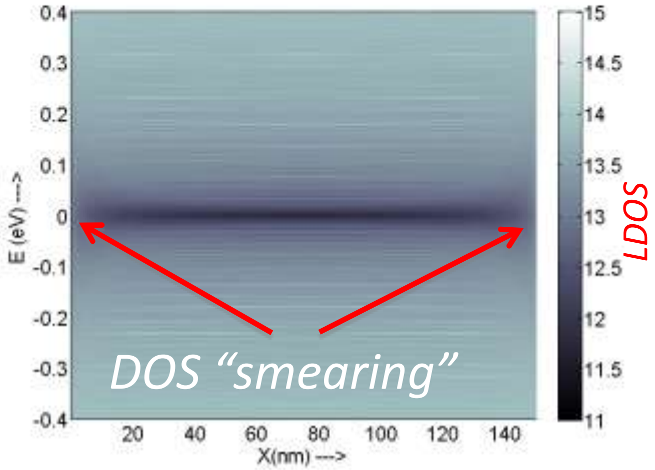


2D Graphene: “Ohmic” Contacts

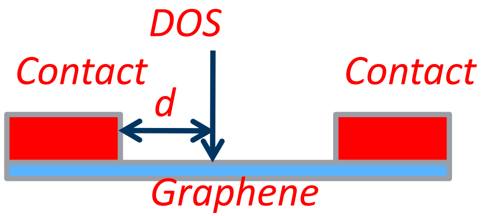


Δ=0meV



DOS “smearing”

Δ=50meV



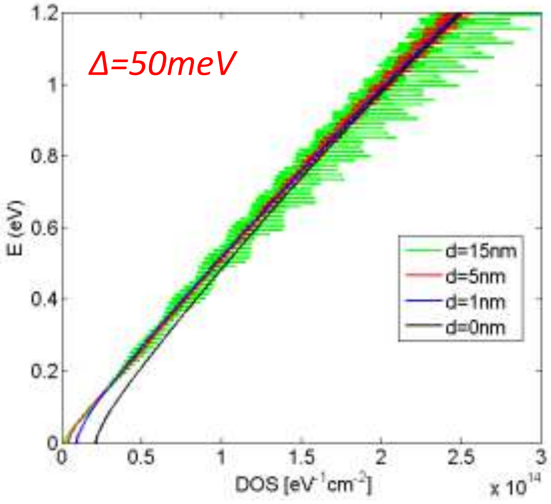
DOS

Contact

d

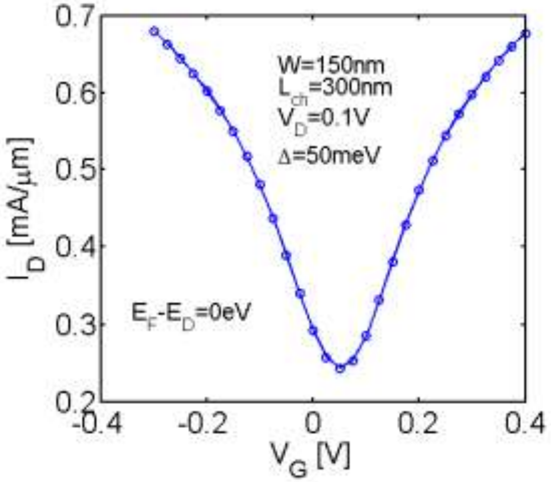
Contact

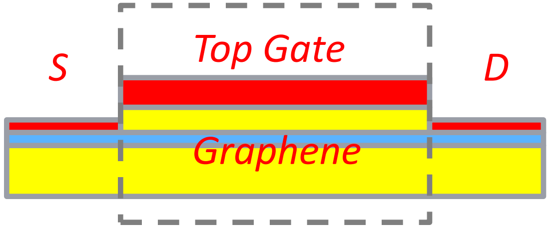
Graphene



- *NEGF simulations of Metal-Induced „Gap’ States in graphene*
- *Metal-Graphene coupling alters graphene bandstructure*
- *Alters device behavior (asymmetric transconductance)*
- *Significant impact on scaling of FETs (both RF & TFETs)*

2D Graphene: “Ohmic” Contacts





- *NEGF simulations of the effect of Work-Function mismatch between graphene & ohmic metals*

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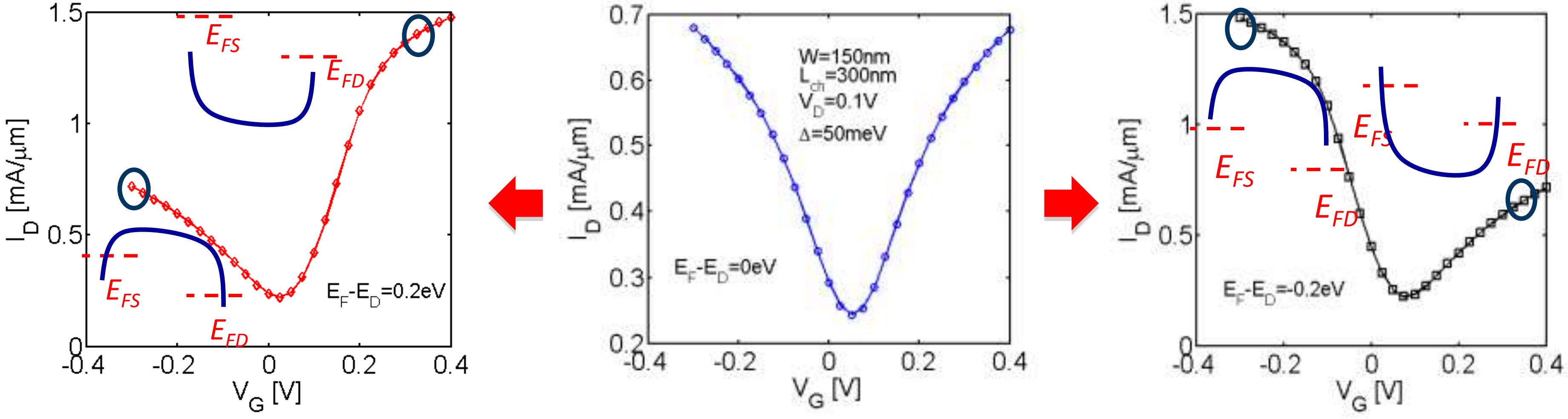
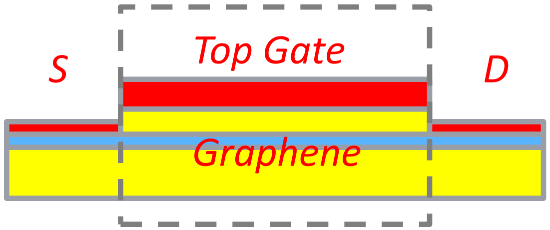


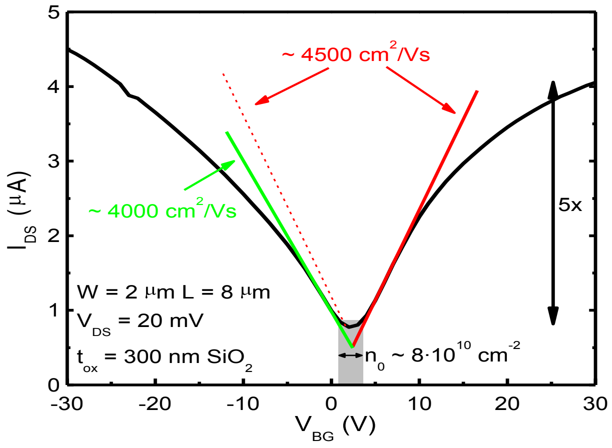


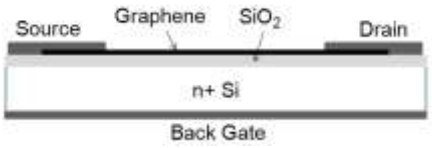
- *NEGF simulations of the effect of Work-Function mismatch between graphene & ohmic metals*
- *Asymmetric transport properties for electrons & holes*
- *Higher drive currents if gate bias „**assists’** work-function difference*
- *Can be used to advantage in TFET design*

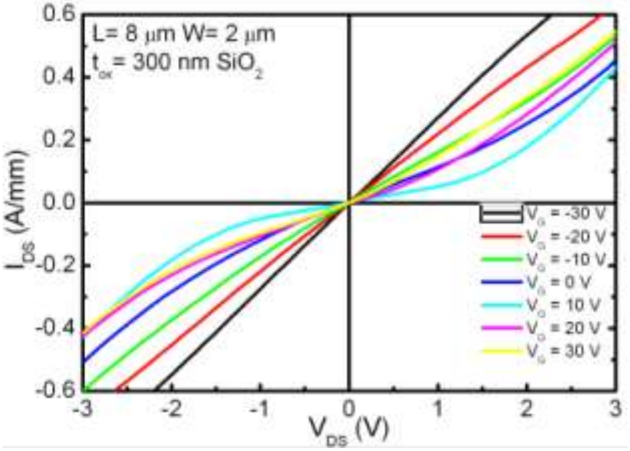
Summary

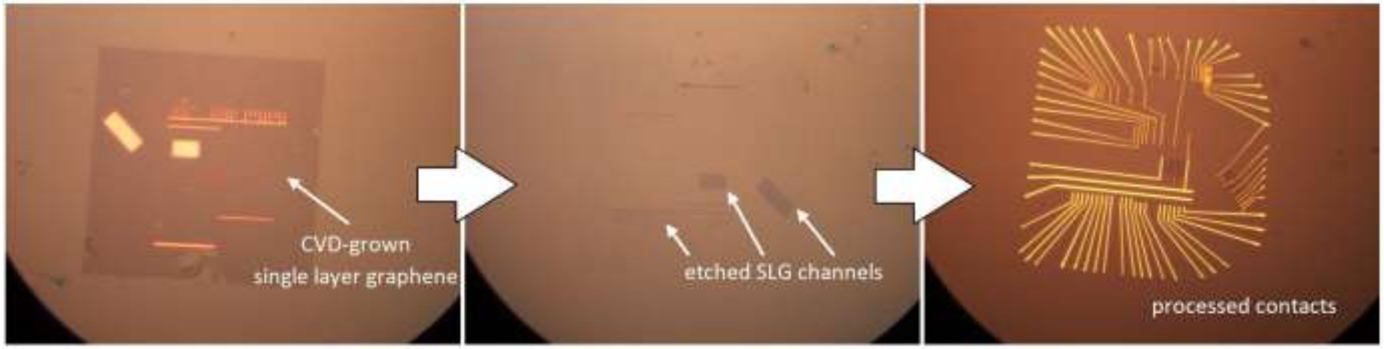
- *GNR TFET is proposed for beyond CMOS logic with high performance and low voltage, where E_G, n^+/p^+ doping and good contacts are required for graphene.*
- *20 nm wide graphene nanoribbons have been fabricated with E_G ~ 50 meV. Larger E_G is needed.*
- *n and p-type dopings in graphene have been demonstrated through electrostatics (gate bias)*
- *NEGF simulations show that contacts can be improved by work-function engineering of the contact metals: higher drive current and asymmetric transconductance can be achieved with large work-function mismatch between graphene and metal.*

CVD Grown Graphene & Characterization









- *Mobilities ~4000 cm²/Vs, FETs demonstrated*
- *Layer transfer process results in low impurity densities (~8x10¹⁰/cm2)*
- *Transfer on to various substrates under investigation.*