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Wafer-level Hall Measurement on SiC MOSFET

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Abstract. Low channel mobility is one of the biggest challenges to commercializing SiC MOSFETs. Accurate mobility measurement is essential for understanding the mechanisms that lead to low mobility. The most widely used effective mobility measurements overestimate the inversion charge for devices that have high level of defects. Mobility measured by the Hall effect is more accurate; however the conventional Hall mobility measurement is tedious. In this work, we demonstrate a wafer-level Hall measurement technique, which is simple and convenient to implement. With this method, extensive study of the mobility degradation is possible.

Introduction

Mobility is the indicator of the intrinsic performance of MOSFETs. An important question during the development of MOSFETs with new materials is that "What is the best achievable mobility?" However, mobility measurements are not simple, particularly when the gate dielectric and its interface are full of defects that trap charges. SiC based MOSFETs are certainly in this category. The often-reported quantity, effective mobility (μ_{eff}), is misleading because it significantly overestimates the inversion charge [1]. Mobility extract by the Hall effect measurement (μ_{Hall}) is free from this problem since only mobile electrons in the channel contribute. Consequently, Hall mobility measurements are sometimes used in the study of SiC MOSFETs to obtain further insight on the device quality [2-4].

Hall mobility measurements are tedious. In addition to the need of a bulky, expensive and dedicated set-up, wafer dicing, wire bonding and device packaging are also needed. Such complexity inhibits frequent measurements. A wide-ranging survey using large number of samples will require heroic efforts and is never done. In this work, we demonstrate a wafer-level Hall measurement method that requires neither packaging nor specialized measurement system. It greatly reduces the efforts needed for Hall measurements and makes device characterization and development more convenient.

Experiments

In these experiments, a donut-shaped permanent magnet with 3 mm inner diameter is placed precisely, using a micro-positioner, above the device under test to provide the magnetic field (the device is placed directly under the center hole of the magnet). The hole in the magnet allows the device as well as the probe contacts to be observable through the microscope. Fig. 1 shows

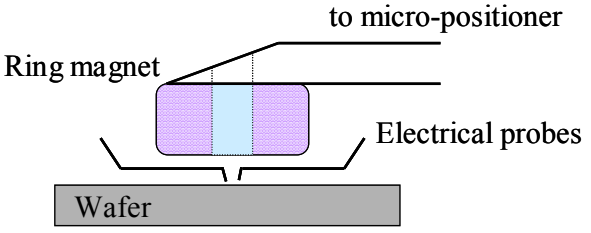

Fig. 1. Wafer-level Hall measurement setup. The magnetic field is provided by a permanent ring magnet. The distance from the wafer is controlled by a micro-positioner.

a schematic of this set-up. The distance of the magnet from the wafer can be adjusted with 25 μm resolution. The magnetic field as a function of distance is calibrated by a small (0.016 mm^2 active area) Hall Sensor. The maximum field this magnet can provide is approximately 3200 Gauss. 4H-SiC MOS-gated Van der Pauw/Hall bar structures are used for this work. The repeatability of the magnetic field is better than 10 Gauss. The size of the gated area is 150 μm × 150 μm.

In order to get μ_{Hall}, inversion sheet charge density (n_s) and sheet resistance (R_s) are measured separately. In the n_s measurement, the gate is kept at a certain potential, the source and substrate are grounded and the drain voltage is modulated from 0.2 V to 0.4 V at 127 Hz with $t_{rise} = t_{fall}$ = 300 μs. The differential voltage between the two Hall terminals is measured using a differential amplifier (10 MΩ input impedance) and monitored with an oscilloscope. The source current is monitored at the same time. This setup is shown in Fig.2. The advantage of using drain voltage modulation is that the noise due to instrumentation can be averaged out within a short period of time. Consequently, the properties of the device under test are less likely to drift during the measurements. This is especially important when measuring SiC MOSFETs, which are known to have significant as-processed charge trapping and de-trapping [5].

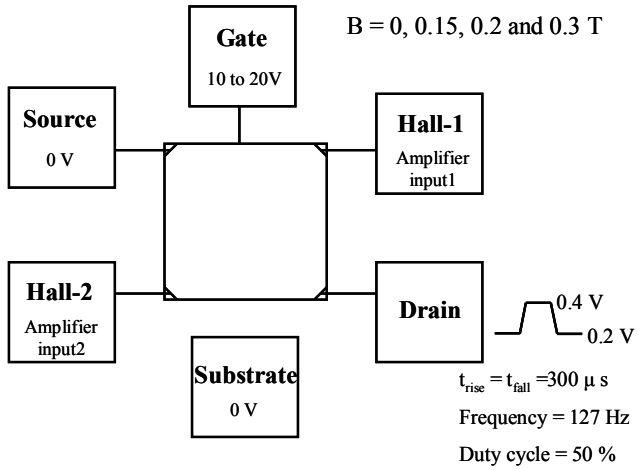

Fig. 2. The 4H-SiC Van der Pauw structure measured, which has an active gate area of 150 μm × 150 μm. The setup shown here is for the inversion sheet charge density (n_s) measurement.

Results and discussions

Since the structure cannot be perfectly symmetric, the differential voltage measured contains an offset voltage, as expressed in Eq. 1 where V_{diff} is the voltage difference between the Hall terminals, V_o is the offset voltage, B is the magnetic field, I is the drain or source current and q is the electron charge. Fig. 3 plots I_s and V_{diff} corresponding to the drain voltage modulation. As the magnetic field increases, the voltage difference between the two flat regions (dV_{diff}) gets larger. Fig. 4 plots dV_{diff}/dI as a function of B field. According to Eq. 2 the inversion sheet charge density n_s can be directly extracted from the slope of Fig. 4. Notice the excellent fit to a straight line, indicating a high level of confidence on the extracted slope and therefore the extracted sheet charge density. This is important because the B field accessible in our set-up is far less than a conventional Hall measurement system. Our signal level is therefore expected to be lower. The drain current modulation approach more than offset the low B field disadvantage of our approach.

$$V_{diff} = V_o + \frac{BI}{qn_s} \quad (1)$$

$$\frac{dV_{diff}}{dI} = \frac{dV_o}{dI} + \frac{B}{qn_s} \quad (2)$$

R_s is measured using Van der Pauw procedures [6]. In Fig. 5, R_s and n_s are plotted as a function of gate voltage. Again, the data are well behaved; give high confidence on the measurement. The Hall mobility can be calculated from $\mu_{Hall}=1/(qn_sR_s)$. Fig. 6 shows the extracted Hall mobility as a function of gate bias. It is almost independent of the gate voltage in the range investigated. This is not the expected behavior of a MOSFET with few defects in the gate dielectric and its interface. However, for SiC-based MOSFET, which has very high oxide trap density, such gate voltage

dependency is surprising. Similar gate bias dependencies of Hall mobility have been reported on SiC devices measured by regular Hall systems [1, 2]. The measured mobility is very small compared to the bulk value. The usual expectations in Si MOSFETs do not apply.

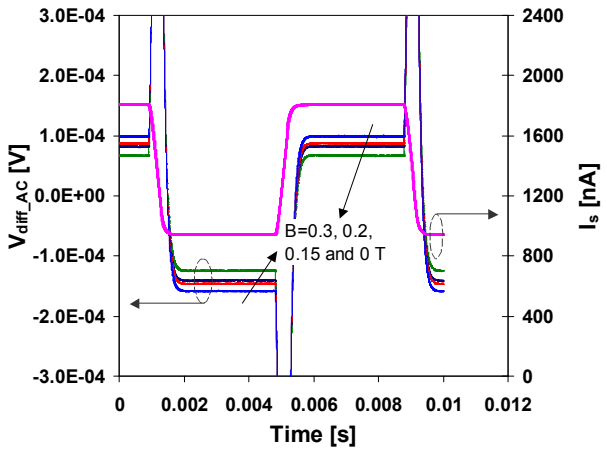

Fig. 3. Source current and differential voltage corresponding to the drain voltage modulation. Four magnetic fields are used. As B increases, dV_{diff} gets larger.

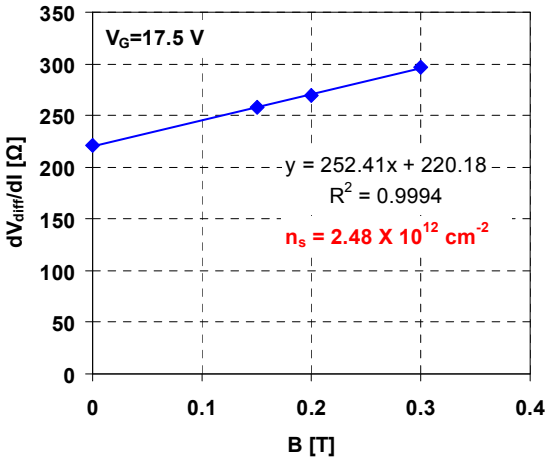

Fig. 4. Inversion sheet charge density (n_s) extraction at V_G=17.5 V.

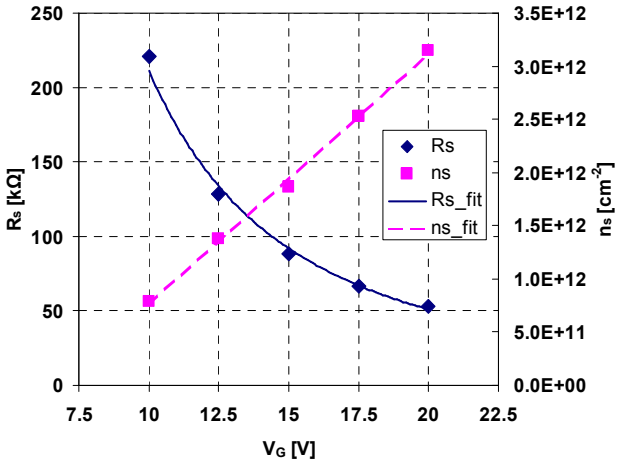

Fig. 5. Sheet resistance and inversion sheet charge density measured at different gate voltages.

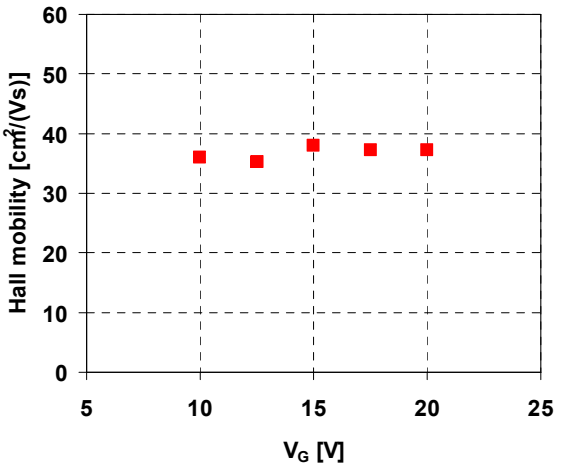

Fig. 6. Hall mobility calculated from R_s and n_s as a function of gate voltage.

Summary

In this work, we have demonstrated a wafer-level Hall mobility measurement method that does not require wafer dicing, wire bonding, packaging nor the regular Hall measurement system. This method makes the device characterization and development more convenient.

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