Compact and Distributed Modeling of Cryogenic Bulk MOSFET Operation

A. Akturk, M. Holloway, S. Potbhare, D. Gundlach, B. Li, N. Goldsman, M. Peckerar, and K. P. Cheung

***Abstract*—We have developed compact and physics-based distributed numerical models for cryogenic bulk MOSFET operation down to 20 K to advance simulation and first-pass design of device and circuit operation at low temperatures. To achieve this, we measured and simulated temperature-dependent current–voltage characteristics of 0.16- and 0.18-μm bulk MOSFETs. Our measurements indicate that these MOSFETs supply approximately 40% more current in the saturation and linear regions of operation when they are cooled from room temperature to 20 K. The threshold voltage monotonically increases as the temperature is lowered, but it saturates below 40 K. The subthreshold slope decreases with the temperature lowering but at a rate that is less than theoretically predicted. The extrapolation of the subthreshold slope indicates a finite value at near absolute zero. We show that the measured behavior can be well corroborated with distributed numerical simulations using the drift–diffusion transport model. In addition, to obtain a compact model for use in low-temperature circuit design, SPICE-type compact models need to be modified to incorporate the subtle temperature effects that are not part of the standard models. To this end, we use the analog behavioral language Verilog-A and the BSIM3 model equation set to include additional temperature dependences into the standard compact models to accurately reproduce measured characteristics.**

***Index Terms*—Cryogenic BSIM, cryogenic compact modeling, cryogenic device modeling, cryogenic MOSFET, Verilog-A.**

I. Introduction

CIRCUIT design for cryogenic electronics is a largely unexplored field. However, applications for cryogenic electronics design are found in various technical areas, including electronics for outer space [1]–[3], as well as electronics that have very low noise requirements such as infrared and far-infrared optical detectors [4]. Furthermore, for any application where the input signal is extremely weak, and a very large signal-to-noise ratio is required, the performance can be enhanced by cryogenic operation [5]. Low-temperature high-performance computing is another field where cryogenic tools and designs are needed to facilitate faster speeds and to avoid thermal runaways [6]. As we are currently "off Moore's law" in terms of system-level performance, a significant improvement in component performance can be achieved by cooling [1]. In addition, if we were to go lower in temperature (down to 20 K and below), we would be in the realm of quantum computing [7], where low-temperature design approaches will prove to be critical.

Developing distributed device simulation capabilities is important for investigating detailed physics of dopant ionization and surface phonon scattering models, as well as the internal operation of MOSFETs [1], [8]–[14]. These simulations can also explain why it is still possible to use MOSFET devices in temperature ranges where carrier freeze-out is a concern [1], [15], [16]. More specifically, standard CMOS electronics operate relatively well at cryogenic temperatures. Both our experimental work and modeling efforts have verified that, for virtually all applications, CMOS electronics operate well at temperatures down to 20 K and even below. Channel mobility of carriers in MOSFETs increases at cryogenic temperatures, which can lead to improved device performance due to higher drive currents [1]. However, threshold voltages increase with decreasing temperatures [1]–[3], [8] as well, and this may render room-temperature low-power electronics inoperable at cryogenic temperatures.

Here, we show methods to calculate current–voltage (I–V) characteristics in the subthreshold, linear, and saturation regions of operation for different bulk MOSFETs. We use these detailed device simulation results to guide the development of compact models in the analog device behavioral language Verilog-A [17]–[19]. The use of device modeling to guide Verilog-A compact model development is necessary because device simulation allows for more physics-based compact models to be developed, and also, it is virtually impossible to gather sufficient experimental data to calibrate compact models for all conditions. Thus, the device models serve as a virtual laboratory that allows for calibration of compact models at the operating conditions where a direct experiment is not available.

SPICE models are imperative for circuit design [20]–[23]. However, BSIM models, which are the standard compact models used for MOSFET-based circuit design, generally do not exist for cryogenic temperatures. We are overcoming this limitation using the circuit/analog behavioral programming language Verilog-A. Here, Verilog-A is used as a device modeling language. It allows for circuit element model revision and creation that is extremely flexible and integrates smoothly into most circuit design SPICE-like computation engines. It is

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therefore our modeling language of choice for implementing new and revised cryogenic device models.

II. Cryogenic Bulk MOSFET Characteristics

We have performed a series of measurements to obtain experimental data for temperature-dependent device characteristics. We used a six-probe Desert Cryogenics system to perform dc measurements on a set of 0.16-μm [24] and 0.18-μm [25] MOSFETs at temperatures ranging from 20 to 300 K. All samples were mounted on a thermal block using a silver thermal compound and annealed for half an hour at 40 °C. The sample was then placed in a Lake Shore Model CPX cryogenic probe station [26]. The system was first pumped down to a vacuum of approximately 2×10^{-7} torr. The probe system was cooled to 4 K using liquid helium, whereas the sample was maintained at room temperature to prevent condensation. The sample was brought down to each measurement temperature at a fixed rate of -8 K/min. The probe station has four dc probe arms with high-precision positioners, which are connected via triaxial cable connections. I–V curves were generated using a 4156B semiconductor parameter analyzer [27]. Each device has four probe terminals, one for each of the following: body, source, drain, and gate. Each probe arm was connected to the four source measurement units of the parameter analyzer with a triaxial cable. I–V measurements were taken at different temperatures. These measurements were then used to calibrate our detailed physics-based device simulator, and eventually, the compact models were implemented in Verilog-A.

For the 0.16-μm N-MOSFET, the measured threshold voltage was found to increase by approximately 0.23 and 0.3 V (using the gate voltage that approximately gives 0.1 μA) above its room-temperature value at 100 and 20 K, respectively. The threshold voltage changes with temperature because of the work function and electron affinities of the polygate and the channel change. The total depletion charge increases by temperature lowering, assuming that band bending rises due to band broadening and the Fermi level approaches dopant energy levels at low temperatures, as well as the channel dopants ionize. Thus, most of the threshold voltage shift is related to a combination of the aforementioned effects used in the standard threshold voltage formula. Furthermore, we observed that the subthreshold slope S decreases as the temperature is lowered, but at a rate slower than that predicted by the standard linear temperature dependence $[S(T) = S(T_o) \times (T/T_o)]$. Specifically, the measured subthreshold slope is calculated to be approximately 78, 26, 14, and 9 mV/dec (millivolts per decade change in current) at 300, 100, 40, and 20 K, respectively. A quadratic extrapolation of these subthreshold slopes to absolute zero gives a value of 5.5 mV/dec. We also observed that, at cryogenic temperatures, the subthreshold slope shows a drain bias dependence, with a sharper slope at the higher drain bias [3]. Additionally, for this N-MOSFET, the saturation current is observed to rise by approximately 40% as the temperature is decreased from 300 to 20 K. This increase is relatively small between 100 and 40 K and negligible between 40 and 20 K. Furthermore, the 0.18-μm N-MOSFET and P-MOSFET show similar temperature dependences. However, the increase in saturation current is limited by approximately 30% and 10% for the N-MOSFET and P-MOSFET, respectively [28]. For all devices at 20 K, we further observed a subtle onset of current rise or kink at high drain biases [29].

In this paper, we focus on the temperature-dependent performance modeling of the 0.16-μm device. The following sections discuss compact and distributed simulations of this device to investigate the effects of low temperature on device and circuit operation.

III. Distributed Physics-Based Numerical Low-Temperature MOSFET Modeling

We developed capabilities for dc device modeling as a function of temperature [1], [13], [14]. The simulator provides the details of how the electron and hole concentrations, the electric potential, and the current densities respond to dc bias at every point inside the device at cryogenic temperatures. This is achieved by self-consistently solving the Poisson equation and the electron and hole current continuity equations.

To achieve agreement between the measured and calculated data, we incorporate temperature dependences of electrical parameters and adjust these temperature dependences as the need arises. To corroborate experimental and simulated I–V curves, we follow the following algorithm: We start with room-temperature simulations using an initial guess for the doping profile, and the known temperature dependences of electrical parameters, as well as layout details such as physical dimensions. We then iterate between Poisson equation and electron and hole current continuity equations until we self-consistently calculate electrostatic potential, electron concentration, and hole concentration profiles. After we achieve convergence for all state variables, we calculate terminal currents and compare them with those measured. In case of a mismatch, we adjust our doping profile. Once we have a room-temperature match between calculated and measured I–V curves, we decrease temperature to start another simulation using the extracted doping profile. (We note that we set the device temperature equal to that of the ambient, as the Joule heating of any measured device is at most a couple of tens of milliwatts, and the thermal resistance of unpackaged chips fabricated in bulk technologies is low [13].) The device simulator we developed already has built-in temperature dependences of carrier mobilities, potentials, intrinsic carrier concentration, etc. We again iterate between the aforementioned Poisson equation and the transport equations to converge on a solution. If our calculated drain and source currents disagree with measured data, we revisit temperature dependences of electrical parameters, particularly those used in mobility modeling. We applied this algorithm to a 0.16-μm-long and 15.6-μm-wide N-MOSFET and obtained room- and low-temperature fits to experimental data in saturation, linear, and subthreshold regions of operations, as shown in Figs. 1 and 2. We note that there is some disagreement in the subthreshold region. We attribute that to additional interface traps that are exposed at the channel–insulator interface at low temperatures. In our device simulations, we do not calculate these additional trap densities as they minimally affect the linear and saturation regions of operation. Here, our goal is to show that

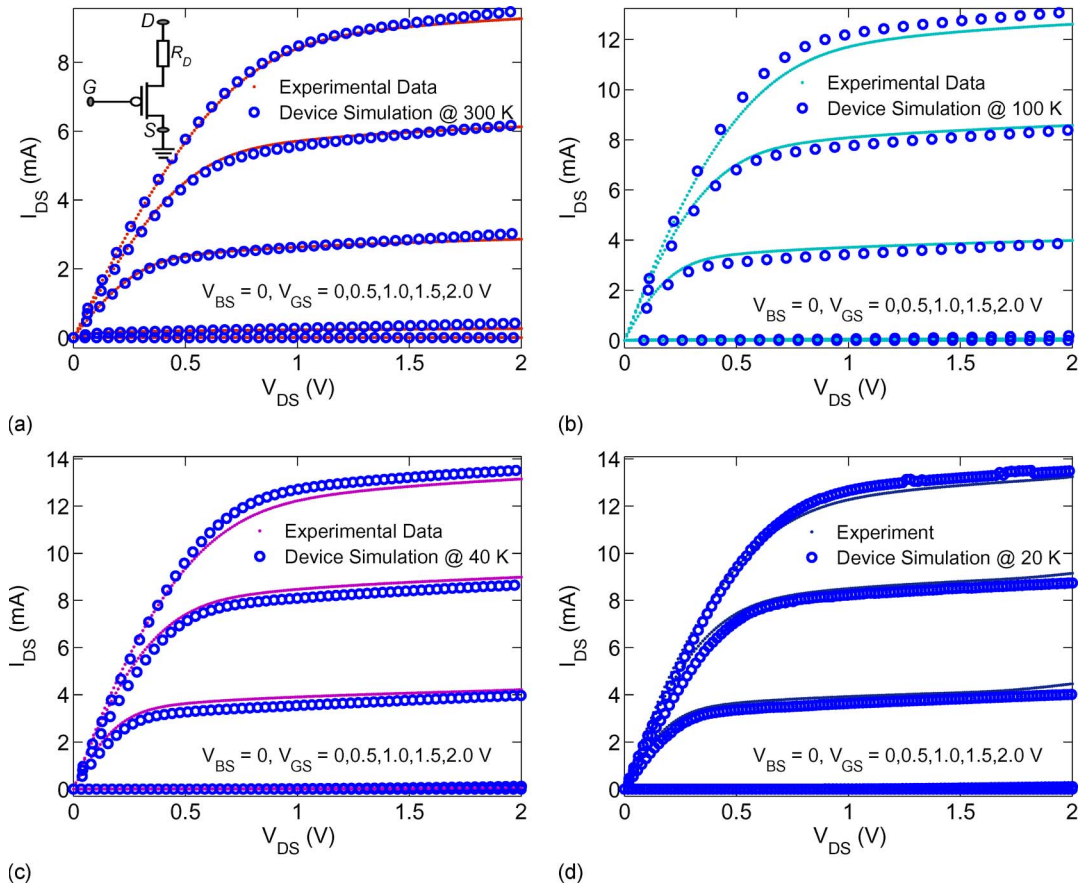

Fig. 1. Temperature-dependent measured and simulated drain-to-source current versus drain-to-source voltage curves of an N-MOSFET with $W/L = 15.6\ \mu\text{m}/0.16\ \mu\text{m}$. Simulation results are obtained using distributed numerical modeling at the indicated temperatures. In addition, a parasitic drain resistance that is 15 Ω at room temperature and decreases with temperature is included in the simulations.

low-temperature I–V characteristics can be predicted using a distributed device simulation. The calculated and measured curves at different temperatures reasonably match well and give us insights about the internal operation of the MOSFET at different temperatures.

The temperature dependences of the intrinsic carrier concentration, thermal voltage, built-in potential, saturation velocity, and other electrical parameters, as well as the incomplete dopant ionization equations, are the same as those stated in [1]. In addition, the lattice temperature anywhere in the device is set to the ambient temperature. Furthermore, at extreme low temperatures, many electrical parameters such as the intrinsic carrier concentration take on extreme small or large values. This creates many numerical problems, which we developed methods to overcome. These methods include scaling, matrix pivoting, and out-of-range value avoidance in double format.

In addition to the aforementioned variables, the temperature-dependent band gap is given as follows:

$$E_g(T) = E_g(0) - 3.18 \times 10^{-4} \times \theta \times \left(\sqrt[p]{1 + \left(\frac{T}{\theta} \right)^p} - 1 \right) \quad (1)$$

where $p = 2.33$, and the temperature $\theta = 203$ K, which is half of the average phonon temperature [30]. The calculated silicon band gaps are 1.12 and 1.17 eV at room temperature and 20 K, respectively.

The bulk mobility only has an implicit temperature dependence via the total ionized dopant concentration [1], [31]. The sole mobility parameter that is adjusted beyond its standard form to obtain matches with experiments is the α in the acoustic phonon scattering term, i.e.,

$$\mu_{\text{ac}}(T) = \frac{1 + [\beta/T] E_\perp^{2/3}}{\alpha(T) E_\perp}. \quad (2)$$

Here, E is the electric field in the direction normal to the insulator–channel interface, and α is a term related to the thickness of the inversion layer, which is usually taken as constant around room temperature. The device simulations that provide best matches to experimental data indicate that alpha takes on values $\times 0.7$, $\times 1.2$, and $\times 2.0$ to that of its room-temperature value at 100, 40, and 20 K, respectively. Furthermore, we have a parasitic drain resistance that is 15 Ω at room temperature and has a temperature coefficient of 0.025 Ω/K (or 1.7×10^{-3} K^{-1}). Our device simulations also indicate that the channel doping is approximately 3×10^{17} cm^{-3}, and the peak source/drain doping is 1×10^{19} cm^{-3}.

Our numerical simulations indicated that all the observed device characteristics can be self-consistently explained. Our investigations showed that carrier freeze-out was not detrimental for MOSFET direct-current operation. We also observed that the dc transconductance and the threshold voltage rose several

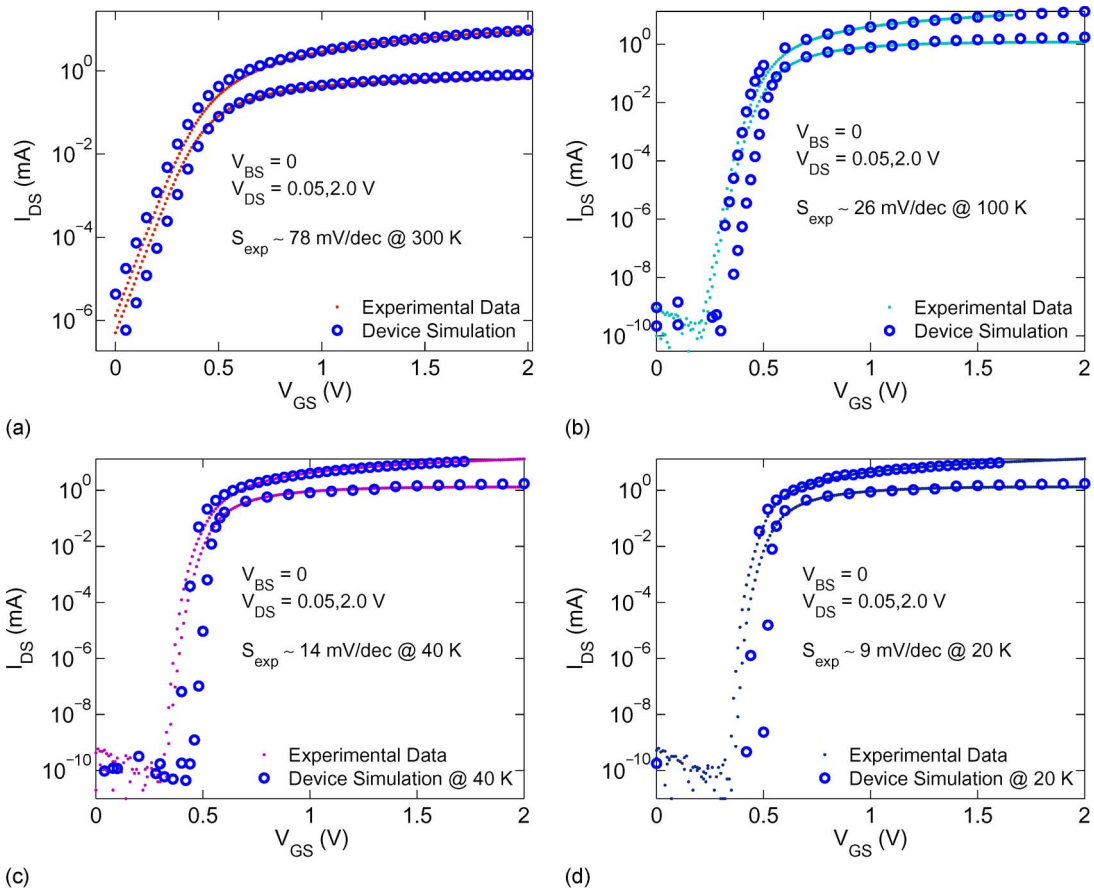

Fig. 2. Temperature-dependent measured and simulated drain-to-source current versus gate-to-source voltage curves of the N-MOSFET with $W/L = 15.6\ \mu\text{m}/0.16\ \mu\text{m}$ shown in Fig. 1. Simulation results are obtained using distributed numerical modeling at the indicated temperatures.

percent as the temperature decreased within the aforementioned range. Our modeling showed the following: 1) that any effects of freeze-out are mitigated by impurity band formation in the source/drain and field-assisted ionization in the device channel; 2) that larger mobilities are achieved at low temperatures due to suppressed phonon-limited scattering; and 3) that cutoff frequencies of devices and circuits operated in the saturation and linear regions of operation are expected to increase with decreasing temperatures.

Once we obtained the physical details of device parameters and the temperature dependences of electrical parameters, we started working on a compact N-MOSFET model. We imported as much as possible from device simulations into the compact model to corroborate our calculated results with experiments.

IV. Cryogenic MOSFET Compact Modeling Using Verilog-A

Modern submicrometer circuits are very complex and require meeting very stringent criteria for their design. Circuit design is generally carried out using an array of computer-aided design (CAD) tools, of which the circuit simulator SPICE plays a most fundamental role. However, the critical problem is that SPICE is not applicable to the low-temperature environments since it is developed to model device operation near room temperature. Therefore, SPICE must be modified, and SPICE-type simulators must be developed to meet low-temperature circuit design requirements. More specifically, SPICE-type models need to be created for all operating points and for virtually all temperatures to achieve reliable circuit design. These models can be calibrated using experiments and device simulations to cover the complete operating temperature range. Once comprehensive calibrated SPICE models and cryogenic simulators are developed, reliable circuits can be designed and fabricated. We implement the new models using Verilog-A, which, unlike existing simulators, will allow for modification of circuit design equations for cryogenic conditions.

Modern circuit simulation is achieved using the standard compact modeling BSIM equations [20]. The equations can be solved efficiently by many commercial simulators. However, BSIM simulation results can be adjusted only by changing device model parameters. (The user is not allowed to access BSIM equations, which are hard coded in the commercial simulators.) In addition, BSIM has been developed for modeling MOSFETs operating approximately in the 250–450 K temperature range. BSIM I–V curves deviate from measurements at extreme low temperatures. Furthermore, we note that other compact models can also be used to simulate device behavior at cryogenic temperatures. For example, the EKV MOST model has been known to have some cryogenic temperature modeling capabilities. However, BSIM3 is the choice of compact model for this work [32].

Here, our goal is to obtain a BSIM-type model and parameter set that is applicable for all temperatures and integrates

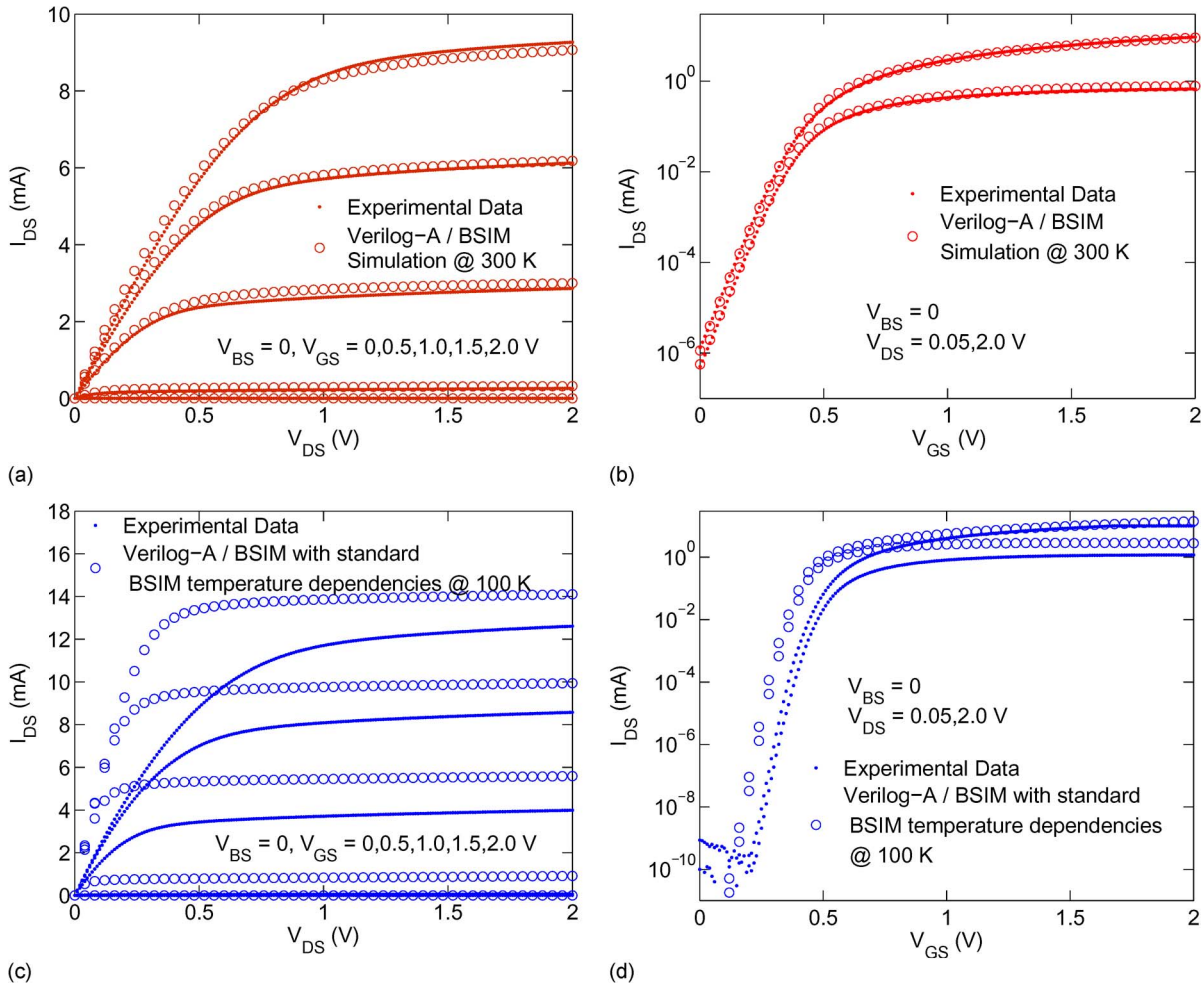

Fig. 3. (a) and (b) Room-temperature measured and simulated drain-to-source current versus gate-to-source and drain-to-source voltage curves of the N-MOSFET with $W/L = 15.6\ \mu\text{m}/0.16\ \mu\text{m}$. Simulation results are obtained using compact Verilog-A/BSIM modeling in Cadence's Spectre. (c) and (d) We lowered the simulator temperature to 100 K and obtained the shown I–V curves. This comparison to measured data reflects the inadequacies of the temperature dependences of the BSIM model set at low temperatures for describing the device performance.

smoothly into existing compact modeling tools. We developed a foundation for overcoming the limitations associated with BSIM to efficiently develop compact models that can be evaluated by commercial simulators. We achieved this with the use of the analog behavioral modeling language Verilog-A. In contrast to standard simulation tools such as Cadence, which are inflexible when it comes to revising the model equations in BSIM, Verilog-A modeling equations can be modified and then evaluated using commercial solvers.

Verilog-A is an industry-standard compact device simulation modeling language that can easily be coupled and compiled with compact circuit simulators such as HSPICE or Cadence's Spectre simulator [33]. Verilog-A enables us to model cryogenic temperature nonstandard MOSFET behavior that cannot be described using, for example, BSIM3 or BSIM4.

We first developed the capability to import the BSIM3 models into Verilog-A [34]. We then input this Verilog-A program into the IC design system Cadence for numerical evaluation. Now that the BSIM model equations are reexpressed in the Verilog-A environment, we can modify them where necessary to be applicable to cryogenic conditions. With this capability achieved, we have developed a preliminary set of compact models for MOSFET circuit design at cryogenic temperatures. More specifically, we have modified compact BSIM models that we imported into Verilog-A to be temperature dependent and reflect operation at cryogenic temperatures. This is achieved by modifying the temperature dependence of key terms in the BSIM equations, which are now accessible through Verilog-A. By using our simulations and measurements as a guide, we have achieved agreement for the temperature dependence of MOSFET I–V characteristics, which were not achieved using the standard BSIM. Additionally, our resulting changes to the BSIM equation set do not lead to convergence problems or noticeably longer calculation times in the circuit simulator.

Fig. 3(a) and (b) shows our measured and simulated I–V characteristics at room temperature. For the compact model simulations, we used Cadence's Spectre simulator [33]. We extracted a parameter list for the BSIM equation set at room temperature using the details deduced from device simulations and the empirical methods. We then changed the device temperature to 100 K and simulated I–V characteristics at this temperature using the 300 K parameter list. The simulator used the built-in temperature dependences of the BSIM3 model to obtain projections to 100 K. As shown in Fig. 3(c) and (d), the

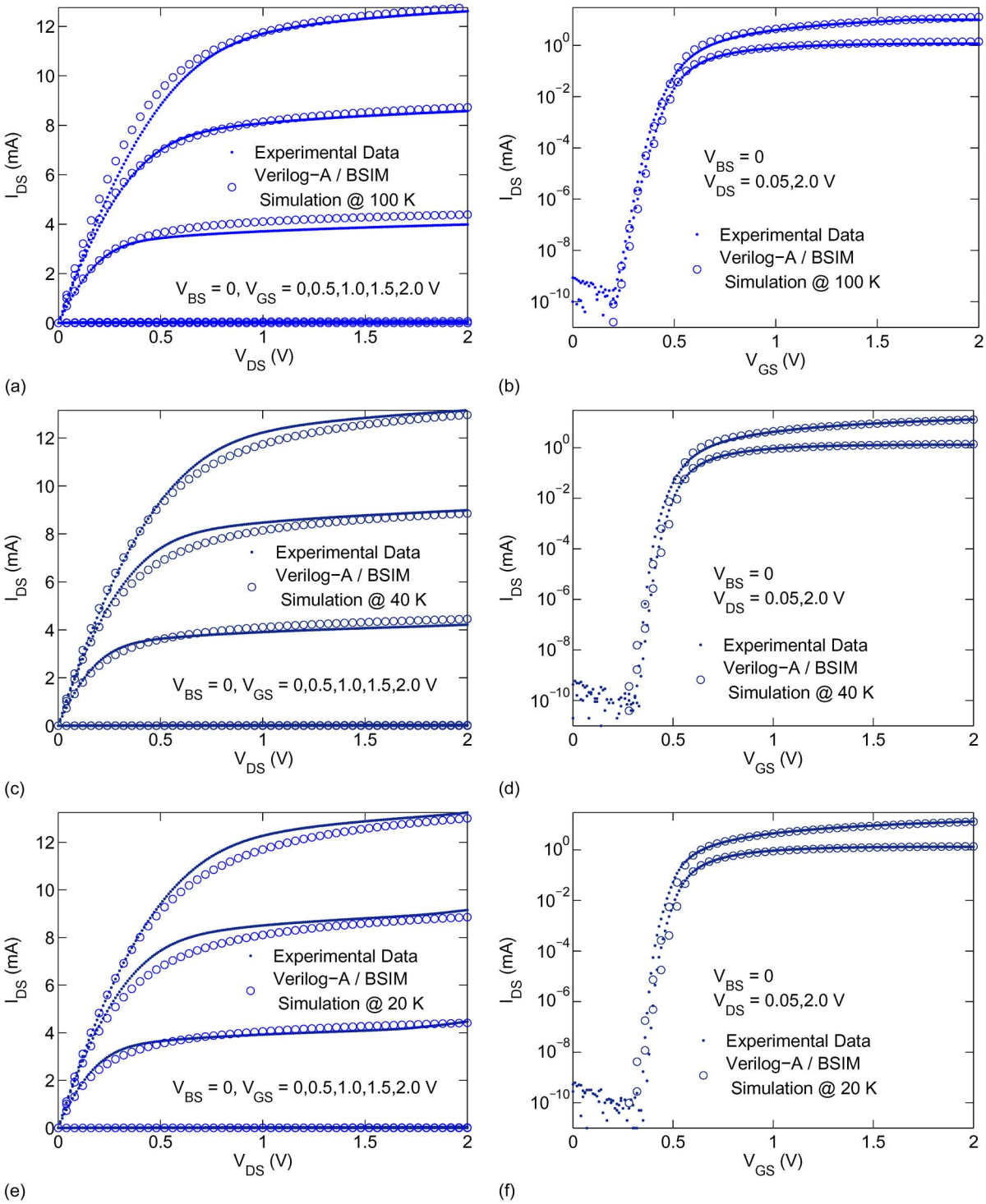

Fig. 4. Temperature-dependent measured and simulated drain-to-source current versus gate-to-source and drain-to-source voltage curves of the N-MOSFET with $W/L = 15.6\ \mu\text{m}/0.16\ \mu\text{m}$. Simulation results are obtained using compact Verilog-A/BSIM modeling in Cadence's Spectre. Unlike the model used in Fig. 3(c) and (d), here, we included additional temperature dependences into the Verilog-A/BSIM model for accurately describing the device performance.

calculated currents are higher than the measured currents by approximately 50%, 100%, and couple decades in the saturation, linear, and subthreshold regions of operation. This would lead to large errors in circuit and system simulations at cold temperatures if the designer solely relies on the temperature dependences incorporated into the BSIM model set. Furthermore, another method to incorporate temperature effects is to extract different BSIM parameter lists at different temperatures, if possible. However, such a solution is impractical in terms of design, time, and effort, particularly when one needs to simulate circuits at various temperatures or to include the effects of chip self-heating on the device performance.

Verilog-A has been used to modify the BSIM model, and an agreement with experiments has been achieved, as shown in Fig. 4. To obtain fits to experimental data at low temperatures, we incorporated additional temperature dependences into the

Verilog-A/BSIM model that is guided by device simulations and experiments. Experimental curves corroborated with simulations only after a temperature-dependent mobility model, a temperature-dependent threshold model, and a temperature-dependent model for the nonideality factor of the subthreshold current were incorporated into the model.

In the new model, the additional temperature dependences of the threshold voltage VTH0, bulk mobility U0, and linear-to-saturation region smoothness parameter (used in the calculation of the effective drain-to-source voltage) DELTA are as follows [20]:

$$\text{VTH0} = 0.12 + (300 - \$\text{temperature}) \times 4e - 4$$

$$\text{U0} = 120.2784/\left(1 + (300 - \$\text{temperature})/50\right)$$

$$\text{DELTA} = 0.012 + (300 - \$\text{temperature}) \times 4e - 4$$

where \$temperature represents the global simulator temperature (in kelvins). Furthermore, the parasitic source-drain resistance has a temperature dependence similar to that used in device simulations. In addition to these additional temperature dependences included into the parameter list, we also changed the equation for the ideality factor n, which affects the subthreshold slope. While the correction is approximately constant between room temperature and 100 K, it is taken as a function of temperature below 100 K. More specifically, $n = \text{no} \times f(T)$, where no is the n calculated using the standard model, and $f(T) = a \times T^b$, with $a = 90.68$, $b = -0.9683$, and $T =$ \$temperature. We also note that a different set of additional temperature dependences may be included to obtain fits to experiments, but for our device, the aforementioned inclusions result in minimal changes with much more accurate fits than those calculated using the standard model. In addition, the Verilog-A/BSIM model allows us to use one parameter list for all temperature points, enabling the seamless and automated design of low-temperature circuits. Fig. 4 demonstrates that the compact model successfully revised to account for cryogenic applications. The model with one parameter list shows agreement with experimental I–V curves at 300, 100, 40, and 20 K.

V. Conclusion

MOS-based architectures usually work better at low temperatures. For the 0.16-μm N-MOSFET, the drive current (saturation current for the largest gate bias: 2.0 V, measured at room temperature and $<$ 40 K) increases by 40%, and there is a concomitant decrease in subthreshold slope (although that slope does not linearly scale with temperature, as first-order theory predicts), as the temperature decreases. The threshold voltage increases with the reduction in temperature down to 40 K and then saturates.

We developed distributed physics-based numerical models to quantify the improvement in MOSFET performance at cryogenic temperatures. We then used device simulations and measurements to develop compact Verilog-A and BSIM-based models for cryogenic MOSFET operation. This paper has clearly demonstrated that the existing framework of compact models of MOSFET parameters can be extended into the cryogenic region of operation down to 20 K.

The standard BSIM model appears to lack the ability to accurately predict the low-temperature operation in all regions of operation. However, the disclosed methodology, modifying these existing compact scripts using a Verilog-A approach, enables achieving current fits in a wide range of temperatures for all regions of operation. This also enables us to utilize existing infrastructure for SPICE-based circuit design and the commercial CAD base for physical layout. These accurate models are essential for the achievement of first-pass cryogenic design success.

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