Micromachined Branch Line Coupler in CMOS Technology

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Abstract—An internally ground-equalized coplanar branch line coupler (BLC) is fabricated by post-processing 2poly/2metal analog CMOS chips. First level metallization is used to equalize the ground planes, hence to suppress the unwanted coupled-slot-line mode propagation. This addition necessitates additional compensation of signal lines to improve the return losses.

Fabricated CMOS chips are post-processed with a two-step procedure. First, a thick polyimide film is screen-printed on the devices as a stress-compensation. Then, the silicon substrate is selectively removed underneath the devices. The measured responses show very good agreement with simulations. Fabricated devices exhibit return losses less than 10 dB and maximum of 1 dB amplitude difference in the frequency range of 25-30 GHz.

I. INTRODUCTION

It has been shown that the unwanted coupled slotline mode (CSL) excited by asymmetrical discontinuities drastically affects the coplanar waveguide (CPW) circuit performance [1]-[3]. To minimize CPW-to-CSL conversion either equalization by wirebonds or air-bridges have been used [1], [4],[5].

In many cases, even small process variations of the equalization structure can result in significant changes in the response of a device. Therefore, it is necessary to have highly accurate and reproducible fabrication techniques. The air-bridge technology satisfies these requirements, and thus is usually favored over equalization by wirebonding in high performance applications.

In this work, we explored a third option by using a metal interconnect layer for this purpose. This alternative is usually dismissed in MMIC designs, since metal interconnect layers are separated by very thin layers of insulating films. This changes the local propagation properties drastically. Similar concerns, though less severe, have led to several studies on the effects of air-bridges on the wave propagation [3]. In the presented work, ground equalizations are realized with a metal layer separated from coupler by 0.75 μm thick SiO_2 layer. Step compensations are employed to improve return loss [4].

The technique is demonstrated in the design of a branch line coupler (BLC). These couplers are widely used in microwave application such as balanced mixers, amplifiers, PIN switches, detectors, and patch antennas [6].

II. DESIGN

A. System Design

The micromachined BLC is designed by using the conventional approach. It consists of two branches with characteristic impedance of Z_0 (assuming the port impedances are Z_0) and the remaining two branches with $Z_0/\sqrt{2}$. All of the four branches are quarter wavelength long at the center frequency of operation. In order to

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minimize the area of the BLC, the branches are laid out with L shaped configuration as seen in Fig. 1. This allows a more efficient use of the silicon area.

The micromachined devices have an effective dielectric constant of 3.8. This is mainly determined by the choice of the stress-compensation layer discussed in the fabrication section.

50 Ω BLC system requires coplanar transmission lines (CTLs) with characteristic impedances of 50 Ω and 35.4 Ω. The dimensions for these impedances are calculated by using the thickness-corrected quasi-TEM formulation given in [7]. To minimize the conductor losses at high frequencies, the thicker aluminum interconnect layer is preferred to realize the CTLs. The fourth port is terminated by using an on-chip polysilicon resistor.

B. Internal Ground Equalization

In this work, 1st level of metallization (Metal1) is used to realize the underpasses for ground equalization. Since this does not require any additional processing it is termed as internal ground equalization.

Metal1 is separated from 2nd level of metallization (Metal2) with a 0.75 μm thick silicon dioxide dielectric layer (ε_r~4.0). This results in extremely high capacitive loading wherever an underpass is used to equalize two Metal2 ground planes. Without a proper compensation, internal ground equalizers would cause considerable change in device performance. To minimize such changes, and improve the return loss, the width of the signal line is adjusted near the underpasses.

The accurate modeling of the compensated ground-equalizations (see Fig. 2) is necessary especially at frequencies above 10 GHz. We assume that this considered section can be modeled by a shunt capacitance C_{ge}. The analytical calculation of this capacitance is very difficult. Particularly, the strip thicknesses become important, when a standard CMOS fabrication process is used. Therefore, even the powerful 2½D field solvers underestimate the value of C_{ge}. The 3D quasi-static analysis of the structure reveals that there are four major contributions to the shunt capacitance as illustrated in Fig. 3. The T-junctions (see Fig. 4) are simulated by extensively by using 2½D and 3D simulation packages. As shown in Fig. 5, the results deviate at frequencies above 10 GHz.

The overall response of the BLC is obtained only after the T-junction, L-shaped quarter wavelength long 50 Ω and 35.4 Ω CTLs are simulated separately by a 2½D em package.

III. FABRICATION

Since the CMOS substrate is highly doped, it becomes extremely lossy at high frequencies. Therefore, it has to be removed selectively to isolate high-frequency devices from the substrate. Whenever it is removed the suspended membrane buckles with the present internal stress [8]. There are several different combinations of thin films that are extremely fragile. When released they mechanically fail. Especially, the membrane between signal and ground in any coplanar device is susceptible to these kind of mechanical failures. To avoid these kind of mechanical failures, it is desired to put the membranes under tensile stress.

A 100 μm thick polyimide film (EPO-TEK 600 by Epoxy Technologies) is deposited on the area that will be suspended by using a steel stencil. Each coating is prebaked one hour at 150 C and followed by final bake at 225 C for 30 minutes. This gives dielectric constant of 6.6.

After stress compensation, the backside of the chip is patterned photolithographically to expose the silicon substrate only underneath the devices that will be suspended. Finally, the silicon is removed by using highly-selective isotropic silicon etchant xenon difluorite (XeF_2). It takes 54 pulses of 2 Torr-XeF_2 to suspend the BLC [8].

IV. MEASUREMENTS

Frequency response of the BLC is measured with HP 8510C Network Analyzer. SOLT (Short-Open-Line-Thru) probe-tip calibration is performed using calibration substrate in 0.1-50GHz frequency range.

After the 3rd port of the device is terminated with a 50 Ω load by means of three wirebonds, the two-port measurements are performed. The measurement data of the resulting two port device is shown in Fig. 6. In the displayed simulations, measured response of the load for terminated ports used but the wirebonds are not included for the 3rd port. This caused considerable deviation from the expected values.

V. DISCUSSION

Internal ground equalization by using an interconnect layer is shown to be a feasible alternative to equalization by wire bonding and air-bridge. It is cheaper than air-bridge, more repeatable than bonding. According to em simulations compensated T-junctions contribute less than 0.3 dB to insertion loss at 27.5 GHz. However, measurements show that at the center frequency, the coupling to the output ports is almost 1.5 dB less than desired 3 dB. The conductor loss for 50 Ω CTLs is characterized with independent experiments. Accordingly, a quarter wavelength long 50 Ω CTL has 0.37 dB loss at 27.5 GHz. Dielectric, radiation and acoustic losses are neglected in this work. The most significant contribution to the overall loss comes from the corner on the first port. The compensation employed in this corner by narrowing the signal line (see Fig. 1) increased the return loss. This is clearly visible in Fig. 6. In future designs this corner will be avoided altogether. The micromachined BLC has better than 10 dB return loss and isolation between the output ports and ±1 dB amplitude difference over the frequency range from 25 GHz to 30 GHz.

VI. CONCLUSION

25-30 GHz internally ground equalized micromachined branch line coupler is designed and fabricated by using 1.2 μm CMOS technology. Coupled slot-line mode propagation that is excited at T-junctions is suppressed by using first level metal underpasses, which are separated by 0.75 μm SiO_2 from the 2nd level metal. Capacitive loading due to these ground equalizers is mitigated by using step compensation and high impedance CTL sections.

VII. REFERENCES

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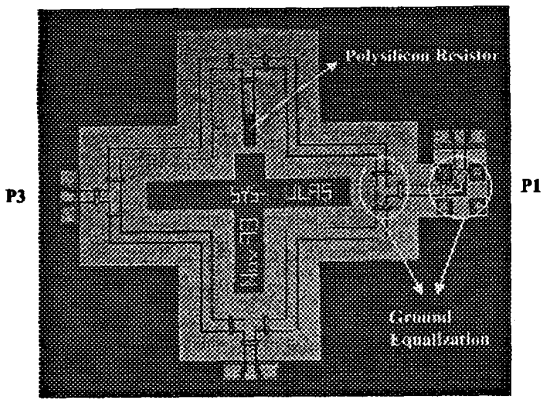

Figure 1: Microphotograph of the micromachined Ka-band branch line coupler.

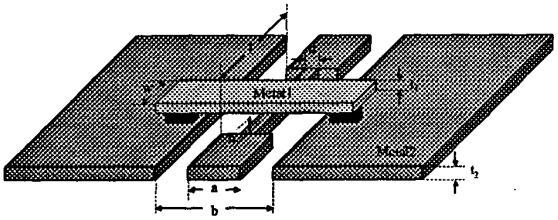

Figure 2: Illustration of a compensated ground equalization section used in BLC. The bridge-like structure is 1st metal layer (Metal1). The discontinuities in the signal are symmetric with respect to Metal1. Coplanar transmission is symmetric and realized by using 2nd metal layer (Metal2).

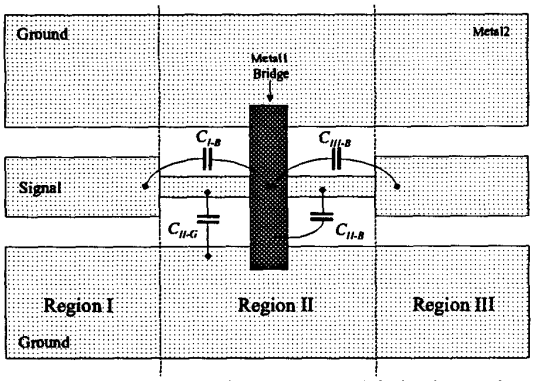

Figure 3: Ground equalizers are modeled with a shunt lumped capacitance C_{ge}. Although, this quasi-static capacitance is dominated by C_{II-B} in many cases, if l is $<2w$ then the contributions from C_{I-B} and C_{III-B} are substantial. If $l>3w$, on the other hand, then C_{II-G} should be considered as well.

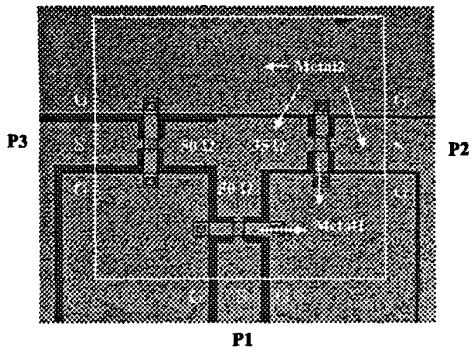

Figure 4: One of the T-junctions showing compensated 2nd level metallization and ground equalizers realized by 1st level metallization.

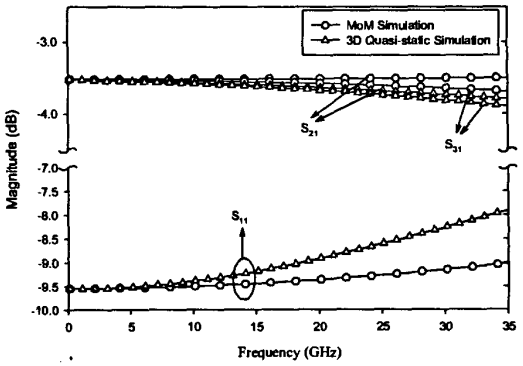

Figure 5: The T-junctions with (l,d)=(35,10) for 50 Ω and (35,20) for 35 Ω are simulated by using the capacitances from a 3D quasi-static field solver. If these results are compared with 2½D simulation (with zero-thickness strips) results, significant difference at frequencies above 10 GHz is observed.

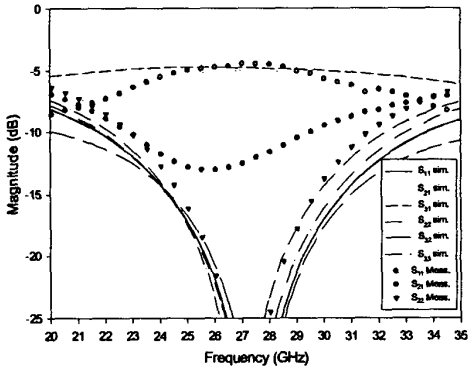

Figure 6: Simulated response of micromachined BLC with measured on-chip 50 Ω termination.