Micromachined 28-GHz Power Divider in CMOS Technology

Mehmet Ozgur, Mona E. Zaghloul, and Michael Gaitan

***Abstract*—A broad-band power divider is presented in CMOS technology. The devices are realized by postprocessing chips that are fabricated in a standard 1.2-μm CMOS process. Developed postprocessing includes wire bonding for ground equalization, deposition of a stress-compensation layer, and selective etching of the silicon substrate. By employing coupled coplanar transmission lines, the area of dividers is minimized to 0.8 mm $\times$ 2.1 mm. A 20–35-GHz power divider exhibits a coupling of -3.8 dB $\pm$ 0.6 dB.**

***Index Terms*—CMOS micromachining, coupled coplanar transmission lines, power divider.**

I. INTRODUCTION

COST-EFFECTIVE fabrication of radio-frequency (RF) components and their integration with analog and digital electronic circuits have become important issues recently with the single-chip communications efforts [1]. In many cases, microwave active circuits, passive microwave components, and low-frequency electronic circuits are fabricated in different processes and integrated afterwards by using a chip scale integration technology [2].

Micromachining CMOS circuits is a promising way to realize high-performance RF components that are inherently integrated with low-frequency active circuits. Previously, low-lost coplanar waveguides were demonstrated without using any stress-compensation [3]. However, the internal mechanical stresses in CMOS layers have prevented fabrication of large suspended membranes necessary for RF components, such as Wilkinson dividers. This limitation has been overcome recently by the addition of a stress compensation layer on the suspended membrane area [4], [5]. Here, this new technique is further improved to realize large RF components in CMOS technology.

In this paper, a high-performance low-cost power divider is presented. This component is important for many applications including: high-power amplifiers [6], signal distribution networks [7], and signal detection circuits [1], [8]. The presented divider structure is very compact (0.8 $\times$ 2.1 mm) and exhibits a coupling of -3.8 ± 0.6 dB over the frequency range from 15 to 35 GHz. In the same frequency range its predicted isolation is better than 10 dB.

Manuscript received November 10, 1999; revised January 27, 2000. This work was supported in part by the Institute of MEMS and VLSI Technology at GWU, Washington, DC, and the Space and Naval Warfare Systems Center (SPAWAR), San Diego, CA.

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Publisher Item Identifier S 1051-8207(00)03346-8.

II. DESIGN

To minimize the area of the power divider, coupled coplanar transmission lines are used to realize quarter wavelength long sections [9]. In this approach for 50-Ω output ports, the desired even mode impedance (Z_e) and the isolation resistor are 71 and 100 Ω, respectively. The isolation resistor is realized by using second-level polysilicon of the CMOS process, which has an average sheet resistance of 23.3 Ω/sq. (see Fig. 1).

The even-to-odd mode impedance ratio of 1.6, $r = Z_e/Z_o$, which determines the bandwidth of operation, is chosen. Then, the cross-sectional dimensions of the coupled coplanar transmission lines as illustrated in Fig. 2, are calculated by using the analytical formulation given in [10]. By taking into account the 1.2-μm CMOS design rules, the dimensions $(a, b, c, d) = (50, 150, 170, 500)$ μm that yield the mode impedances of $(Z_e, Z_o) = (72.2\ \Omega, 44.1\ \Omega)$ are chosen. To minimize the conductor losses only second-level metallization is used in the design.

Simulation of the final structure is performed with Sonnet Em Suite [11]. The resistor is modeled as an ideal high-resistive region with ideal contacts. The bond wires that are used for ground equalization are also included in the simulations as 50-μm-high 25-μm-wide metal strips.

III. FABRICATION

The devices are fabricated in a commercial 1.2-μm 2poly/2metal CMOS process through MOSIS [12]. The CMOS-fabricated devices are ground equalized by using bond wires. Then, the area that will be suspended is stress compensated by using a single-component screen-printable polyimide Epotek 600 (Epoxy Technologies). Curing is done in two steps. It starts with a prebake at 150 °C for 1 h and follows with a final cure at 275 °C for 30 min. This creates a fairly uniform, low-stress, and low-k ($\varepsilon_1 = 2.4$) dielectric film. The thickness of this layer is controlled by the thickness of the stencil, but the minimum value that can be achieved is dictated by loop heights of the wire bonds. Therefore, loop heights are kept to the smallest value possible. Nonetheless, several different chips were fabricated, each having a different number of coatings. Each coating adds approximately 100-μm-thick film of polyimide. The results reported in this work are from the chips with five layers of coating. Afterwards, the backside of the chip is patterned photolithographically to expose the

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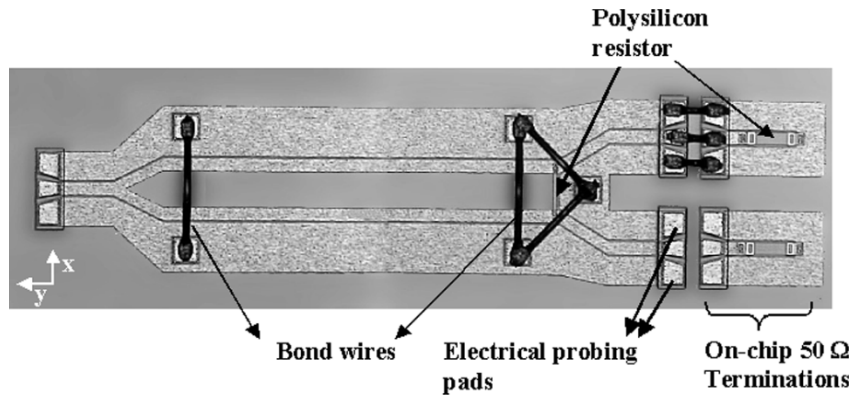

Fig. 1. Micrograph of one of the power dividers before postprocessing. Bond wires are used for ground equalization and terminating the output ports.

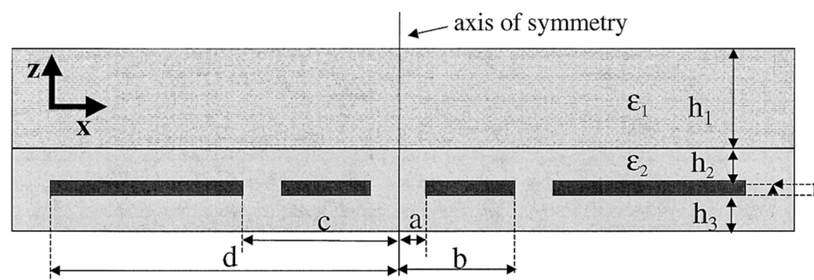

Fig. 2. Cross-sectional view of the coupled coplanar section along x-axis. Stress compensation layer and SiO_2 are shown with the dielectrics ε_1 and ε_2, respectively.

silicon only under the area that will be suspended. Finally, the exposed silicon is etched by using XeF_2 [4]. Fig. 3 illustrates a cross-sectional view of a postprocessed CMOS chip.

IV. Results

All of the measurements are performed from the backside of the chips by using 50-GHz HP 8510C Network Analyzer. SOLT (short-open-load-thru) calibration method is employed in the probe tip measurements. During fabrication of the samples, one of the output ports of each power divider is terminated with a 50-Ω load by using bond wires. These termination loads are designed immediately adjacent to the output ports by using second-level polysilicon. As a result, all the dividers are measured as two-port devices. Excellent divider characteristics are observed in the frequency band of interest (20–35 GHz). The results shown in Fig. 4 exhibit good agreement with the simulation results. The differences between measurement and simulation are due to inaccuracies in bond-wire, dielectric and conductor modeling, assumption of zero-thickness metallization, and, most importantly, due to probing difficulties in microwave measurements. CMOS pads are covered with a thin layer of aluminum oxide that prevents high quality electrical contacts.

Isolation between output ports cannot be measured in the available test chips, since a termination resistor at the input port was not included in the design. Bonding to an existing on-chip 50-Ω termination is not possible because of the excessive distance to the nearest termination. Therefore, as shown in Fig. 4, we report only the simulation results for isolation. It is higher

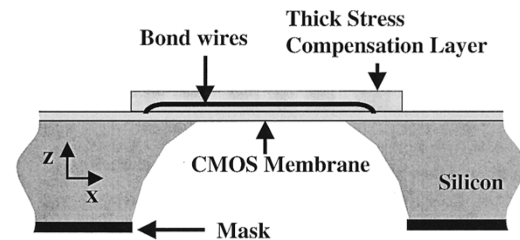

Fig. 3. Cross-sectional view of the postprocessed CMOS chip with enclosed bond wires and thick stress-compensation layer along x-axis.

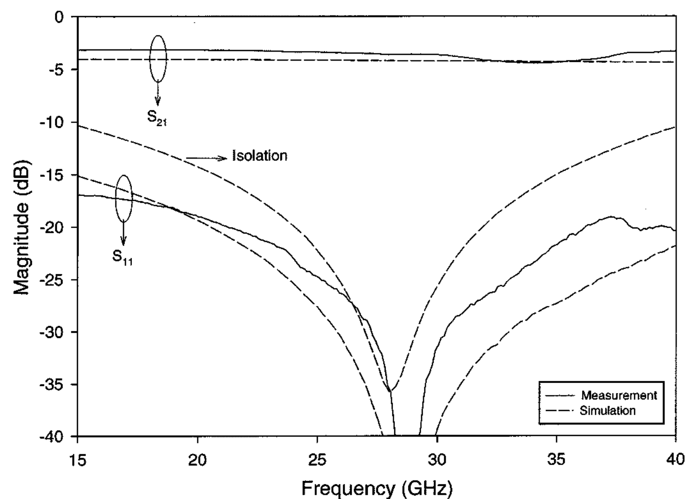

Fig. 4. Measured and simulated responses of the power divider.

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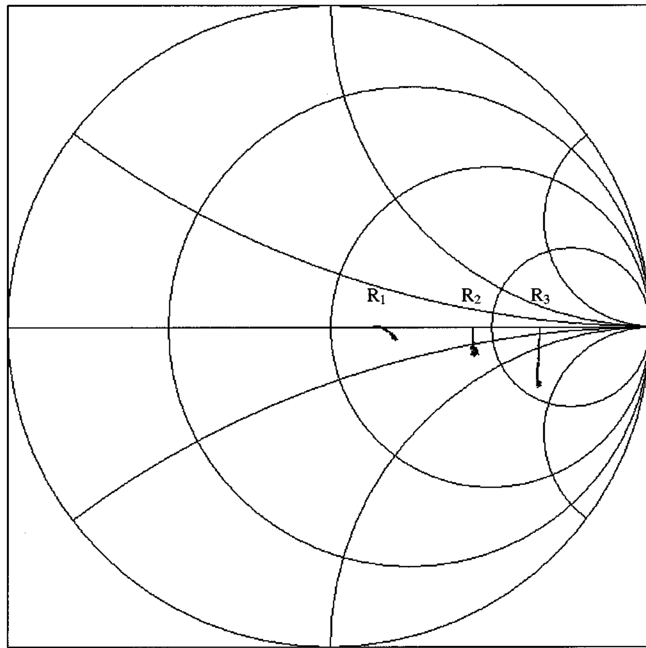

Fig. 5. Frequency dependencies of three polysilicon test resistors R_1, R_2, and R_3 are measured up to 50 GHz. All three resistors are fabricated by using second-level polysilicon layer and have resistances of 63.6, 118.3, and 236.1 Ω, respectively, at dc.

than initial estimations due to variations in the sheet resistance of polysilicon.

One of the difficulties with the fabrication of power dividers in CMOS technology is that the isolation resistor can only be realized by using polysilicon available in CMOS processes. The process-dependent variation in sheet resistance can be as large as 10% from the mean value. In this work, all polysilicon resistors are realized by using second-level polysilicon layer. In the run from which the data in Fig. 5 is taken, the sheet resistance was 10% higher than average. This translates into a 10% increase in all resistors. The terminations, which are designed as 48 Ω, are fabricated as 52.1 Ω. Similarly, the isolation resistor turned out to be 113 Ω with the contact resistances. In electromagnetic simulations, this resistor is modeled with the measured value of the sheet resistance. The result of the electromagnetic simulation, which includes coupled lines and isolation resistor, is used together with the wire-bond model and the measured response of on-chip terminations to obtain the results shown in Fig. 4. Simulations with various sheet resistance values indicate that the performance of the divider is not very sensitive to the process variations. The change in S_{21} and S_{31} due to these variations is estimated to be less than 0.1 dB. The change in return losses can be as large as 3 dB only around the center frequency, but the overall change can be neglected, because the return losses remain to be more than 40 dB.

Beside the process variations, resistor geometry is important at high frequencies, as well. Parasitic effects are minimized in 50-Ω terminations by using the same width as for 50-Ω transmission lines. On the other hand, the width of the isolation resistor is determined by the impedance ratio of coupled lines and the sheet resistance of polysilicon layer. This results in undesired capacitive effects at high frequencies as shown in Fig. 5 for the resistors R_2 and R_3.

The frequency of operation can be extended without major changes in the presented structure. The main limitation for the bandwidth of operation comes from the signal line to ground line separation. When the metal strips are closely spaced, not only the fabrication, but also the design of the divider becomes extremely difficult.

V. Conclusion

A 20–35-GHz power divider was fabricated in CMOS technology with an improved postprocessing procedure. This low-cost power divider is monolithically integrated with low-frequency electronic circuits. It exhibits a coupling of -3.8 dB $\pm$ 0.6 dB.

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