Inverter Dynamic Electro-Thermal Modeling and Simulation with Experimental Verification[1]

J. Reichl*, J-S. Lai*, A. Hefner**, T. McNutt**, D. Berning**

* Future Energy Electronics Center, Virginia Polytechnic Institute and State University, Blacksburg, VA USA
** Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD USA

Abstract — A full electro-thermal simulation of a three-phase space-vector-modulated (SVM) inverter is performed and validated with measurements. Electrical parameters are extracted over temperature for the insulated gate bipolar transistor (IGBT) and diode electro-thermal models. A thermal network methodology that includes thermal coupling between devices is applied to a six-pack module package containing multiple IGBT and diode chips. The electro-thermal device models and six-pack module thermal model are used to simulate SVM inverter operation at several power levels. Good agreement between model and measurement is obtained for steady state operation of the three-phase inverter. In addition, transient heating of a single IGBT in the six-pack module is modeled and validated, yielding good agreement.

Keywords: DBC, electro-thermal model, IGBT module, model validation, thermal network, six-pack module, space vector modulation, three-phase inverter.

I. INTRODUCTION

Increasing demands for higher power density in power electronics is placing greater demands on improving the quality of understanding of the interactions between the thermal and electrical properties of semiconductor devices. The insulated gate bipolar transistor (IGBT) module has become the semiconductor switching device of choice for medium to high power applications during the past several years. These modules contain multiple IGBT and diode chips mounted on a common baseplate with an insulating medium. As a result of the close proximity of the IGBT and diode chips, thermal coupling within the module must be considered for effective computer aided design of the power electronic system.

In reference [1], a methodology was introduced for simulating the full electro-thermal behavior of power electronic systems. This methodology was extended by using compact electro-thermal models for the power semiconductor devices [2], and using thermal network component models for the heat conduction and cooling system components [3]. An example electro-thermal inverter simulation without validation was performed in [4], including the electro-thermal behavior of a discrete IGBT package, but the electro-thermal behavior for the diode was not included. Recently, several electro-thermal models have been developed for different power devices and modules using this methodology [5-8] but validated electro-thermal system simulations have not been presented.

In this paper, simulated and measured electro-thermal results are presented for a space vector modulated (SVM) [13] three-phase inverter using multiple IGBTs and diodes in a six-pack module package. The simulations use the recently developed six-pack thermal network component model [7] that includes lateral heat coupling effects between all devices within the package and an advanced node spacing algorithm to increase accuracy and computational efficiency. Model parameters are extracted for both the IGBTs and diodes within the module. This paper presents the first electro-thermal simulation including both IGBT and diode electro-thermal models, the first electro-thermal simulation of a full-wave three-phase inverter, and the first system simulation to include a fully coupled six-pack module package thermal model. The models and simulation are experimentally validated for the electrical and thermal, steady-state and transient condition of the inverter.

II. ELECTRO-THERMAL DEVICE MODELS

To perform electro-thermal simulations using the Saber®[2] circuit simulator, the compact electro-thermal models for power semiconductor devices are connected to both the electrical and thermal networks [2]. For example, the IGBT electro-thermal model has three electrical terminals (gate, collector, and emitter) and one thermal terminal for the junction temperature. The IGBT electrical terminals are connected to other electrical network components of the inverter, and the thermal terminal is connected to suitable thermal network component models such as chip, six-pack module package, and heat sink models.

In order to couple the electrical and thermal networks, the IGBT electro-thermal model needs to describe the instantaneous electrical behavior in terms of the instantaneous temperature of the device silicon chip surface. The temperature-dependent electrical model is based upon the IGBT model parameters and the physical properties of silicon. The IGBT electro-thermal model also calculates the instantaneous power dissipation that supplies heat to the surface of the silicon chip thermal model through the thermal terminal.

To perform the electro-thermal simulations, models must be available for each electrical and thermal component of the system and parameters must be extracted for each semiconductor device. The electrical and thermal model parameters extracted in this paper are shown in Table 1 for the IGBT and diode models. The IGBT model parameters are extracted using the IMPACT tools [9,10] and the diode

[1] Contribution of the National Institute of Standards and Technology; not subject to copyright.

[2] Certain products are identified to better explain procedures. This identification is not a product endorsement, and the products so identified may not be the best for the purpose.

Authorized licensed use limited to: NIST Virtual Library (NVL). Downloaded on July 26,2010 at 17:51:48 UTC from IEEE Xplore. Restrictions apply.

model parameters are extracted using the procedure developed in [11]. These parameters are used with the Saber IGBT and diode electro-thermal models, along with the six-pack module thermal model to simulate the SVM three-phase inverter described below.

Table 1. Extracted parameters for electro-thermal device models

A. Electro-thermal IGBT Model Parameters

$A = 1\ \text{cm}^2$	IGBT chip area
$I_{sneo} = 1.5\times10^{-12}\ \text{A}$	Emitter electron saturation current
$W_b = .015\ \text{cm}$	Metallurgical drift region width
$V_{TO} = 6.4\ \text{V}$	MOSFET channel threshold voltage
$N_b = 1.5\times10^{14}\ \text{cm}^{-3}$	Base dopant density
$K_{plino} = 23\ \text{A/V}^2$	Linear region transconductance
$K_{psato} = 11.5\ \text{A/V}^2$	Saturation region transconductance
$\tau_{HLO} = .651\ \mu\text{s}$	High level minority carrier lifetime
$C_{gs} = 3.98\ \text{nF}$	Gate - source capacitance
$C_{oxd} = 15.1\ \text{nF}$	Gate - drain overlap oxide capacitance
$\tau_{HL1} = 2.365$	High level minority carrier lifetime temp. coeff.
$I_{sne1} = 1.189$	Emitter electron saturation current temp. coeff.
$V_{T1} = -7.2\ \text{mV/K}$	MOSFET channel threshold voltage temp. coeff.
$K_{plin1} = 1.0286$	Linear region transconductance temp. coeff.
$K_{psat1} = 2.1032$	Saturation region transconductance temp. coeff.

B. Electro-thermal Diode Model Parameters

$I_{SL} = 1.25\ \text{mA}$	Saturation current for low level recombination
$N_L = 3.89$	Emission coefficient for low level injection
$BV = 600\ \text{V}$	Breakdown Voltage
$C_{JO} = 3\ \text{nF}$	Zero - bias junction capacitance
$T_{SW} = 130\ \text{ns}$	Charge sweep out time
$TT = 165\ \text{ns}$	Carrier Lifetime
$X_{TI} = -2.36$	I_{SL} temperatu re exponent
$T_{NL1} = -6.35\times10^{-4}$	Linear NL temperatu re coefficien t
$T_{NL2} = -4.14\times10^{-6}$	Quadratic NL temperatu re coefficien t
$BETA = 1.71$	Temperatur e exp. of carrier lifetime TT
$BETASW = 1\times10^{-6}$	Temperatur e exp. of carrier lifetime T_{SW}

III. THERMAL NETWORK MODELS

The thermal network component models describe the heat flow process from the semiconductor heat sources to the cooling system including thermal coupling between devices. The method used to develop and to implement thermal network component models in the Saber circuit simulator is described in [3]. This method was used in [7] to develop a thermal model for a six-pack IGBT power module which consists of silicon chips, direct bond copper (DBC) electrical insulating layer structures, and a base plate as indicated in Fig. 1.

The thermal network component models are derived from the heat diffusion equation. Important parameters used with the IGBT electro-thermal model include the geometry of the component, the nonlinear thermal properties of the material, and other non-linear heat transport mechanisms such as convection. The three-dimensional heat flow is accounted for by using the appropriate symmetry in the discretization in each region of the component using the effective heat flow area approach [3]. This is used to derive expressions for the two-dimensional network of thermal resistances, thermal capacitances, and the heat energies. The accuracy of the thermal component model is determined by the number and the locations of the thermal nodes within the component. The thermal gradients disperse as the heat diffuses through the chip, so a grid spacing that increases logarithmically with distance from the heat source results in the minimum number of thermal nodes required to describe the temperature distribution for a range of power dissipation levels.

As shown in Fig. 1, there are three DBC insulating structures mounted on one baseplate, where each DBC structure contains two IGBTs and two diodes. Each IGBT is a paralleled combination of two silicon chips and each diode is comprised of one chip. Each chip, 18 total, is accounted for in the thermal model by using an advanced effective heat flow area algorithm to represent each IGBT (Q1-Q6 in Fig.1) and diode (D1-D6) as a unique thermal source. The thermal model is then divided into 12 thermal networks with a thermal network designated for each IGBT (Q1-Q6) and for each diode (D1-D6). Within each network, three sections are considered: one section is for the silicon chip, one for the DBC, and one for the base-plate layer. Lateral coupling between the networks is also included.

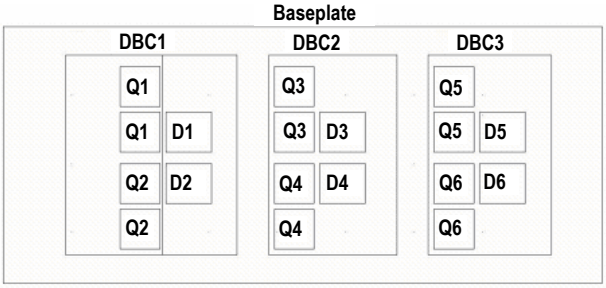


Fig.1 Internal structure of the studied power module

IV. INVERTER SIMULATION AND MODEL VALIDATION

Figure 2 shows the circuit diagram of a six-pack IGBT module-based inverter for a 10-kW ac motor drive. The module is mounted on a motor end plate, as shown in Fig. 3. The picture also indicates that four parallel-connected high-frequency dc bus capacitors, represented by C_{dc}, are surrounding the module to ensure sufficient bypassing.

There are eight switching states. Fig. 4 shows each switching state vector. Vectors V_1-V_6 trace out a hexagon divided into six sectors with sixty degrees apart. These vectors represent the three phase voltages with switching states (100), (110), (010), (011), (001), and (101), respectively. Using vector V_1 as the example, the corresponding switching state (100) means phase-a upper

Authorized licensed use limited to: NIST Virtual Library (NVL). Downloaded on July 26,2010 at 17:51:48 UTC from IEEE Xplore. Restrictions apply.

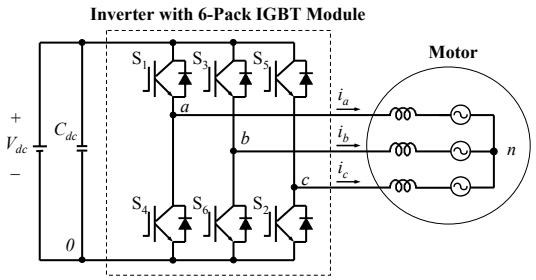


Fig. 2. Circuit diagram of the three-phase inverter motor drive using a six-pack IGBT module.

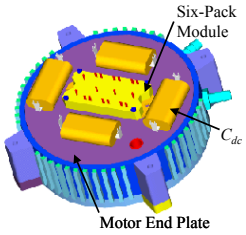


Fig. 3. Physical mounting of IGBT on a motor end plate.

switch S_1 is turned on, while phase-b and -c upper switches S_3 and S_5 are turned off. It should be noticed that upper and lower switches in each phase should be switched complimentarily. Thus switching state (100) also means phase-a lower switch S_4 is turned off, and phase-b and -c lower switches S_6 and S_2 are turned on.

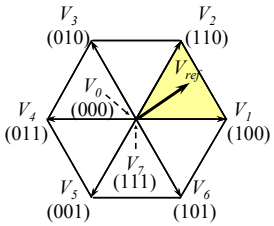


Fig. 4. Sector partition in a space-vector diagram.

Vectors V_1-V_6 all have the same magnitude, but different phase angles. Vectors V_0 and V_7 both have a magnitude of 0 and are designated as the zero switching state. This state can be realized by turning on all the lower or upper switches. The output voltage reference V_{ref} has a magnitude and an angle that are typically different from any of the vectors. There are numerous SVM methods to synthesize V_{ref} [13]. Some SVM methods emphasize the output waveform quality, and some emphasize the efficiency. The particular SVM method used in this research study is to have a switching sequence of chosen switching vectors shown in Fig. 5. Using the shaded sector shown in Fig. 4 as the example, this particular sequence synthesizes the voltage reference V_{ref} with both zero vectors (V_0, V_7) and two adjacent vectors (V_1, V_2) with a symmetrical sequence, resulting in the lowest total harmonic distortion (THD). The sequence in Fig. 5 also indicates the switch turn-on or -off duties for the shaded sector that is enclosed by (V_1, V_2) and zero vectors (V_0, V_7). Time intervals or duty cycle periods T_0, T_1 and T_2 are calculated by the digital signal processor (DSP) in every switching cycle T_s. The duty cycle periods should satisfy $V_{ref} = (V_1 \cdot T_1 + V_2 \cdot T_2)/T_s$ and $T_s = T_0 + T_1 + T_2$.

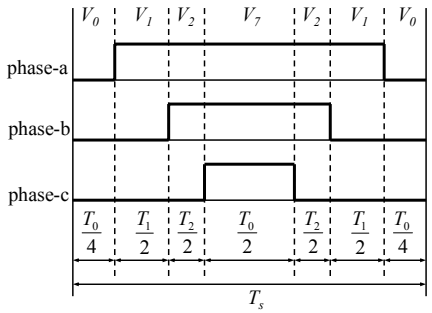


Fig. 5. Space vector modulation diagram timing diagram of the SVM inverter control algorithm.

The turn-on period of the phase-a upper switch is the sum of $T_1 + T_2 + T_0/2$, the turn-on duty of phase-b upper switch is the sum of $T_2 + T_0/2$, and the turn-on duty of phase-c upper switch is $T_0/2$. Similar switching patterns can be applied to other sectors.

The test circuit of Fig. 6 is used to independently validate the performance of the 6-pack module package thermal model. This circuit uses the temperature sensitive parameter (TSP) method to measure the IGBT chip transient temperature response where the gate-cathode threshold voltage is the TSP [12]. Either upper or lower IGBTs (IGBT1 or IGBT2) can be used; the unused devices of the six-pack are disabled by connecting their gate and cathode terminals together as shown. Neither diode is forward biased during the measurements.

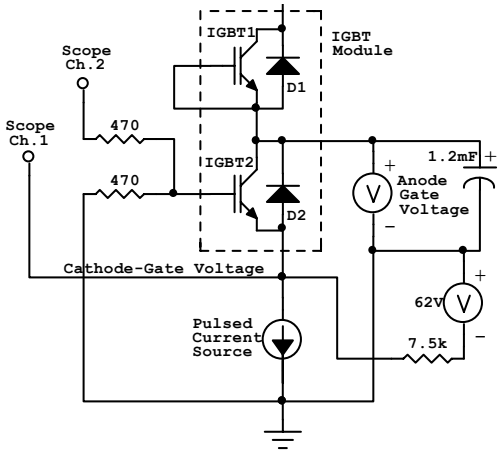


Fig. 6. High Speed IGBT Thermal transient test circuit.

The cathode of the test IGBT is connected to a pulsed constant current source that is referenced to ground, and the anode of the IGBT is connected to a heavily-bypassed voltage supply, also referenced to ground. The gate of the IGBT is grounded through a 470 Ω resistor that serves as a damping resistor to prevent oscillation. This circuit arrangement causes the IGBT to operate in the active or linear region during the heating phase of the measurement. There is a small auxiliary current source comprised of a 62 V voltage supply and 7.5 kΩ resistor which is used to limit the amplitude of the measured switching voltage that

Authorized licensed use limited to: NIST Virtual Library (NVL). Downloaded on July 26,2010 at 17:51:48 UTC from IEEE Xplore. Restrictions apply.

appears on the cathode, and to provide the capability of using the TSP measurement during the cooling phase [12]. The cathode voltage is applied to channel 1 of a digitizing oscilloscope, and the gate voltage is applied to channel 2 of the oscilloscope. The data acquisition is used to provide a differential gate-to-cathode measurement because a substantial voltage transient appears at the gate during switching.

Fig. 7 shows the measured and simulated transient thermal response of the six-pack module package to heating one IGBT at different power levels: 380 W, 950 W, and 2700 W. The simulations were run in Saber using a constant power pulse source connected to the IGBT thermal module model. Only one IGBT is connected to the power source. A constant temperature source is connected to the base plate of the module representing the constant heat sink temperature used in the experiment.

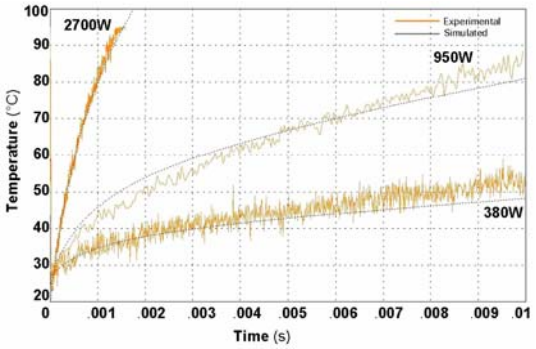


Fig.7. Simulated transient thermal response of 6-pack module for heating of single IGBT under various power conditions with experimental verification using high-speed temperature sensitive parameter measurement.

The inverter simulation was implemented in Saber using the physics based electro-thermal models for the IGBTs and diodes. The SVM control scheme was implemented in a Saber MAST model. In the MAST model, the duty ratios were calculated based on the modulation index, switching frequency, and bus voltage. The model for the IGBT gate drivers are behavioral models, which convert the digital inputs (logic signals) created from the SVM MAST model to the appropriate analog IGBT gate-drive signals. In this case, the gate drive signals switch from -5 to 17 V with 10 ohms of series gate resistance.

Figure 8 demonstrates the functional circuit implemented in Saber, where each IGBT (Q) and diode (D) correspond to those of Fig. 1. The gate terminals of the IGBT are tied to the behavior gate drive model (not shown). The thermal terminals on the IGBT's and diodes connect to the six-pack IGBT thermal model via a common net name. The motor is modeled as an inductor-resistor network on each phase as shown. The inductors are 1mH and resistors are 2.2 Ω. The module base-plate used in hardware is mounted on a temperature controlled heat sink; likewise, the thermal model in the simulation connects the module base-plate to a constant temperature source. This is designated as Ambient in the figure. An effective thermal resistance designated $R_{thermeff}$ is shown, which includes an insulating layer of Thermstrate[TM,3] placed between the base-plate and heat sink. The thermal resistance of the Thermstrate[TM] was determined to be 0.025°C-in^2/W. Each thermal node of the base-plate was given a thermal resistance based on the effective heat flow area at that node. The thermal resistances of each node were then combined in parallel to give the effective thermal resistance $R_{thermeff}$ shown in Fig. 8.

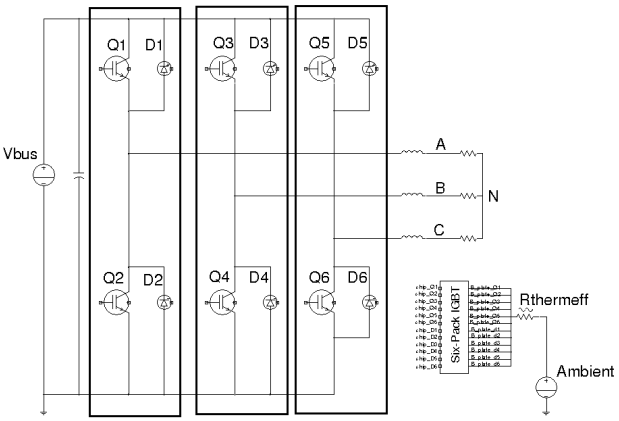


Fig. 8. Functional circuit used in the simulation

The temperatures at several points in the inverter system were monitored with thermocouples, and the temperature monitored at the IGBT base-plate was used for thermal validation. Both transient and steady state temperatures were recorded and analyzed.

The inverter was pulsed with a series of different power levels and baseplate temperature measurements were made as shown in Fig 9. Three power levels designated Case1 (4 kW), Case2 (7 kW), and Case3 (11 kW) are used for model validation. All three cases use a modulation index of 0.8 and switching frequency of 10 kHz. The active time for each inverter power level is long enough for the inverter and thermal network being validated to reach a steady-state condition. Also shown on the figure is the average temperature that was measured.

As seen in Fig 9, it takes 50 to 100 seconds to arrive at a thermal steady-state condition. This is very difficult to do with limited storage space and computational speed in the simulator.

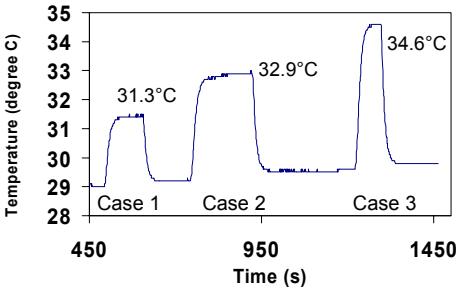


Fig. 9. Measured transient heating of single IGBT under various power conditions

[3] Certain products are identified to better explain procedures. This identification is not a product endorsement, and the products so identified may not be the best for the purpose.

Authorized licensed use limited to: NIST Virtual Library (NVL). Downloaded on July 26,2010 at 17:51:48 UTC from IEEE Xplore. Restrictions apply.

To account for this difficulty, a four-step iterative process is used to determine the initial condition for the IGBT temperature.

1- First, a full electro-thermal simulation of the inverter is performed over a few 60 Hz cycles (three in this case).
2- The average dissipated power is determined for each device using the Wave-Calc waveform calculator in Saber Scope to integrate the dissipated power over a complete 60 Hz cycle.
3- The calculated value of the average power is then used in a pulsed power source into the thermal model to determine an initial temperature condition for the IGBT.
4- Another full electro-thermal simulation is performed with the initial temperature condition found in step 3.

This iterative process is repeated until the average power converges to steady state. Fig. 10 shows all three phase currents for two 60 Hz cycles of Case 3, and Fig. 11 shows the corresponding chip junction temperatures for each phase. Notice the IGBT junction temperatures have spikes occurring at the switching frequency, 10 kHz. This is due to the switching losses. The 60 Hz variations of the IGBT chip surface temperatures are due to the sinusoidal load current variation. Obviously the highest magnitude of temperature occurs during the peak amplitude of load current.

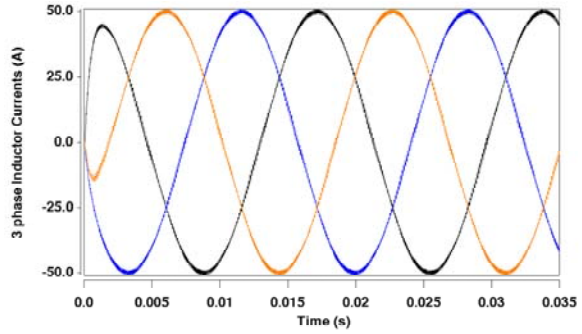


Fig. 10. Simulated three-phase inverter current waveform for each phase in a two 60 Hz cycles of the inverter for the 10.8 kW condition.

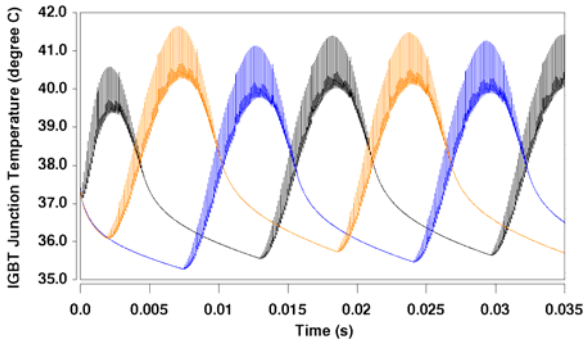
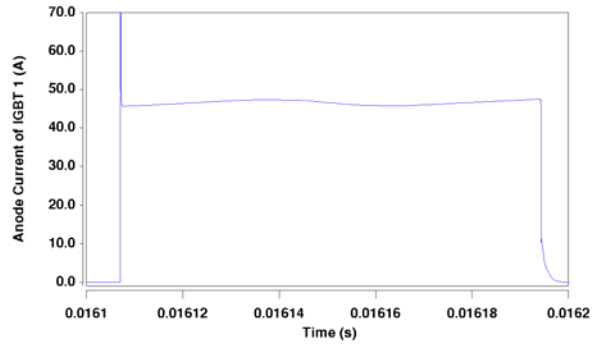


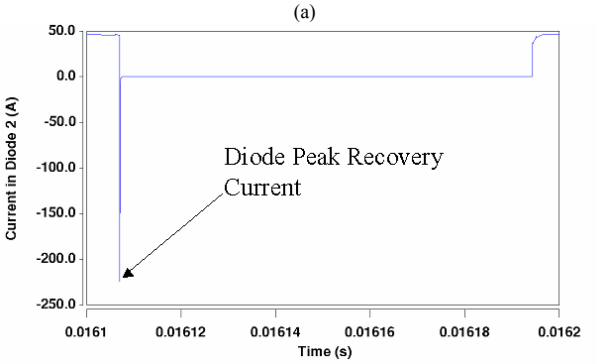
Fig. 11. Simulated three-phase inverter IGBT chip junction temperature waveform for each phase in two 60 Hz cycles of the inverter for the 10.8 kW condition.

The current in each phase is conducted through an IGBT and anti-parallel diode. Considering phase "a" for a moment made up of Q1, Q2, D1 and D2. When the inductor load current is positive, the current is carried through Q1 and D2. When the load current goes negative, the current is carried through Q2 and D1. Other phases operate in the same manner.

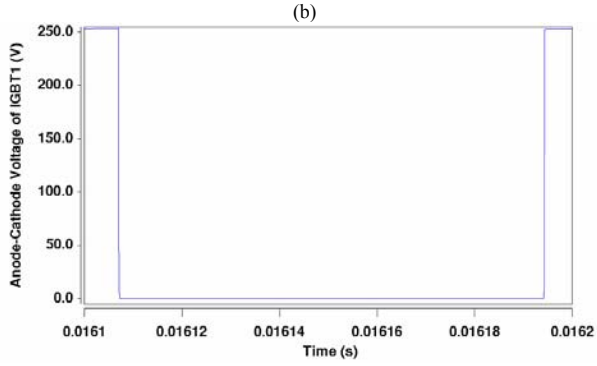
The next set of figures shows a switching cycle condition for IGBT 1 designated Q1 in Fig 8. The IGBT anode current, current though D2, anode voltage, power dissipation, energy and IGBT chip surface temperature for Case 3 are shown in Fig.12(a-f).



(a)

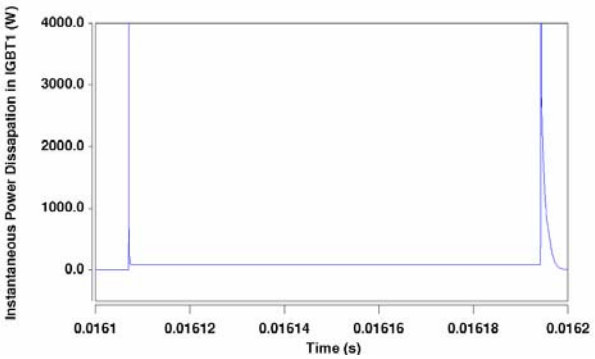


(b)

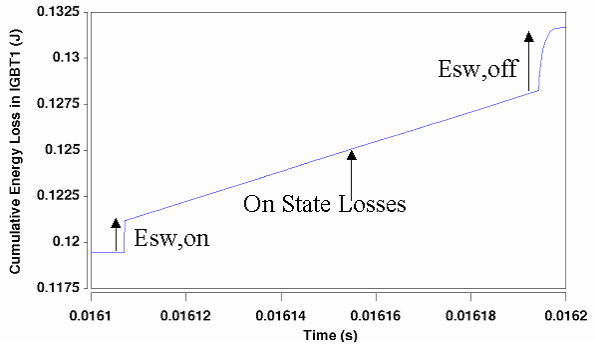


(c)

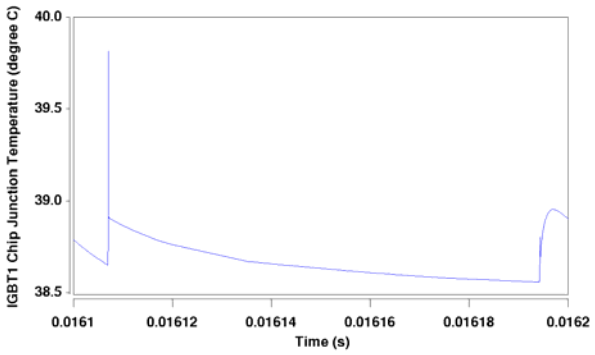
Authorized licensed use limited to: NIST Virtual Library (NVL). Downloaded on July 26,2010 at 17:51:48 UTC from IEEE Xplore. Restrictions apply.



(d)



(e)



(f)

Fig. 12. Simulation results of one 10 kHz switching cycle for the (a) IGBT anode current, (b) current though D2, (c) anode voltage,(d) power dissipation, (e) energy and (f) IGBT chip surface temperature for Case 3.

The spike at turn-on occurs because Q1 is forced to block the full supply voltage of 252 V and a current that is larger than the load current during the reverse recovery of D2. This reverse recovery spike from the diode can be seen in Fig 12a. In practice, this turn-on energy/loss, Esw-on seen in Fig. 12d, can be reduced by using a larger IGBT gate resistance as to reduce the peak diode reverse recovery. However, this results in higher over all duty cycle loss because the device takes longer to turn on. Once the reverse recovery of D2 is complete, the voltage across Q1 drops and approaches the IGBT on-state voltage.

The instantaneous power dissipation is now determined by the product of the on-state voltage and load current. This power dissipation makes up the on-state or conduction losses. The power dissipation during the on-state condition of the switching cycle is much smaller than the power dissipation seen during switching, but is much longer in duration. Therefore, the energy-loss waveform of Fig. 12e rises with a constant slope (determined by the load current and IGBT on-state voltage) during the on-state phase of the switching cycle.

Simulated voltage and current waveforms are shown in Fig.13 for a single turn-off event for Q1. When Q1 is commanded to turn off, the anode-to-cathode voltage rises. This voltage is eventually clamped by D2 at the bus voltage of 252 V plus the on-state voltage of D2 because constant current is maintained in the load inductance. The anode current through Q1 then drops rapidly due to the channel being cut off. A slow decaying tail follows which is caused by the stored charge in the base region of Q1. This decaying tail increases as temperature increases and leads to higher losses because the lifetime increases with temperature.

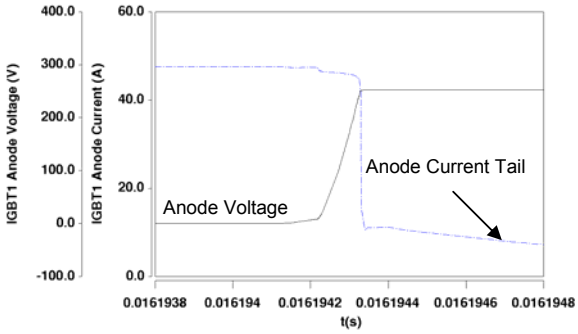


Fig. 13. Turn off Waveforms of IGBT1

Thus, a large anode-cathode voltage and current exist at the same time, resulting in a large power dissipation and temperature spike at turn-off. Although the power dissipation level is not as high as during the turn-on event, the turn-off switching time is much longer due to the slowly decaying excess carriers in the IGBT base. Thus, the turn-off switching energy $E_{sw,off}$ indicated in Fig. 12(e) is larger than the turn-on energy.

Fig. 14 shows the simulated relationship between the IGBT chip surface temperature, T_j, the package header chip interface T_h, and the package case base-plate interface T_c. The chip junction is the only node that has a thermal response to the high switching frequency. This is because the other two nodes have higher capacitive energies and only respond to the lower frequency. As a result, the lower nodes only respond thermally to the 60 Hz load variation. As the nodes get even further down into the module towards the bottom of the base-plate, there is not much thermal response to the 60 Hz. The high capacitive energies of these lower nodes do not respond to the lower frequency, but take much longer to reach steady state condition. This is the reason for initial conditions in the electrical simulation. It will be shown later, that these lower nodes take a few seconds or even minutes to reach steady state.

Authorized licensed use limited to: NIST Virtual Library (NVL). Downloaded on July 26,2010 at 17:51:48 UTC from IEEE Xplore. Restrictions apply.

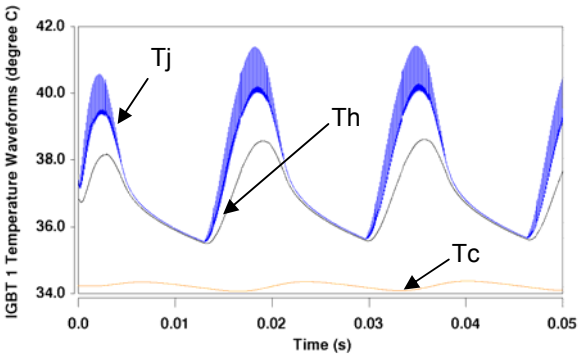


Fig. 14. Temperature waveforms of IGBT1 showing surface Tj, header chip interface Th, and case base-plate interface Tc.

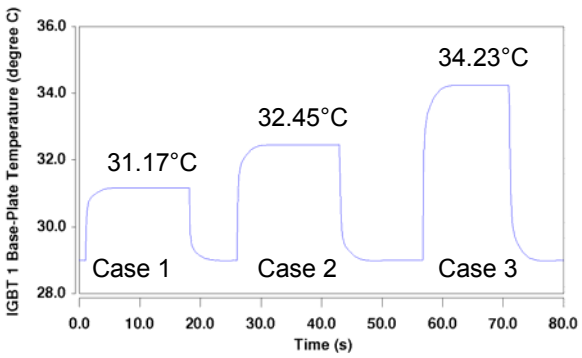


Fig. 15. Base-plate temperatures of IGBT1 for the cases shown in Table 2.

The temperature T_c in Fig.14 shows the instantaneous base-plate temperature of IGBT 1 for case 3, resulting from the full electro-thermal simulation. Fig. 15 shows the average base-plate temperature, used for model validation, of IGBT 1 resulting from a thermal simulation of each case. The thermal simulation uses a constant power pulse equal to the average steady state power measured in the full electro-thermal simulation. The power pulse is used as an input to the thermal model network. Note, the time scale of Fig. 15 differs from the time scale of Fig. 9 because only steady state operation is required for validation and thus does not require the same amount of time shown in Fig. 9. The average power dissipated in the IGBTs and diodes for each case was calculated as shown in Table 2. Table 3 compares the measured and simulated results for all three cases.

Figure 16 illustrates device-device coupling effects considered in the six-pack module model by showing the difference in average DBC temperatures of D1 for each power pulse. Note that with device-device coupling, D1 is a few degrees warmer due to heat coupling through the DBC between Q1,D1,Q2,and D2 [7].

Table 2. Average Steady State Power of each case

	IGBT	Diode
Case 1	17 W	1.5 W
Case 2	27 W	2.2 W
Case 3	41 W	2.9 W

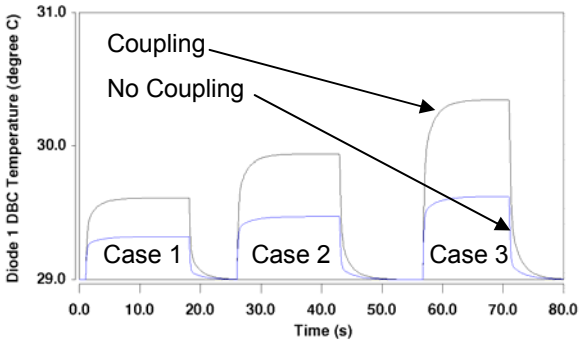


Fig. 16. DBC temperatures of Diode 1 for each case in Table 2, both with and without device-device coupling.

V. CONCLUSION

A full electro-thermal simulation of a three-phase SVM inverter has been performed and validated. A thermal network methodology that includes thermal coupling between devices has been applied to a six-pack module package containing multiple IGBT and diode chips. The electro-thermal device models and six-pack module thermal model are used to simulate SVM inverter operation at several power levels. Good agreement between model and measurement has been obtained for steady state operation of the three-phase inverter, as well as the transient heating of a single IGBT in the six-pack module.

Table 3. Measured vs. Simulated Results

Case 1 – 150 V Bus Voltage	**Simulated**	**Measured**
Output current (rms)	20.9 A	22.6 A
Average steady state temperature	31.17 °C	31.3 °C
Case 2 – 200 V Bus Voltage	**Simulated**	**Measured**
Output current (rms)	27.95 A	30.02 A
Average steady state temperature	32.45 °C	32.9 °C
Case 3 – 252 Bus Voltage	**Simulated**	**Measured**
Output current (rms)	35.1 A	38.35 A
Average steady state temperature	34.23 °C	34.6 °C

Authorized licensed use limited to: NIST Virtual Library (NVL). Downloaded on July 26,2010 at 17:51:48 UTC from IEEE Xplore. Restrictions apply.

REFERENCES

[1] A.R. Hefner, D.L. Blackburn, "Simulating the Dynamic Electro-Thermal Behavior of Power Electronic Circuits and Systems," *IEEE Trans. on Power Electronics*, vol. 8, pp. 376, 1993.

[2] A.R. Hefner, "A Dynamic Electro-Thermal Model for the IGBT," *IEEE Trans. on Industry Applications*. vol. 30, p. 394, 1994.

[3] A.R. Hefner, D.L. Blackburn, "Thermal Component Models for Electro-Thermal Network Simulation," *IEEE Trans. on Components, Packaging, and Manufacturing Technology* vol. 17, p. 413, 1994.

[4] H. Mantooth, A. Hefner, "Electro-thermal Simulation of an IGBT PWM Inverter," in *IEEE Trans. on Power Electronics*, vol. 12, pp. 474, 1997.

[5] H. Mantooth, J. Duliere, "A unified diode model for circuit simulation," *IEEE Trans. on Power Electronics*, vol. 12, no. 5, Sept. 1997.

[6] J. Rodriguez, Z. Parrilla, M. Veléz-Reyes, A. Hefner, D. Berning, J. Reichl, and J. Lai "Thermal Component Models for Electro Thermal Analysis of Multichip Power Modules," *Conf. Rec. IEEE Industry Applications Society Meeting*, pp. 234-241, Oct. 2002.

[7] J. Reichl, D. Berning, A. Hefner, J. Lai, "Six Pack IGBT Dynamic Electro-Thermal Model; Parameter Extraction and Validation," *Proc. of IEEE Applied Power Electronics Conference and Exposition*, pp.246-251, Anaheim, CA, Feb. 2004.

[8] T. Kojima, Y. Yamada, Y. Nishibe, M. Ciappa, and W. Fichtner, "A Novel Compact Thermal Modeling Approach to Electro-thermal Simulation for Automotive IGBT Modules," *Proc. of International Power Electronics Conf,* pp. 787-792, Niigata, Japan, April 2005.

[9] A.R. Hefner, "Modeling Buffer Layer IGBT's for Circuit Simulation," *IEEE Trans. on Power Electronics*, vol. 10, pp.111-123, March 1995.

[10] A.R. Hefner, "Automated Parameter Extraction Software for Advanced IGBT Modeling," *Proc. of IEEE Workshop on Computers in Power Electronics,* pp. 10-18, Blacksburg, VA, July 2000.

[11] T. McNutt, A. Hefner, A. Mantooth, J. Duliere, D. Berning, R. Singh, "Parameter Extraction Sequence for SiC Schottky, Merged PiN Schottky, and PiN Power Diode Models," *Proc. IEEE Power Electronics Specialists Conf,* pp. 1269-1276, Cairns, Australia, June 2002.

[12] D. Berning, J. Reichl, A. Hefner, M. Hernandez, C. Ellenwood, and J. Lai, "High Speed IGBT Module Transient Thermal Response Measurements for Model Validation," *Proc. IEEE Industry Applications Conf*, Oct. 2003, pp. 1826-1832.

[13] D.G. Holmes and T.A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice,* New York, NY: IEEE Press and John Wiley & Sons, 2003.

Authorized licensed use limited to: NIST Virtual Library (NVL). Downloaded on July 26,2010 at 17:51:48 UTC from IEEE Xplore. Restrictions apply.