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Intercomparison of Methods for Detecting and Characterizing Voids in Bonded Wafer Pairs

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The Wafer Bond Task Force of the SEMI MEMS Standards Committee has begun a round robin experiment to evaluate methods for identifying and characterizing voids in bonded wafer pairs for three-dimensional integrated circuit (3D IC) applications. Due to the numerous process steps that the wafers have undergone and the presence of Through-Silicon Vias (TSVs), bonded wafers containing 3D ICs are expected to suffer a higher rate of post-bonding voids than other bonding applications. In addition, 3D ICs will likely be more sensitive to small voids than other bond applications. In this round robin experiment eight approaches to void metrology are being compared by 13 participating laboratories to highlight the relative abilities of each of these metrologies to identify potentially killer defects.

Background

Wafer bonding, a technology for combining multiple wafers into a single substrate, provides a powerful tool for a number of disparate applications. These include packaging of MEMS devices, where the devices are patterned into a wafer and an unpatterned wafer is bonded to the surface to provide a high-quality seal to maintain an environment within the package (vacuum, dry, etc.) and/or protect the device from the outside environment. In some instances, a transparent cap wafer (e.g., borosilicate glass) is used to allow for optical signals to pass to the MEMS device. For successful bonding, both surfaces must be smooth and extremely clean.

Another application is producing engineered substrates for high-performance CMOS processes. The most common of these is silicon-on-insulator (SOI), but also includes substrates engineered with different materials (e.g., III-V on silicon) or crystal orientations (e.g., (110) silicon on (100) silicon). These engineered substrates are normally produced using unpatterned wafers and the top (device) layer is thinned so the stack is only slightly thicker than a single wafer. For most engineered substrate applications, both starting wafers are unpatterned; these bonds require rotational orientation to ensure that the desired silicon planes are aligned.

A third application in production is stacked chips, referred to as 3D integration. 3D integration provides increased packaging density, through stacking and connecting multiple patterned chips, thus increasing areal density without shrinking the transistors or increasing the chip size. In addition to increasing transistor density, wafer bonding will allow for heterogeneous integration of dissimilar circuits, such as logic CMOS, DRAM CMOS, MEMS, optoelectronics, etc. These circuits typically cannot be co-fabricated using a single process due to dissimilar starting materials (silicon vs. III-V) and/or process flows (temperature, materials, etc.).

The simplest form of 3D chip stacks involves bonding a stack of chips to a wafer and using wire bonding to connect the different layers. To facilitate the wire bonding, the chips are progressively slightly smaller towards the top of the chip stack. This technology is used for applications where volume is at a premium, such as cell phones and other portable devices.

An alternate approach to directing signals between stacked chips is through the use of through-silicon vias (TSVs), which are metal plugs extending through the wafer. In this approach, holes are etched through the silicon and filled with a conductor, such as copper. This process can involve thinning the wafer, either before or after etching and filling the TSV. After bonding, electrical signals are transmitted through these TSVs between the chips. TSVs have the advantage of reduced delay between circuit elements on different chips. However, they are more susceptible to failure due to misalignment and partial delamination.

Electrical connection between the different layers of a 3D IC will be provided by through-silicon vias (TSVs), which are vertical metal plugs through one wafer; these TSVs must be aligned to specific features on the second wafer. The presence of TSVs and other circuitry on the bond surface of each of the wafers to be bonded – in contrast to using bonding as a package or for SOI starting material, where one or both of the wafers is unpatterned – means that both wafer surfaces are likely to fail a basic requirement of successful wafer bonding: that the surfaces are smooth and clean. Rather, the surfaces will include different materials and will likely exhibit significant roughness, leading to a situation where the conditions are conducive to production of voids in wafer pairs. Such circuits are more sensitive to smaller voids than other applications of wafer bonding.

Metrology Needs for Wafer Bond

The MEMS packaging and 3D IC applications of wafer bonding have similar metrology needs. The key measurements relate to determining bond integrity. That is, after bonding, a determination needs to be made as to whether the bond is complete and of sufficient strength for the application. Unbonded regions, referred to as voids, can lead to premature failure of the bond or, if the device requires that the interior of the package be held at vacuum or another environment, can expose the device to the ambient. Bond strength is measured using delamination tests, such as the one described in SEMI Standard, **MS5-0310 - Test Method for Wafer Bond Strength Measurements Using Micro-Chevron Test Structures** (1).

A number of qualitative methods for identifying and characterizing voids remaining after bonding have been described in the literature. These methods will be described in

the following section. However, the 2009 International Technology Roadmap for Semiconductors (ITRS) highlights that successful implementation of 3D ICs will require a bond technology with alignment and void tolerances far beyond those needed for MEMS packaging applications (2). In this experiment we are moving from a qualitative approach – identifying the presence of large voids – to a quantitative measure of how different classes of tools can be used to identify and characterize voids. This experiment will provide a baseline for characterization of voids of dimensions that can serve as killer defects in 3D ICs. From the results of this experiment, the capabilities of different tools to measure progressively smaller voids will be better known by the 3D interconnect community.

Metrology Tools

A number of tools have been proposed and/or used for identification and localization of voids in the bond layer (note that metrology techniques that do not provide spatial information – dimension and location – are not being used in this experiment). However, in the literature, these measurements are typically used for relative and qualitative comparisons between different bonding processes (3) (4) (5). Even when a size distribution has been measured, the dimensions of the measured voids are in the range of 0.5 mm and higher, significantly above the expected killer defect value for 3D IC applications (6). The tools described in this section are those that one or more laboratories will use in the round robin experiment.

Scanning Acoustic Microscope (SAM)

Scanning Acoustic Microscopy (SAM) uses ultrasound, typically in the 100 MHz to 400 MHz frequency range, to survey the interface of a bonded wafer pair. Ultrasound is reflected, transmitted or refracted through bonded wafer pair materials. Differences in acoustic impedance of those materials allow an analog pattern of the wafer pair interface to be discerned through the transducer that both generates the ultrasound and measures its reflected signal. The transducer needs to have a coupling fluid present between the transducer and the bonded wafer pair, and typically, deionized water is used.

Voids (air gaps) between the bonded wafer pairs will not transmit ultrasound; 100% of the energy is reflected and can be mapped on the wafer pair as a void. Sub 100-micron resolution of voids is possible. SAM software can typically bin the void areas and locate them using a Cartesian coordinate system (Figure 1).

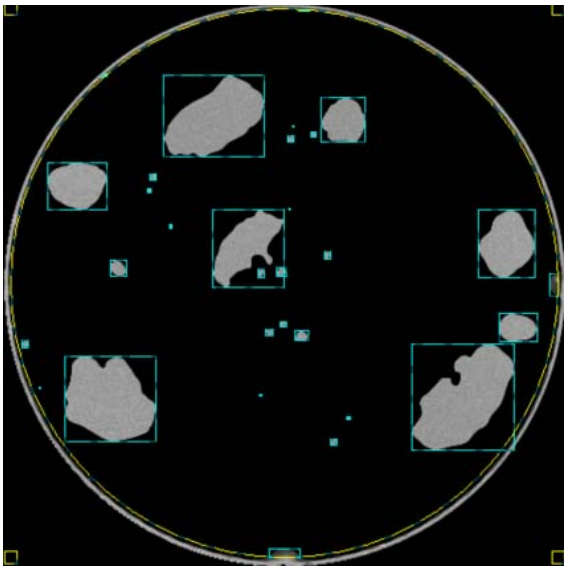

Figure 1. Void map, including size and location binning, on a bonded wafer pair derived from SAM image.

Resonance Ultrasonic Vibrations Technology (RUV)

RUV (7) uses vibrations in the 20 KHz to 100 KHz frequency range that are generated using a piezoelectric transducer which is vacuum coupled to a bonded wafer pair. A separate acoustic transducer monitors the deviation in the bonded wafer pair's resonance frequency response curve. Voids in the wafer pair are detected by comparing the bonded wafer pair RUV signal to a known void-free wafer pair's response curve. Void size and location is mapped by the acoustic transducer monitoring the bonded wafer pair.

Infrared Confocal Microscope

Silicon is opaque to the visible portion of the electromagnetic spectrum. Near Infrared (NIR) wavelengths (800nm – 1500 nm) can be used to evaluate the interface of bonded wafer pair in a variety of metrology techniques, including void and defect characterization. Sub-micron resolution for bonded wafer pair void metrology is possible using an IR confocal microscope (Figure 2). When an Infrared Confocal microscope is installed in a defect review tool, KLA results file format ((KLARF) defect maps are supported, enabling rapid void characterization.

Figure 2. Infrared image of missing adhesive (130-micron void) and particle at the interface of a bonded wafer pair. Dendritic structure formation for improperly cured adhesive is also shown (10-micron void).

Model Based Infrared Reflectometry (MBIR)

Mid-infrared wavelengths (>1500nm) are used to measure bonded wafer pairs. Reflected/refracted radiation from voids at the bonded wafer pair interface is evaluated by a model to characterize void size, depth and pattern uniformity (8). MBIR is a technique originally intended for measuring deep-trench DRAM structures and is being used for characterizing high-density through silicon vias (TSV). It will also be considered for void detection and characterization at the interface of bonded wafer pairs

Near Infrared Defect Metrology

Using Near Infrared optics, voids at the interface of a bonded wafer pair are identified as defects and mapped. Voids are detected as defects due to a deviation in the void's pixel representation when compared to a bonded wafer pair that is considered defect free (golden wafer pair). These deviations are mapped using KLARF files, and when reviewed in a defect review tool equipped with an IR microscope, rapid void characterization is enabled.

Figure 3. Defect (1) identified at interface of bonded wafer pair using NIR defect metrology

Full Wafer Infrared Illumination

A bonded wafer pair is illuminated (full wafer illumination) and inspected using NIR optics (9) (10). Macro-inspection techniques using transmitted and reflected IR enable bond layer delaminations, air-bubble inclusions and adhesive layer thickness variations to be identified and characterized when compared to a known void-free wafer pair.

IR Coherence Interferometer

IR Coherence Interferometry is a technique for capturing three-dimensional images from light scattered from a sample. This technique relies on the change in path for the light as it moves through different regions of the sample. The resultant signal is interpreted to give a full three-dimensional of the sample. Used since the early 1990s for imaging soft materials in biological applications, especially in-vivo diagnosis of the retina, it has more recently is being applied to non-biological applications (11), such as imaging voids in bonded wafer pairs.

Bonded wafer pairs are scanned using a low coherence IR interferometer. Voids at the interface of the of the bonded wafer pair cause reflections and scattering; from the resultant intererferometric signal, a three-dimensional representation of the sample, including location and dimension of voids, is produced.

X-ray tomography

X-ray tomography (11) (12) uses a similar approach to measurement as IR Coherence Interferometry, but instead of IR, it uses higher-energy X-Rays. In X-ray tomography, a

series of X-ray images is combined to create a complex three-dimensional image of the sample. This technology, which is also referred to as CT (or CAT) scanning, is used widely in medical and materials applications, including applications such as measuring the quality of wire bonds. Resolution of approximately one-micrometer resolution, at acceptable throughputs, is anticipated.

Round Robin

Round Robin Protocol

In a round robin experiment, each participating laboratory receives one or more samples to measure using their specific tool set. A measurement protocol is provided along with the samples. If the round robin is intended to investigate a single measurement tool or validate a standard, specific measurement procedures may also be provided. Thirteen laboratories – representing tool manufacturers and research organizations – are participating in this round robin. The final results of this round robin will be used in the development of a SEMI Standard Test Method for characterizing voids. It is expected that this standard will provide a best practice for using and reporting the results from several or all of the techniques used in the round robin.

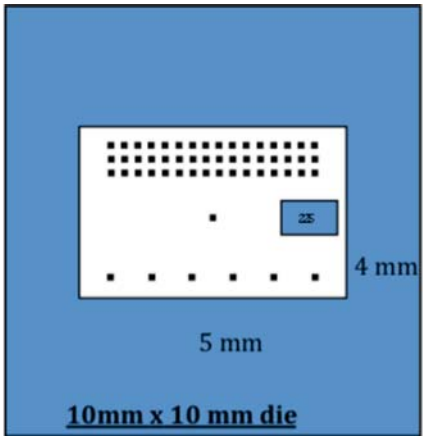

Figure 4. Schematic of the 10 mm by 10 mm test chip. Each black dot represents a programmed void; the programmed voids differ between test chips.

Round Robin Test Chip

A test chip set has been designed with programmed voids of different sizes (1 μm to 300 μm) and level of isolation – isolated, dense, and semi-dense (Figure 4). In addition to the multiple sizes, the bonded wafer pairs are fabricated with one of several programmed void thicknesses, ranging from 100 nm to 1000 nm. Eight instances of this test chip set will be patterned onto a set of 300 mm wafers (Figure 5). These wafers will be bonded to unpatterned, oxidized, wafers and sawn into quadrants, each quadrant containing two chip sets. Thirteen laboratories – representing tool manufacturers and research organizations – are participating in this round robin; each laboratory will receive quadrants from four wafers, each of which has a different programmed void thickness. These laboratories will characterize the voids using metrology tools such as IR, SAM, ultrasonic, etc. Each participating laboratory is receiving quadrants from four wafers,

each of which has a different programmed void thickness and be asked to report the locations and dimensions of the programmed voids.

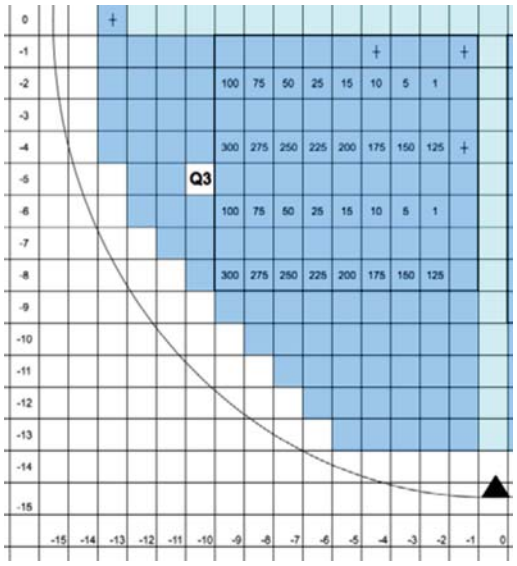

Figure 5. A quadrant of a 300 mm bonded wafer pair with two sets of test chips. Each participating laboratory is asked to characterize the test chips with one or more metrology tools.

The full results of this round robin will be used in the development of a SEMI Standard Test Method for characterizing voids. It is expected that this standard will provide a best practice for using and reporting the results from several or all of the techniques used in the round robin.

Conclusion

A round robin experiment involving thirteen laboratories is underway to provide quantitative data on how different classes of metrology tools are able to characterize voids between bonded wafers. The test structures are designed with programmed voids of dimensions near the smallest expected to be killer defects in 3D integration.

The final results of this round robin will be used in the development of a SEMI Standard Test Method for characterizing voids. It is expected that this standard will provide a best practice for using and reporting the results from several or all of the techniques used in the round robin.

The manufacturer of 3D chips stacks can use the results of this experiment to understand which tools are capable of identifying and characterizing voids of dimensions that would cause device failure.

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