# Modeling the Inter-Electrode Capacitances of Si CoolMOS Transistors for Circuit Simulation of High Efficiency Power Systems

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***Abstract* — The CoolMOS™+ transistor is a power MOSFET type device that utilizes a "super-junction" embedded within its drift region in order to improve the trade-off between on-resistance and breakdown voltage. The super-junction results in unique inter-electrode capacitance characteristics that require an advanced modeling approach to accurately represent switching performance. This paper describes a new compact circuit simulator model for the CoolMOS™ transistor and demonstrates the model performance using the Saber† simulator for a 650 V, 60 A device. The model is suitable for implementation in the Saber simulator that accurately describes all three inter-electrode capacitances (i.e., gate-drain, gate-source, and drain-source capacitances) for the full operating range of the device. The model is derived using the actual charge distribution within the device rather than assuming a lumped charge or one-dimensional charge distribution. Simulation results show excellent agreement with measurement results in contrast to previous modeling approaches used for this device. The compact model developed in this work is going to be utilized in the design of a high efficiency soft-switching inverter for electric vehicle motor drives and a high efficiency bidirectional DC-DC converter at zero-voltage switching (ZVS) operation.**

***Index Terms--CoolMOS™, power MOSFET, superjunction, compact model, inter-electrode capacitance.***

## I. INTRODUCTION

The CoolMOS™ transistor was introduced as an alternative device to provide the fast switching speed of power MOSFETs while also reducing the on-resistance by a factor of 5 [1] compared to conventional MOSFETs in the 500 V to 1200 V range. Fig. 1 shows a cross-sectional drawing of the CoolMOS™ transistor and includes a diagram of the internal capacitances of the device. As shown in Fig. 1, the drift region of the CoolMOS™ transistor is formed with a combination of vertical n- and p- strips [1, 2] rather than the constant n- region of the conventional power MOSFET. CoolMOS™ transistors serve as the main switching devices in many high efficiency soft-switching converter applications [3, 4]. Utilization of a CoolMOS™ device rather than an IGBT also allows synchronous rectification during the reverse conducting period and achieves fast turn-off without tail current. Recent work also considers a hybrid soft switching module approach consisting of an IGBT in parallel with a CoolMOS™ transistor.

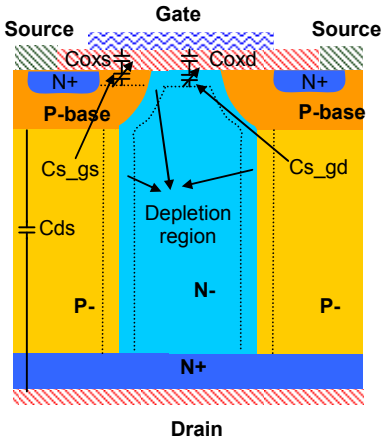


**Fig. 1** Cross-section of the CoolMOS™ transistor with inter-electrode capacitances model topology superimposed.

Characterization of all three inter-electrode capacitances, including drain-source capacitance ($C_{ds}$), gate-source capacitance ($C_{gs}$), and gate-drain capacitance ($C_{gd}$) of a 650 V

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Si CoolMOS™ transistor was demonstrated in [5]. The inter-electrode capacitances of power MOSFET type devices are very important in modeling its switching behaviors accurately, especially when investigating the effect of the variation of $C_{gd}$, which dominates the output switching waveforms due to the "Miller" effect. Although there are numerous power MOSFET models available, the previously developed models use a basic SPICE sub-circuit approach [6-10] and either uses a simple lumped charge approach [11] or a simplified one-dimensional delta-depletion [12] in the drift region to calculate the inter-electrode capacitances. These approaches do not adequately represent the nonlinear inter-electrode capacitance characteristics necessary to predict the device behavior for soft switching conditions or for hybrid modules using parallel IGBTs and CoolMOS™ devices.

This paper describes an approach for modeling the inter-electrode capacitances that accounts for the actual charge distribution inside the CoolMOS™ capacitors [13] and uses this approach to derive the presented Saber-compatible model. Linearization of the key model equation was also employed to simplify the numerical complexity while retaining the functional accuracy of the device capacitances. Model equations were implemented in Saber which was used to validate the CoolMOS™ model static and dynamic behaviors, as described later in this paper.

## II. Discussion of Equivalent Circuit

The basic device structure and model topology for an n-type CoolMOS™ transistor is shown in Fig. 1. The equivalent circuit in the nonconducting state is derived as shown in Fig. 2. $C_{gd}$ consists of the gate-drain overlap oxide capacitance ($C_{oxd}$) and the gate-drain junction capacitance ($C_{s\_gd}$) in a relationship given by

$$\frac{1}{C_{gd}} = \frac{1}{C_{oxd}} + \frac{1}{C_{s\_gd}} . \qquad (1)$$

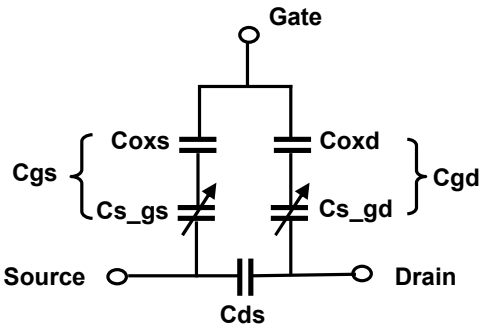



**Fig. 2** The simplified equivalent circuit of the CoolMOS™ transistor in the nonconducting state.

Similarly, $C_{gs}$ consists of the gate-source oxide capacitance ($C_{oxs}$) and the gate-source junction capacitance ($C_{s\_gs}$) in the same form as (1).

Characterization of the inter-electrode capacitances $C_{ds}$, $C_{gs}$, and $C_{gd}$ was performed using a custom-built high voltage CV measurement system which has a protection circuit isolating the high voltage from the LCR meter as well as many safety features [5]. Fig. 3 shows the measured results for $C_{gd}$ and $C_{gs}$, respectively, obtained by sweeping the gate voltage and stepping the drain voltage. As expected $C_{oxd}$ and $C_{oxs}$ are constant values under all conditions while $C_{s\_gd}$ and $C_{s\_gs}$ vary with the gate-source voltage ($V_{gs}$) and drain-source voltage ($V_{ds}$).

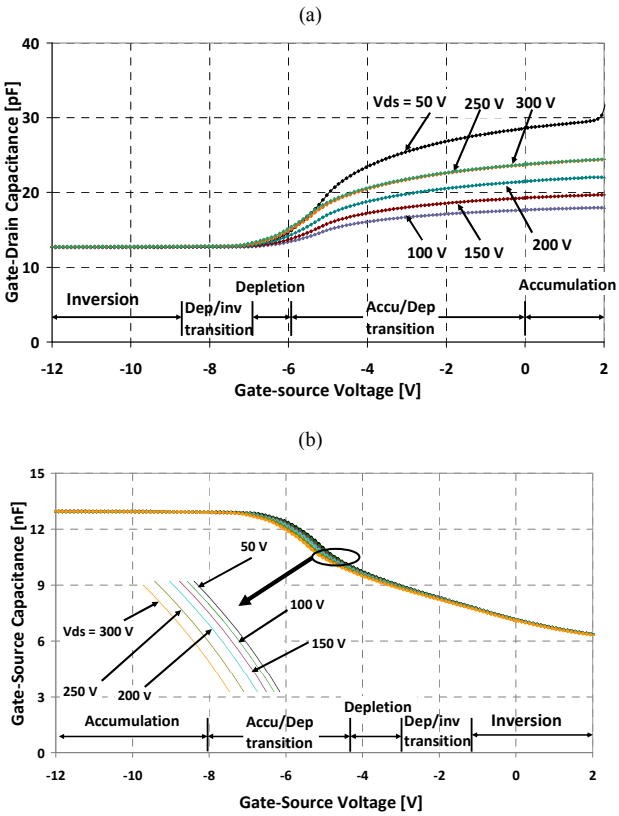



**Fig. 3** (a) Transition from the region of accumulation to depletion and then inversion of $C_{gd}$ with decreasing $V_{gs}$. Notice that the curves overlap for $V_{ds}$ = 250 V and 300 V; (b) transition from the region of accumulation to depletion and then inversion of $C_{gs}$ with increasing $V_{gs}$.

For an n-type MOSFET, when $V_{gs} > 0$ , the gate-drain overlap is in *accumulation* (see Fig. 3 (a)). Upon applying a small amount of negative gate voltage, the gate-drain overlap will move from *accumulation* to *depletion*. As $V_{gs}$ decreases towards -12 V, it will eventually go to *inversion* where the number of minority carriers remains fixed. This explains why

the capacitance value for $C_{gd}$ stays constant as shown in Fig. 3 (a). On the other hand, due to the overlap between the gate and the p-base, the behavior of $C_{gs}$ is the opposite of that of $C_{gd}$ as a function of the gate bias $V_{gs}$ as shown in Fig. 3 (b). As $V_{gs}$ decreases from 2 V to -12 V, the p-base surface goes from *inversion* to *depletion* and eventually to *accumulation*.

## III. Derivation of Model Equations

In many publications, model equations used to calculate capacitances usually take $V_{ds}$ as the independent variable (x-axis), with $V_{gs}$ as a parameter which only appears in the boundary conditions [12, 14]. Thus, it is not possible to calculate capacitances as a function of $V_{gs}$ using these model equations. Furthermore model validation is even less practical.

$V_{gs}$ must be explicitly included in the model equations of inter-electrode capacitances rather than accounted for as a boundary condition. However, it is relatively easy to establish a simple model based on the delta-depletion formulation [15], which is a rather crude representation. This is demonstrated in Fig. 4; the dotted curve (a) represents the simulation result from the first-order delta-depletion theory by assuming the depletion threshold voltage ($V_{TD}$) set to 4 V. The simple model does not work well in the neighborhood of the transition points when going from accumulation to depletion.

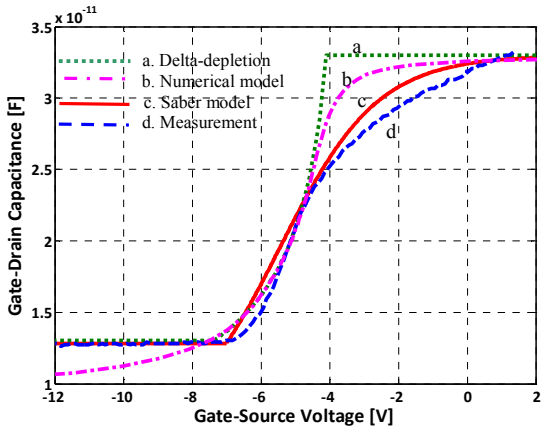



**Fig. 4** Comparision of (a) the delta-depletion model (dotted), (b) the numerical model (dash-dot), (c) the simplified model simulation (solid), and (d) the measured (dashed) $C_{gd}$ versus $V_{gs}$ curves of a 650 V, 60 A CoolMOS™ for drain-source voltage at 50 V.

The model presented in this paper is based on deriving the actual charge distribution inside the MOS transistor. The general capacitance formula including the a.c. inversion layer polarization effect was derived by Brews [13]. Model equations employed here are generic and applicable to all insulator-semiconductor systems [16].

### A. Device Physics Equations

The expressions for the charge density, electric field, and potential as a function of position inside the semiconductor are obtained by solving Poisson's equation in one dimension [13, 15]. The physical parameters used in the calculation including doping concentration in the drift region ($N_d$) and oxide layer thickness ($t_{ox}$) were extracted as a first step using the Hefner model [14]. The capacitance-voltage (CV) relationships for an ideal n-type MOS transistor are given as:

$$C = \frac{C_{ox\_eff}(V_{ds})}{1+\left(\frac{K_o W_{eff}}{K_s x_o}\right)} \tag{2}$$

where $C_{ox\_eff}$ is the effective oxide capacitance as a function of $V_{ds}$, and the effective depletion width is given as

$$W_{eff} = \begin{cases} \hat{U}_s A_D L_D \left[\dfrac{2F(U_s,U_F)}{e^{U_F}\left(1-e^{-Us}\right)+e^{-U_F}\left(e^{Us}-1\right)}\right] & \ldots\text{acc/depl (3.1)} \\ \dfrac{\sqrt{2}A_D L_D}{\left(e^{U_F}+e^{-U_F}\right)^{1/2}} & \ldots\text{flat band (3.2)} \\ \hat{U}_s A_D L_D \left[\dfrac{2F(U_s,U_F)}{e^{-U_F}\left(1-e^{Us}\right)+e^{U_F}\left(e^{-Us}-1\right)/(1+\Delta)}\right] & \ldots\text{depl/inv (3.3)} \end{cases}$$

where $A_D$ is a fitting parameter for $W_{eff}$, and

$$\Delta = \frac{\left(e^{-Us}+U_s-1\right)/F(U_s,U_F)}{\int_{Us}^{0}\dfrac{e^{-U_F}\left(e^{U}-1\right)\left(e^{-U}+U-1\right)}{2F^3(U,U_F)}dU}. \tag{4}$$

The dimensionless semiconductor surface electric field $F(U_s,U_F)$ is defined by

$$F(U_s,U_F)=\sqrt{e^{U_F}\left(e^{-U_s}+U_s-1\right)+e^{-U_F}\left(e^{U_s}-U_s-1\right)}. \tag{5}$$

$U_s$ and $U_F$ are the normalized potentials, defined by $U_s = q\phi_s/kT$ and $U_F = q\phi_F/kT$, where $\phi_s$ is the surface potential and $\phi_F = (kT/q)\ln(n_i/N_d)$ is the Fermi potential. The symbol $\hat{U}_s$ is defined by $\hat{U}_s$ = 1, for $U_s > 0$; and $\hat{U}_s$ = -1, for $U_s < 0$. The intrinsic Debye length $L_D$ is given as

$$L_D = \sqrt{K_s \varepsilon_0 kT \Big/ 2q^2 n_i} \tag{6}$$

where $K_s$ is the dielectric constant for Si, and $\varepsilon_0$ is the permittivity of free space. The gate voltage is related to the oxide voltage, the surface potential, and the flat-band voltage $V_{FB}$ through the relationship

$$V_{GS} = V_{FB} + \phi_s + \hat{U_s} \frac{kTK_s t_{ox} F(U_s, U_F)}{qK_o L_D} \quad (7)$$

where $K_O$ is the dielectric constant for the oxide and $t_{ox}$ is the thickness of the oxide layer.

It should be noted that Eqs. (3) and (4) are only valid for n-type semiconductors, which are used to calculate $C_{gd}$ for the n-drain CoolMOS™ transistor in this paper. These two equations need to be modified to be used for p-type devices, and the modified equations must be used to calculate $C_{gs}$ for the CoolMOS™ transistor due to the presence of p-bases in the source region [15].

### *B. Numerical Model for CoolMOS™*

The above equations were first implemented in Matlab™+ to compare the model predictions with measured data in order to evaluate their accuracy and applicability to the CoolMOS™ transistor. The capacitance cannot be expressed explicitly as a function of $V_{gs}$ as shown in Eqs. (2) to (7). In Matlab™, a numerical method has to be used to solve the problem by assuming a set of $U_s$ values.

In Fig. 4, the dash-dotted curve (b) shows the simulated curve of $C_{gd}$ using the numerical approach for $Vds = 50$ V. It exhibits better agreement with the measured data especially in the neighborhood of the transition points going from accumulation to depletion where simple delta-depletion analysis fails. This validates the accuracy of the theoretical equations derived from the exact charge distribution analysis.

### *C. Saber Model for CoolMOS™*

Although the above theoretical equations were validated using Matlab™ through comparison with experiment, they are not ready to be implemented in Saber for circuit simulation due to the complexity of model Eqs. ((4), (5), and (7)). Simplification and linearization need to be performed to reduce the numerical complexity while improving the functional accuracy of the device capacitances with the help of some free parameters. Furthermore, the analysis is conducted for accumulation, depletion and, inversion as shown in the following sub-sections, respectively.

#### *C.1 Model Equation Linearization*

From the circuit perspective, $V_{gs}$ is the voltage reference that circuit designers use. However, from the device physics point of view the surface potential, $U_s$, is the one used in the above equations to calculate capacitances. These two variables are related through Eq. (7) but in an implicit form through the function $F(U_s, U_F)$, which depends on $U_s$ in both exponential and linear form described in Eq. (5). The linearization of $F(U_s, U_F)$ is critical in order to express Eq. (7) in an explicit form that can be coded into Saber.

+ Matlab software is a trademark of MathWorks Inc.

A typical variation of $F(U_s, U_F)$ as a function of $U_s$ is shown in Fig. 5 for the CoolMOS™ transistor in the n-drain region with $N_d$ = 1e15 cm$^{-3}$. $U_F$ is calculated to be -11.5 with this $N_d$. In the accumulation region, the values of $U_s$ are positive (see Fig. 5) and $V_{gs} > V_{FBD}$. With negative $U_F$ and positive $U_s$, the term $e^{-U_F}\left(e^{U_s} - U_s - 1\right)$ is much larger than the other term $e^{U_F}\left(e^{-U_s} + U_s - 1\right)$ in Eq. (5). So, in the accumulation region, $F(U_s, U_F)$ can be written as

$$F(U_s, U_F) \approx \sqrt{e^{-U_F}\left(e^{U_s} - U_s - 1\right)}. \quad (8)$$

The exponential term ($e^{U_s}$) in (8) can be expressed through Taylor series for further linearization in the form of

$$e^{U_s} = 1 + U_s + \frac{U_s^2}{2!} + \cdots \frac{U_s^n}{n!} \quad . \quad (9)$$

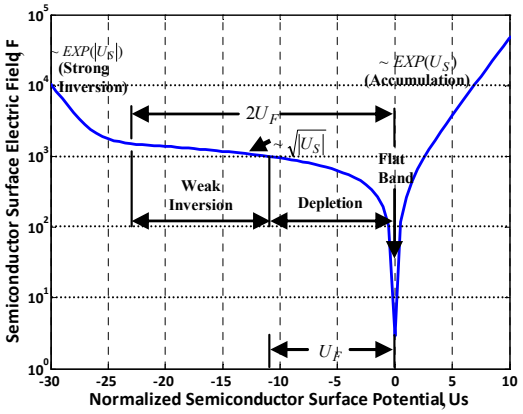



**Fig. 5** Relationship between the dimensionless semiconductor surface electric field F and the normalized semiconductor surface potential $U_s$ in log scale for n-drain device.

By combining Eq. (8) and Eq. (9) (first three terms only), $F(U_s, U_F)$ can be linearized and then substituted into Eq. (7) which is reorganized as

$$U_s = \frac{V_{gs} - V_{FB}}{B_D\left(\frac{kT}{q}\right)\left(1 + \frac{K}{\sqrt{2}}\right)} \quad (10)$$

where $K = \frac{K_s \cdot t_{ox}\sqrt{e^{-U_F}}}{K_o \cdot L_D}$ is a constant and $B_D$ is the fitting parameter in the linearization process.

#### *C.2 Saber Model Refinement*

The above linearization is conducted for the accumulation and the transition from accumulation to depletion regions where $U_s > 0$ (or $V_{gs} > V_{FBD}$). Through Eq. (10), a set of $U_s$

values can be calculated corresponding to the measured $V_{gs}$ values, instead of assuming a set of predefined $U_s$ values in the numerical model. Equation (3.1) was employed to find the values of $W_{eff}$ which were used to calculate the capacitance values through Eq. (2) for the accumulation case. It should be noted that at $U_s = 0$ (or $V_{gs} = V_{FBD}$), Eq. (3.2) must be employed to calculate $W_{eff\_FB}$ which only depends on constant physical parameters (i.e., $U_F$ and $L_D$).

Once $V_{gs}$ drops below $V_{FB}$, the n-drain surface changes to depletion/inversion with negative $U_s$. It can be seen from the measured data (dashed curve (d)) in Fig. 4 that the capacitance remains constant in the depletion/inversion region. This is because the relatively sluggish generation-recombination process will not be able to supply or eliminate minority carriers in response to the applied a.c. signal. The number of minority carriers in the inversion layer therefore remains fixed at its d.c. value, and $W_{eff}$ simply is well approximated by constant $W_{eff\_FB}$ [16]. This makes $C(inv) = C(FB) =$ constant by having a constant $W_{eff}$ for all depletion/inversion biases. The above analysis simplifies the equation used in the numerical model and reduces the numerical complexity of solving Eq. (3.3), which requires integration.

The above discussion and development of the model equations is focused on calculation of $C_{gd}$ for the CoolMOS™ transistor with an n-type drift region. It should be noted that the behavior of $C_{gs}$ is opposite to $C_{gd}$ as a function of $U_s$. For $C_{gs}$, it is in accumulation, when $U_s < 0$ (or $V_{gs} < V_{FBS}$), and moves to depletion/inversion, when $U_s > 0$ (or $V_{gs} > V_{FBS}$). Therefore, some modifications are needed before applying the same approach and linearization technique which was used for $C_{gd}$ to calculate values for $C_{gs}$.

$C_{ds}$ is modeled by the standard delta-depletion because it simply changes with $V_{ds}$, given as

$$C_{ds} = \frac{C_{jo}}{\left(1 - \frac{V_{ds}}{V_{\delta}}\right)^{m}} \tag{11}$$

where $C_{j0}$ is the zero-bias junction capacitance, $V_{\delta}$ is the junction potential, and $m$ is the grading coefficient.

An overall Saber-compatible model can now be constructed by combining the results of the foregoing analysis of accumulation, depletion, and inversion regions. In Fig. 4, the solid line shows the simulated curve of $C_{gd}$ using the Saber model for $V_{ds}$ = 50 V, which exhibits excellent agreement in the full range with the measured data. Notice that the Saber model obtained much better accuracy than the numerical model in the neighborhood of the transition points going from accumulation to depletion. This is due to the inclusion of fitting parameters $A_D$, $A_S$, $B_D$, and $B_S$ give the Saber model more flexibility to better match the measured data.

## IV. Model Parameters

Table I lists the primary model parameters that were used for modeling the inter-electrode capacitance for CoolMOS™ in Saber. These parameters are derived and extracted from measurements. Parameters $C_{oxd\_eff}$ and $C_{oxs\_eff}$ are the effective gate-drain and gate-source oxide capacitances, which decrease monotonically with increasing $V_{ds}$ because of the depletion region developed by the gate-to-drain voltage. And their capacitance values can be extracted directly from the measured CV curves at small positive $V_{gs}$ values. $U_{FD}$ and $U_{FS}$ are physical parameters which can be calculated from the semiconductor doping concentration.

Table I
Primary model parameters used for inter-electrode capacitances.

| | Model Parameter | Comments |
|---|---|---|
| $C_{gd}$ | $C_{oxd\_eff}$ | Gate-drain effective oxide capacitance |
| | $V_{FBD}$ | Drain flat band voltage |
| | $A_D$ | Effective depletion width fitting parameter for drain |
| | $B_D$ | Linearization fitting parameter for drain |
| | $U_{FD}$ | Normalized Fermi potential for drain |
| $C_{gs}$ | $C_{oxs\_eff}$ | Gate-source effective oxide capacitance |
| | $V_{FBS}$ | Source flat band voltage |
| | $A_S$ | Effective depletion width fitting parameter for source |
| | $B_S$ | Linearization fitting parameter for source |
| | $U_{FS}$ | Normalized Fermi potential for source |
| $C_{ds}$ | $C_{j0}$ | Zero-bias junction capacitance |
| | $V_{\delta}$ | Junction potential |
| | m | Grading coefficient |

The two fitting parameters $A_D$ and $A_S$ are employed to correct a deviation in the lateral depletion behavior that is caused by the n- and p- super-junctions in the drift region. The CoolMOS™ transistor exhibits very nonlinear behavior in the nonconducting state [1]. This is a result of the lateral electric field that builds up, which drives the charge towards the contact region. Therefore, extreme care must be exercised when extracting model parameters, because they must make the simulation curves work continuously under all bias conditions. As described in subsection (C.1) of section III, another two fitting parameters $B_D$ and $B_S$ are employed because of the linearization of Eq. (7) for $C_{gd}$ and $C_{gs}$, respectively.

## V. Model Validation

Both static and transient validations of the Si CoolMOS™ transistor are demonstrated. The results illustrate a very good agreement between the measured data and the simulated results as shown below.

### A. *Model Capacitance Results*

The results for the measured and modeled $C_{gd}$ values are plotted versus $V_{gs}$ with $V_{ds}$ as a parameter in Fig. 6. The good agreement over such a large range of bias conditions validates the accuracy of the new modeling approach as seen from Fig. 6 (a) where $V_{ds}$ ranges from 0 V to 40 V; and (b) where $V_{ds}$ ranges from 50 V to 300 V. For a particular small positive $V_{gs}$ value, $C_{gd}$ decreases monotonically with increasing $V_{ds}$, due to the depletion region developed by the gate-to-drain voltage [10].

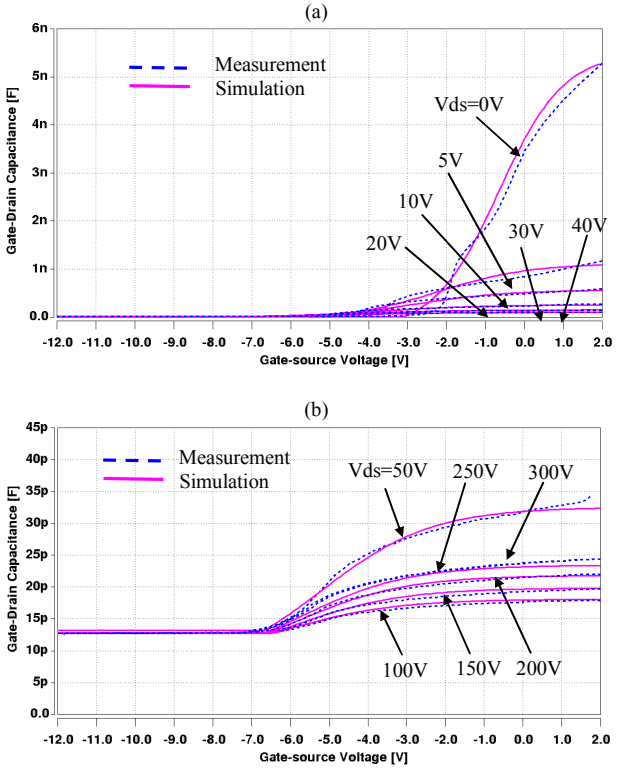



**Fig. 6** Gate-Drain capacitance versus gate-source voltage of the 650 V, 60 A (0.57 cm$^2$) CoolMOS$^{TM}$ at 25 $^oC$ for drain-source voltage (a) at 0 V, 5V, 10 V, 20 V, 30 V, and 40 V; and (b) at 50 V, 100 V, 150 V, 200 V, 250 V, and 300 V.

Fig. 7 shows the model (solid) and measured (dashed) $C_{gd}$ curves with $V_{ds}$ on the horizontal axis and $V_{gs}$ as the stepping parameter. Because the curves remain consistent for the high-bias range, they are condensed for $V_{ds}$ between 60 V to 300 V in order to show more details in the low-bias range as seen from Fig. 7. Notice that the $C_{gd}$ curve peak at non-zero $V_{ds}$ for $V_{gs} \leq -3$ V. This feature is due to the variation of $V_{FB}$ for different $V_{ds}$ (see Fig. 5 (a)).

Fig. 8 is a comparison of the measured (dashed) and simulated (solid) $C_{gs}$ values over a range of bias conditions that were obtained by sweeping $V_{gs}$ from 2 V to -12 V and stepping $V_{ds}$ from 50 V to 300 V. In this plot the onset of drain inversion at negative $V_{gs}$ results in a large increase of $C_{gs}$ as is expected from standard MOS theory [10].

Fig. 9 shows simulated (solid) and measured (dashed) $C_{ds}$ curves as a function of $V_{ds}$. Measured results indicate that $C_{ds}$ does not vary much with $V_{gs}$. The step in the measured data is reproduced in the simulation data at approximately the same $V_{ds}$. Most likely, this step feature is due to the full depleted in the p strip.

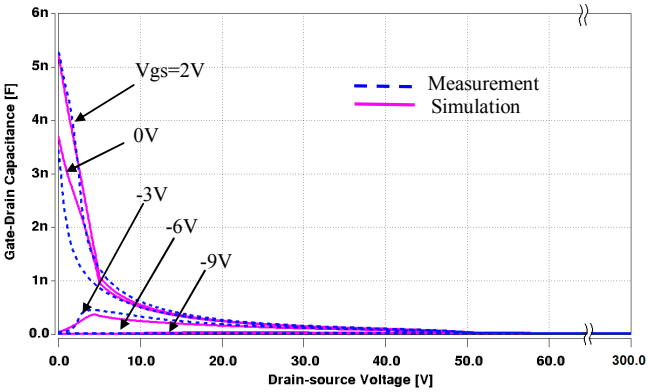



**Fig. 7** Gate-Drain capacitance versus drain-source voltage of the 650 V, 60 A (0.57 cm$^2$) CoolMOS$^{TM}$ transistor at 25 $^oC$ for drain-source voltage sweeping from 0 V to 300 V by condensing $V_{ds}$ between 60 V to 300 V.

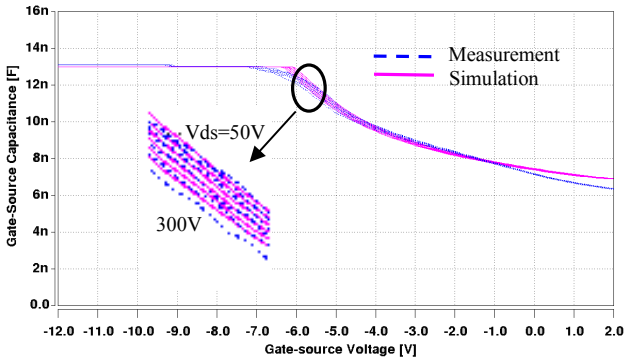



**Fig. 8** Gate-Source capacitance versus gate-source voltage of the 650 V, 60 A (0.57 cm$^2$) CoolMOS$^{TM}$ transistor at 25 $^oC$ for drain-source voltage at 50 V, 100 V, 150 V, 200 V, 250 V, and 300 V with zoomed-in plot.

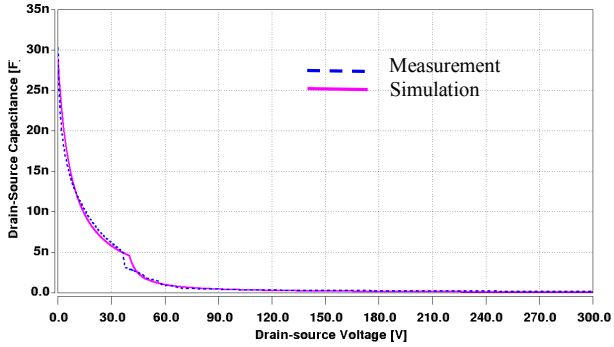



**Fig. 9** Drain-Source capacitance versus drain-source voltage of the 650 V, 60 A (0.57 cm$^2$) CoolMOS$^{TM}$ transistor at 25 $^oC$.

## B. *Gate-charge Characterization*

The previous results have mainly demonstrated the model validation in the non-conducting state. Fig. 10 shows the comparison between measured data and the simulated data for gate charge characterization.

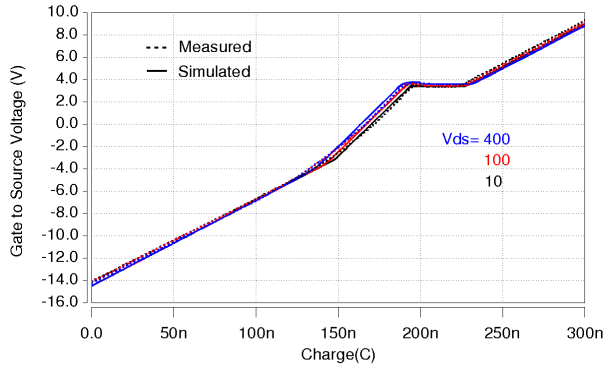


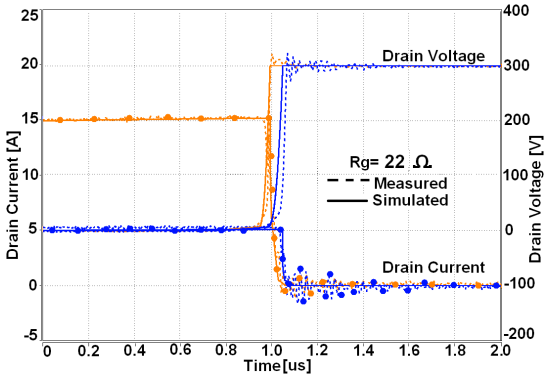

**Fig. 10** Gate charge results of the 650 V, 60 A (0.57 cm$^2$) CoolMOS$^{TM}$ transistor at 25 $^{o}$C.

## C. *Inductive Switching Tests*

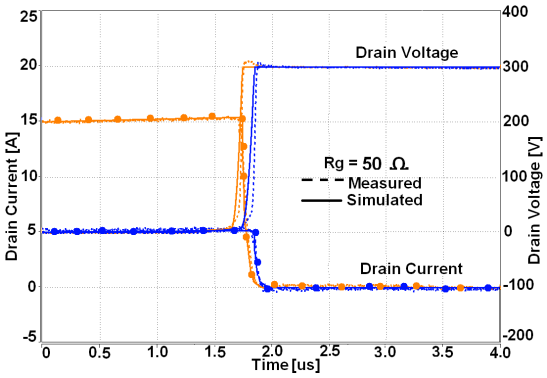
Inductive switching tests were performed using a well-characterized double-pulse test system. In the beginning, the CoolMOS$^{TM}$ body diode was used as the freewheeling diode in the test circuit. However, it introduced excessive noise during device turn-on, which eventually damaged both devices unexpectedly when the test was being performed beyond the 100 V level. A commercial Si Schottky diode (600 V, 55 A) was then employed as the freewheeling diode, and it performed adequately for the rest of the switching tests.

The gate resistor $R_g$ was varied to provide different turn-off speeds for the devices. Fig. 11 shows the simulated (solid) and measured (dashed) inductive switching turn-off waveforms of the drain current (with dots) at 5 A and 15 A, respectively, and the drain voltage clamped at 300 V at 25 $^{o}$C for (a) $R_g$ = 22 Ω; (b) $R_g$ = 50 Ω; and (c) $R_g$ = 75 Ω. Fig. 12 illustrates the comparison between the measured data and the simulated data for the gate voltage (top) as well as the drain current at 15 A and the drain voltage at 300 V (bottom) using three different $R_g$ (22 Ω, 50 Ω, and 75 Ω) at 25 $^{o}$C.

(a)




(b)




(c)

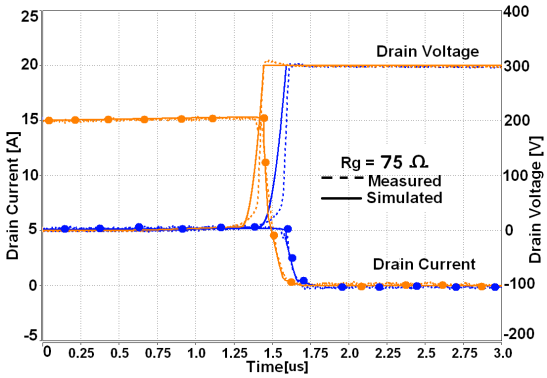



**Fig. 11** Simulated (solid) and measured (dashed) inductive switching turn-off waveforms of drain current (dotted) and drain voltage at 25 $^{o}$C for (a) $R_g$ = 22 Ω; (b) $R_g$ = 50 Ω; and (c) $R_g$ = 75 Ω.

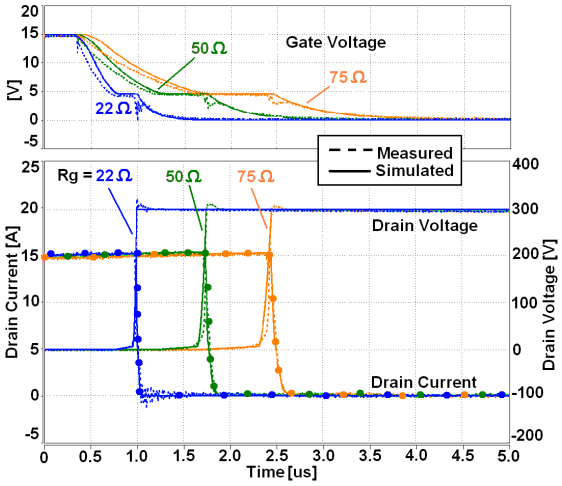



**Fig. 12** Simulated (solid) and measured (dashed) inductive load switching waveforms of gate voltage (top); and drain current at 15 A (with dots) and drain voltage at 300 V for $R_g$ = 22 Ω, 50 Ω, and 75 Ω at 25 °C.

## VI. Conclusion

An enhanced method for modeling the inter-electrode capacitances of super-junction power MOSFET devices has been developed and validated with experimental results. By working with the actual charge distribution inside the CoolMOS™ capacitors [13], a numerical model was established as a first step. Further simplifications and linearization were then performed to transfer the numerical model into a Saber-compatible model that even improves the accuracy, especially in the transition range from *accumulation* to *depletion*. The comparison between the simulated data with the measured results validates the accuracy of the new physical model.

## References


[1] L. Lorenz, G. Deboy, A. Knapp, and M. Marz, "CoolMOS™—A new milestone in high voltage power MOS," in *Proc. ISPSD*, 1999, p.3.

[2] G. Deboy, M. Marz, J. P. Stengl, H. Strack, J. Tihanyi, and H. Weber, "A new generation of high voltage MOSFETs breaks the limits of silicon," in *IEDM Tech. Dig.*, 1998, p. 683.

[3] P. Sun, J. Lai, H. Qian, W. Yu, C. Smith, and J. Bates, "High efficiency three-phase soft-switching inverter for electric vehicle drives," Vehicle Power and Propulsion Conference, 2009. VPPC '09. IEEE, pp. 761-766.

[4] W. Yu, H, Qian, and J. Lai, "Design of high-efficiency bidirectional DC-DC converter and high-precision efficiency measurement," Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE, pp. 685-690.

[5] P. Ralston, T. Duong, N. Yang, D. Berning, C. Hood, A. Hefner, and K. Meehan, "High-voltage capacitance measurement system for SiC power MOSFETs," in *Energy Conversion Congress and Exposition*, 2009. *ECCE*, pp. 1472-1479.

[6] P. O. Lauritzen, "Power semiconductor device models for use in circuit simulators," in *IEEE IAS Meeting Conf. Record*, Oct. 1990, pp. 1559-1563.

[7] M. I. Simas, M. S. Piedade, and J. C. Freire, "Characterization of power MOSFET's in high commutation level," in *PESC'88 Record*, pp.667-673.

[8] C. H. Xu and D. Schroeder, "Modeling and simulation of power MOSFET's and power diodes," in *1988 PESC Conference Proceeding*, pp. 76-83.

[9] C-E. Cordonnier, "SPICE model for TMOS," Motorola Application note AN1043, 1989.

[10] R. S. Scott and G. A. Franz, "An accurate model for power DMOSFET including interelectrode capacitance," in *1990 PESC Conference Proceeding*, pp. 113-119.

[11] I. Budihardjo and P. Lauritzen, "The lumped-charge power MOSFET model, including parameter extraction," *IEEE Transactions on Power Electronics*, Vol. **10**, 1995, pp. 379-387.

[12] K. Shenai, "A circuit simulation model for high-frequency power MOSFET's" *IEEE Transactions on Power Electronics*, Vol. **6**, 1991, pp. 539-547.

[13] J. R. Brews, "An improved high-frequency MOS capacitance formula," *Journal of Applied Physics*, Vol. **45**, 1974, pp. 1276-1279.

[14] T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and S. H. Ryu, "Silicon carbide power MOSFET model and parameter extraction sequence," IEEE Trans. Power Electronics, vol. 22, no. 2, pp. 353-362, March 2007

[15] R. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley, 1996.

[16] D. Schroder, *Semiconductor Material and Device Characterization*, Wiley-Interscience, 2006