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Fabrication, characterization and simulation of high performance Si nanowire-based non-volatile memory cells

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Abstract
We report the fabrication, characterization and simulation of Si nanowire SONOS-like non-volatile memory with HfO_2 charge trapping layers of varying thicknesses. The memory cells, which are fabricated by self-aligning *in situ* grown Si nanowires, exhibit high performance, i.e. fast program/erase operations, long retention time and good endurance. The effect of the trapping layer thickness of the nanowire memory cells has been experimentally measured and studied by simulation. As the thickness of HfO_2 increases from 5 to 30 nm, the charge trap density increases as expected, while the program/erase speed and retention remain the same. These data indicate that the electric field across the tunneling oxide is not affected by HfO_2 thickness, which is in good agreement with simulation results. Our work also shows that the Omega gate structure improves the program speed and retention time for memory applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Semiconductor memory is essential for information processing as it occupies more than half of the floor space in a modern microprocessor. As a key part of silicon technology, semiconductor memory has been continuously scaled to achieve higher density and better performance in accordance with Moore's law. Semiconductor non-volatile memory (NVM), a major subset of solid-state memory, can retain information when the power is removed. Among a variety of NVM technologies, Flash memory has the advantages of high density, low power consumption and excellent portability. The small size of Flash memory cells ensures a low cost per bit in a commodity memory business, and its memory architecture has overcome many of the scaling and reliability issues during the early development of electrically reprogrammable non-volatile semiconductor memories. Consequently, for a long period of time Flash memory has been the dominant form of NVM in terms of production volume and magnitude of sales dollars.

Flash memory may reach fundamental scaling limits, however, because a thick tunneling oxide is required to prevent charge leakage and achieve 10 years' retention. Such a thick tunneling oxide requires high programming/erasing voltages to charge/discharge the floating gates. Relatively large transistor sizes are required for the isolation of the applied high gate voltages which consumes significant areas for the peripheral circuitry and limits the area available to the memory array. In addition, as memory cell separation is reduced, low gate coupling and serious floating gate interference will significantly degrade circuit performance [1–3]. As Flash memory approaches its scaling limit, several alternative strategies have been proposed to extend or replace

the current Flash memory technology. For example, memory technologies that use low internal programming voltages, such as ferroelectric, magnetic and resistance change memories, are being developed [4–6]. These approaches are revolutionary, but major challenges must be overcome to achieve small memory size and aggressive technology design architecture.

One of the most promising candidates for future non-volatile memory applications when the CMOS scaling extends to and beyond the 22 nm node is the silicon–oxide–nitride–oxide–silicon (SONOS) charge trapping memory. For SONOS memory, the conventional polysilicon floating gate charge storage medium is replaced by silicon nitride (SiN), where the charge is stored in spatially isolated deep level traps. Difficult Flash challenges, maintaining the gate coupling ratio and reducing the neighboring cell cross-talk, may be resolved by using such charge trapping memories [7].

In addition to the engineering of trapping layers, the device performance can also be improved by using innovative non-planar channel geometries. Low-dimensional materials (LDM), such as nanotubes and nanowires, have properties that may enable their use as potential solutions for future devices. For example, semiconductor nanowires enable surrounding gate structures for more effective electrostatic control. Among the various nanostructure materials, silicon nanowire (SiNW) has induced great scientific interest as possible building blocks for future nanoelectronic circuitry. The replacement of a bulk silicon channel in planar metal–oxide–semiconductor field-effect transistors (MOSFETs) by SiNWs will reduce short channel effects and enhance the device performance [8].

In this work, SONOS-like NVM memory cells based on self-assembled SiNWs and HfO_2 trapping layers have been fabricated, characterized and simulated. The memory cells exhibit excellent fast program/erase operations, long retention time and good endurance. Figure 1 shows the three-dimensional schematic of the fabricated memory cell. The SiNW channel offers an efficient surrounding gate structure, which significantly reduces the short channel effects. It has been shown that the 'natural length' λ of a surrounding gate transistor, which corresponds to the minimum gate length to prevent short channel effects, logarithmically depends on the oxide thickness [9, 10]. Therefore the channel length of a surrounding gate nanowire field effect transistor can be shorter than in a planar transistor where the natural length has a square root dependence on the oxide thickness. In addition to the lateral scaling, the surrounding gate structure makes it possible to scale the channel length without the need to reduce the gate oxide thickness significantly, which improves charge retention. Moreover, the surrounding gate structure enhances the electric field in the tunneling oxide region which leads to faster operational speed, low operational voltage and low power consumption in memory applications (section 4). In this study HfO_2 is used as the charge trapping layer instead of the SiN layer used conventionally in the SONOS devices. An HfO_2 trapping layer has several advantages over the traditional SiN trapping layer. Figure 2 shows the band diagram at program and erase conditions for both HfO_2 and SiN SONOS-like memory cells. During the program operation where the modified Fowler–Nordheim tunneling dominates, the electrons must tunnel through a thicker energy barrier in the nitride cell than in the HfO_2 cell. Hence, electron tunneling and charge storage will be easier in HfO_2 devices, leading to a faster write time. However, during an erase operation, the holes must tunnel through a much thicker barrier to the HfO_2 valence band, as compared to the SiN case, which may slow down the erase speed. Since the holes are minimally involved in the erase operation, the net positive charge in the HfO_2 trapping layer is limited and the over-erase problem is minimized [11]. Therefore, there is a tradeoff between solving the over-erase problem and reduced erase speed.

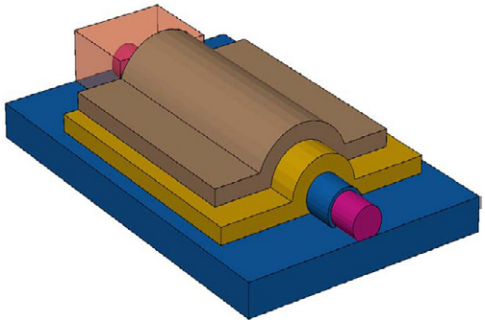

Figure 1. 3D schematic of the resulting device (cut along the channel width direction). The SiNW channel is surrounded by tunneling oxide, charge trapping layer and blocking oxide, respectively. The far end of the SiNW is covered by a metal layer as the source/drain contact.

2. Memory cell fabrication

Memory cells were fabricated by using a self-assembly-based process, similar to one used in our previous research on SiNW $SiO_2/HfO_2/SiO_2$ [12] and SONOS cells [13]. The essential steps are as follows: first, a layer of thermal SiO_2 was grown by dry oxidation on a silicon wafer. On top of the oxide, the SiNWs were grown from an Au catalyst in pre-defined locations by low pressure chemical vapor deposition. The SiNWs were grown at 500 mTorr (of SiH_4) and 440 °C. Following this step, tunneling SiO_2 ($\approx$3 nm) was grown by dry oxidation on the SiNWs. Then the Al source/drain electrodes were patterned on the nanowires. Layers of HfO_2 and Al_2O_3 were deposited on the nanowire to form the charge trapping layer and the blocking oxide by atomic layer deposition. The last step was the formation of Al gate electrodes. This hybrid process combines self-assembly and photolithography to achieve large-scale integration and clean SiNW/dielectric interfaces for better electrical properties compared to devices formed by using common nanowire device fabrication processes which depend on microfluidic and electrophoresis alignment [14]. An SEM (scanning electron microscopy) picture of a typical SiNW NVM cell with a 5 μm gate length is shown in figure 3(a). Figure 3(b) shows a transmission electron microscopy (TEM) image of the cross section of a typical memory cell, which indicates that the gate dielectric stack almost completely surrounds the SiNW channel. To evaluate the effect of trapping layer thickness, four memory cells (H1–H4) with different HfO_2 thicknesses were fabricated: H1 (5 nm), H2 (10 nm), H3 (20 nm) and

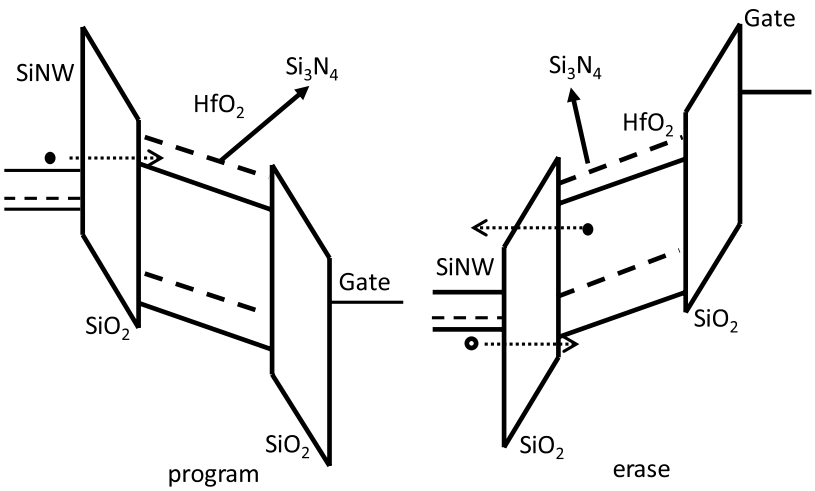

Figure 2. Energy band diagram under program and erase conditions for both SiN and HfO_2 memory cells.

H4 (30 nm). In the experiment, the tunneling oxide and the blocking oxide were fixed at 4 nm and 20 nm, respectively.

3. Electrical characterization

Figure 4 shows the transfer current–voltage (I_D–V_G) characteristics of cells H1–H4 in the initial state (i.e. HfO_2 is neutral) and the programmed state (i.e. HfO_2 is charged negative). The SiNW memory cells exhibit p-MOSFET I–V characteristics as reported previously [12]. The four memory cells have similar (but not identical) threshold voltages, as seen from these initial state I–V curves. The programmed state threshold voltage shift was measured after applying a 3 s pulse of +14 V on the gate, which is long enough to see the difference between the four cells. I–V curves before and after the programming operations have the same subthreshold slope value (∼80 mV/dec), indicating that the threshold voltage shift is not due to interface states but due to the fixed charges in the HfO_2 layer. The memory windows are 3.0 V, 3.6 V, 4.3 V and 4.5 V for cells H1–H4, respectively. This window variation is expected because the areal charge trap density (number of traps per unit area) increases with HfO_2 thickness; therefore, the thicker the HfO_2 layer, the larger the threshold voltage shift for these long programming times. The programmed threshold voltage of cell H4 is only slightly larger than H3 because the electron traps in the thicker HfO_2 layer in H4 are not completely charged at this program voltage and time.

The programming/erasing (P/E) speed characterizations (i.e. threshold voltage shift (ΔVTH) versus P/E time) are shown in figure 5. As shown in figure 5(a), the slopes of the threshold voltage shifts versus P/E time become steeper as the P/E voltages increase, indicating faster P/E speeds. The electric field across the tunneling oxide increases with the P/E voltage, resulting in an increased electron tunneling flow from the nanowire channel to the HfO_2 layer. As shown in figure 5(b), the four cells H1–H4 have approximately the same memory window within a P/E time range from 100 ns to 10 ms. Despite the difference in HfO_2 thickness, all the cells (H1–H4) have similar P/E speed. As the P/E time further increases, the cell with a thicker HfO_2 (and subsequently more charge traps) exhibits a larger threshold voltage shift, as illustrated in figure 4. At these longer program times, the charge is limited by the total number of traps available in the HfO_2 layer. It is also noted that the erase speed is slightly slower

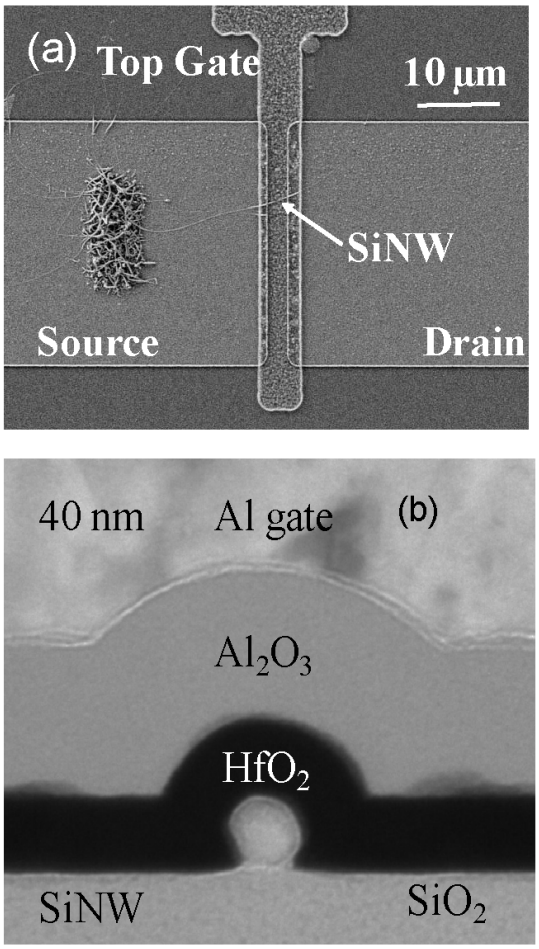

Figure 3. (a) Top view SEM image of a typical SiNW memory cell. (b) Transmission electron microscopy of a typical cell's cross section: dielectric stacks almost completely surround the Si nanowire channel.

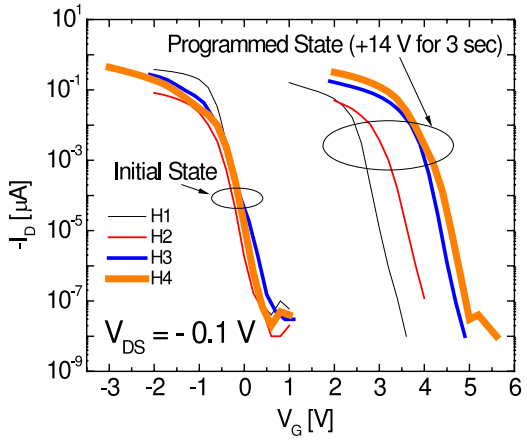

Figure 4. Transfer I–V characteristics of memory cells at initial and programmed states. The programmed states were achieved by applying +14 V bias at the gate and 0 V at the source and drain for 3 s.

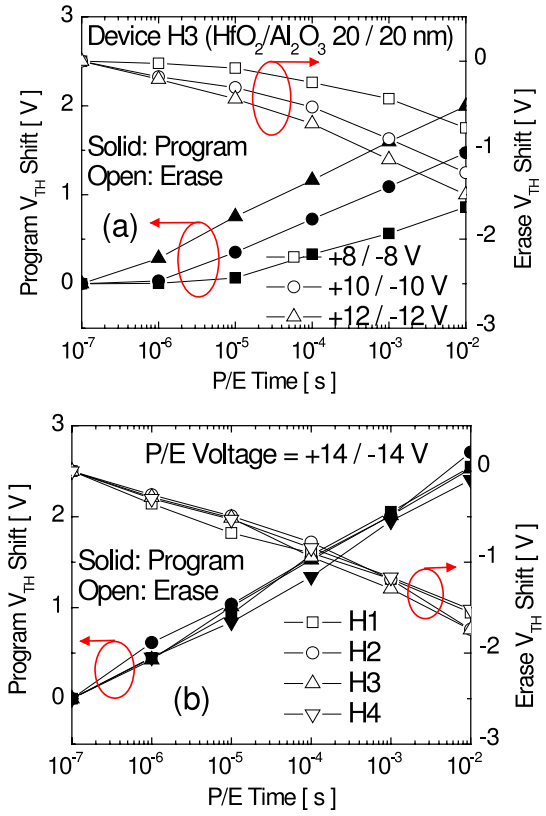

Figure 5. (a) Programming and erasing speed characterization (threshold voltage shift versus P/E time) of cell H3 at different P/E voltages. (b) P/E speed characterization of cells H1–H4 at P/E voltage = 14 V.

than the programming speed, which arises from the higher hole tunneling energy barrier during erase operation [11].

To investigate why the four cells with different HfO_2 thicknesses have the same P/E speed, a numerical simulation of the electric field profile was carried out by using the Synopsys Sentaurus TCAD device simulator[5]. Figure 6(a) shows the

[5] Certain commercial equipment, instruments or materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is neither intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

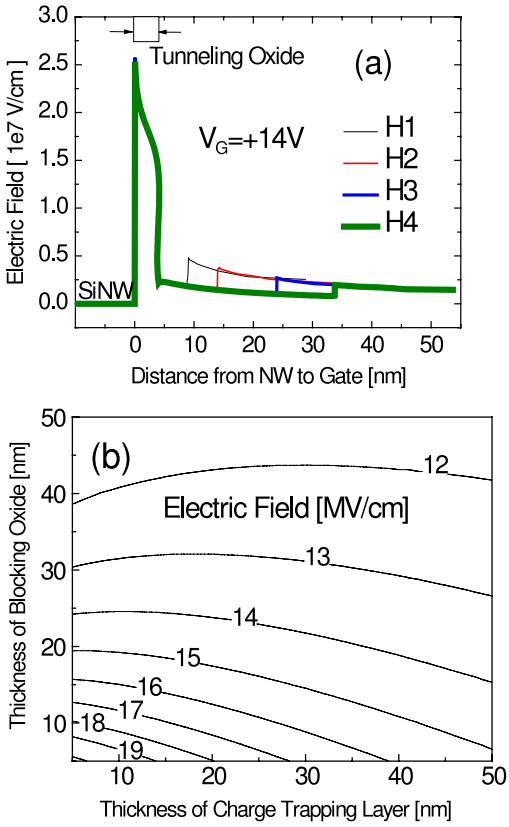

Figure 6. (a) Simulated electric field profiles of cells H1–H4: the four cells have almost the same electric field at the interface between SiNW and tunneling oxide. (b) Simulated contour plots of the electric field at the interface between SiNW and tunneling oxide as a function of the trapping layer (HfO_2) and blocking oxide thickness. The electric field only weakly depends on HfO_2 thickness.

simulated electric field profiles of cells H1–H4, with a V_G = +14 V of programming voltage. The simulation accounts for the electric field immediately before tunneling begins. It does not include tunneling or account for the charges trapping in the HfO_2. Simulations such as this one can lead to artificially large instantaneous electric fields [15]. Experimentally, tunneling begins at lower fields as the programming voltage is applied, leading to a lowering of the electric field across the SiO_2 tunneling barrier due to the charges trapped in the HfO_2 layer. As shown in figure 6(b), this simulation clearly illustrates that the tunneling electric fields across the SiO_2 tunneling barrier of the four cells are comparable, leading to the same tunneling current. While the tunneling electric field profile is relatively insensitive to the HfO_2 thickness, it is predicted to strongly depend on the blocking oxide thickness in this structure. One can therefore infer that about the same amount of charge is stored in the HfO_2 for all four cells for the same P/E pulse (for relatively short pulses). The capacitance between the charge trap centers and the metal gate is dominated by the capacitance of the Al_2O_3 blocking oxide (which is the same for all four cells and much less than that of the HfO_2 layer);

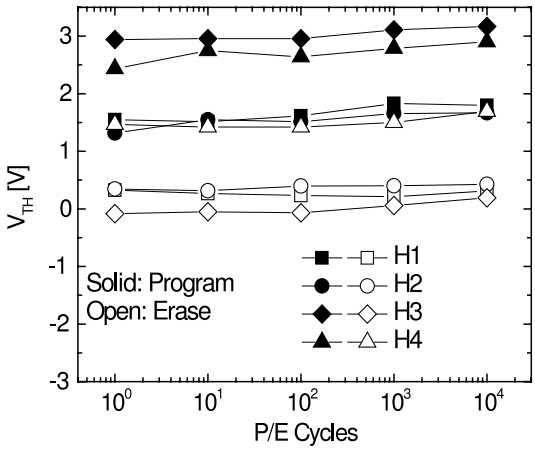

Figure 7. Memory endurance characteristic of cells H1–H4 at room temperature. The memory windows are almost unchanged after 10^4 P/E cycles.

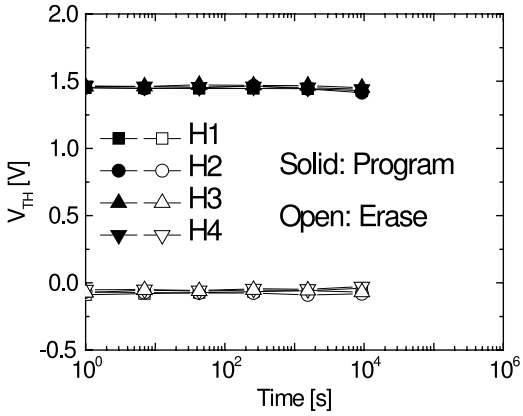

Figure 8. Memory retention characteristic of cells H1–H4 at room temperature. A 1.5 V memory window is almost unchanged after 10^4 s. The projected memory window in 10 year retention is 1.3 V.

thus the same amount of charge stored in the HfO_2 trap centers will result in the same threshold voltage shift for all four cells. Simulation results support this conclusion as does the measured data shown in figure 5.

Figure 7 shows the cell endurance where a slight upward shift of the threshold voltage is observed for both programmed and erased states after a number of P/E cycles. The cells maintain the same memory window (with no noticeable degradation) after 10^4 P/E cycles. The program and erase pulses are +8 V for 1 ms and −8 V for 10 ms, respectively. The upward shift of V_{TH} may be due to accumulation of electrons trapped in residual deep traps in the HfO_2 layer. Figure 8 shows the excellent retention capability of cells H1–H4. All four cells retained the same memory window for the duration of 10^4 s. This is attributed to the high quality of the silicon dioxide tunneling barriers, which were thermally grown on the intrinsic SiNWs. It is noted that charge degradation occurs in the cell with thin HfO_2 when the memory window is larger than 3.0 V (data not shown). This is attributed to the high internal electric field across the tunneling oxide that arises when there is a large electron density in the HfO_2 layer.

4. Numerical simulation analysis and design

We have studied the SiNW NVM cells by fabrication and characterization in sections 1 and 2. In this section, theoretical modeling and numerical simulations that account for charge trapping/detrapping effects and the carrier tunneling effects are carried out to further study the program/erase speed and retention capability both in terms of trapping material and device structure. The simulated geometries are not intended to directly model the experimental devices but are chosen to elucidate the underlying physical mechanisms and demonstrate possible device performance characteristics in these nanowire charge trapping devices.

The schematic cross section of the two-dimensional double-gate (DG) charge trapping memory device used in the simulations is shown in figure 9(a). The n-channel memory cell consists of a tunneling oxide, a charge trapping layer (nitride

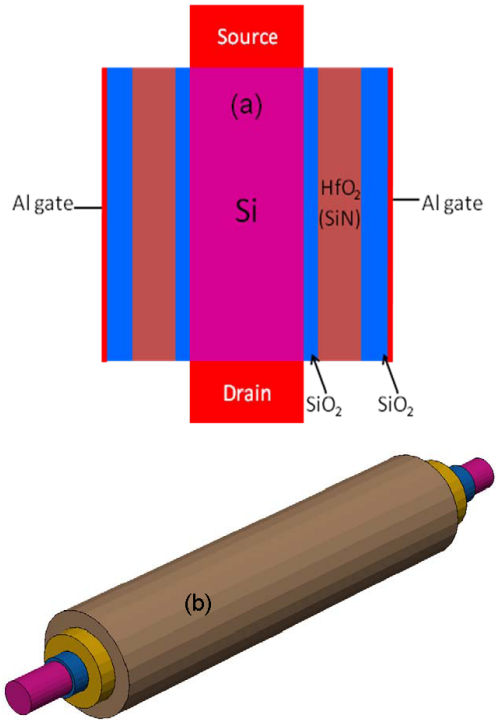

Figure 9. Schematic of the devices under investigation by numerical simulation. (a) Double-gate (DG) memory cell. (b) Gate-all-around (GAA) memory cell. Both devices have the exact same cross-section view along the channel length direction.

or hafnium oxide, 8 nm) and blocking oxide (4 nm) between the channel and metal gate. The tunneling oxide material is SiO_2. Instead of Al_2O_3, SiO_2 is employed as the blocking oxide material in order to simplify the simulation process. The three-dimensional gate-all-around (GAA) device used in the simulation is shown in figure 9(b). Figure 9(a) can also be viewed as the cross-section view of the GAA structure of figure 9(b) along the channel length direction.

In order to study the time evolution of program/erase and retention processes in the memory devices, a physics-based model has been developed to describe electron/hole tunneling across the tunneling oxide and blocking oxide, as well as carrier dynamics, and trapping/detrapping in the

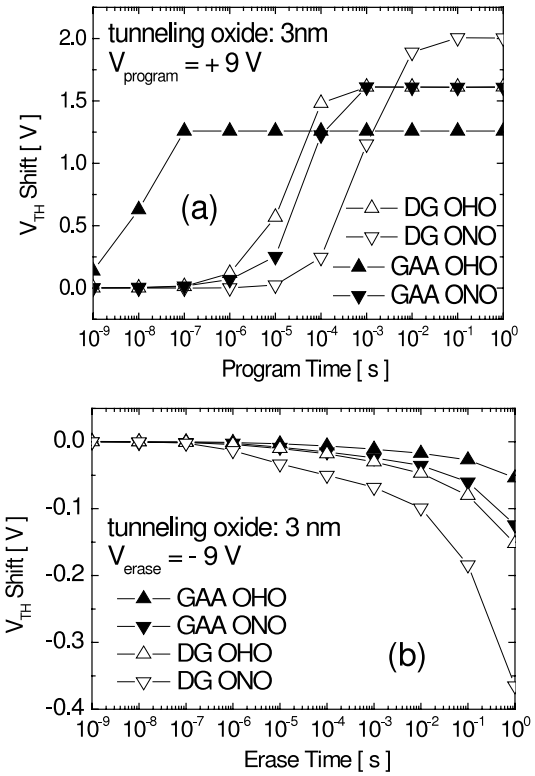

Figure 10. Simulated (a) program and (b) erase characterization for each memory cell with 3 nm of tunneling oxide.

charge trapping layer (based upon the Shockley–Read–Hall recombination model). The tunneling oxide and blocking oxide were considered as pure tunneling barriers (with no traps). It has been reported that the electron trap level is 1 eV in SiN [16, 17]. In this study, for comparison purposes, the electron trap levels are defined as 1 eV below the conduction band, while the hole trap levels are defined as 1 eV above the valence band in the charge trapping layers (SiN or HfO_2). Only local trap capture and emission is taken into account. The continuity equation for electrons, holes and trapped carriers has been numerically solved coupled with Poisson's equation under time-dependent condition by using a Sentaurus device simulator (see footnote 5). A fully intrinsic (backward-Euler) approach, which is known to be stable irrespective of the time discretization, is used with an automatic selection of the time step.

The simulated program and erase behavior for both DG and GAA memory cells with the gate voltage at ± 9 V are shown in figure 10. As shown in figure 10(a), the HfO_2 memory cells exhibit faster program speed and slightly smaller threshold voltage shifts than the SiN cells, with similar device structure. However, figure 10(b) indicates that the erase speeds of HfO_2 cells are much slower than those of SiN cells. The improved program speed and degraded erase speed of HfO_2 memory cells arise from the band structure differences as discussed earlier (figure 2). Furthermore, it is found that erase speeds are much slower than program speeds in all memory cells simulated in this work, which is consistent with the experimental results presented above. During an erase operation, the electrons in the deep levels are not readily detrapped. It should be noted that hole tunneling from the silicon to the charge trapping layer (HfO_2) is unlikely due to the larger barrier height for holes (4.6 eV) compared to that of electrons (3.1 eV).

The electric field and energy band profiles of the DG and GAA memory cells with the gate biased at +9 V were simulated just before the commencement of the program operation. As plotted in figure 11(a), the cylindrical geometry enhances the electric field at the tunneling oxide/nanowire interface between the SiNW and tunneling oxide. The electrical field at the interface is about 1.5 times higher in the GAA cell with respect to the planar DG cell, enhancing carrier injection and program speed. On the other hand, the GAA structure depresses the electric field in the blocking oxide, preventing the hole injection from the gate electrode and electron tunneling from the storage node. By using a cylindrical geometry, a high electric field is generated at the $Si–SiO_2$ interface, enhancing electron tunneling across the gate stack without degrading the retention time. In addition, as shown in figure 11(b), the barrier width experienced by electrons during the program operation decreases from 3 to 2 nm. Because the tunneling probability exponentially depends on the width of the barrier through which the electron tunnels, the cylindrical GAA cell has a high carrier tunneling efficiency, exhibiting a much faster program speed than the planar DG device, as illustrated in figure 10(a). Due to the geometry in these simulations, the gate capacitance of the DG structures is smaller than in the comparable GAA structures. When the trapping layers are fully charged, the DG devices have a larger threshold voltage shift as shown in figure 10(a).

As plotted in figure 10(b), the simulated erase characteristics show that the DG cells are slightly better than the GAA cells. As shown in figure 11(c), the erase electric field of the DG cells is higher than that of the GAA cells; therefore the DG cells have a faster erase speed. For those NVM cells, the trapping layers are fully filled with electrons before the erase operation. As shown in the comparison between figures 11 (a) and (c), the erase electric field is much lower than the program electric field. This is because the stored charges in the trapping layer isolate the electric field applied by the external erasing gate bias, leading to a lower electric field during the erase operation.

During the retention, the electric field across the tunneling oxide is very small and the accumulation layer hole density is negligible; there is no significant hole tunneling into the trapping layer. Hence only electron detrapping to the conduction band and tunneling back into the channel are considered. Figure 12(a) shows the effect of varying the tunneling oxide thickness on the retention characteristics of GAA memory cells with an 8 nm HfO_2 trapping layer. This is expected because the retention capability depends on the tunneling oxide thickness due to the tunneling distance. As plotted in figure 12(b), the HfO_2 cells are predicted to have a longer retention time than the SiN devices due to the deeper trap levels, which can be easily explained by the energy band offset in figure 2. These simulations also predict that GAA cells have better retention capability than DG cells. As illustrated in figure 12(c), the electric field across the tunneling

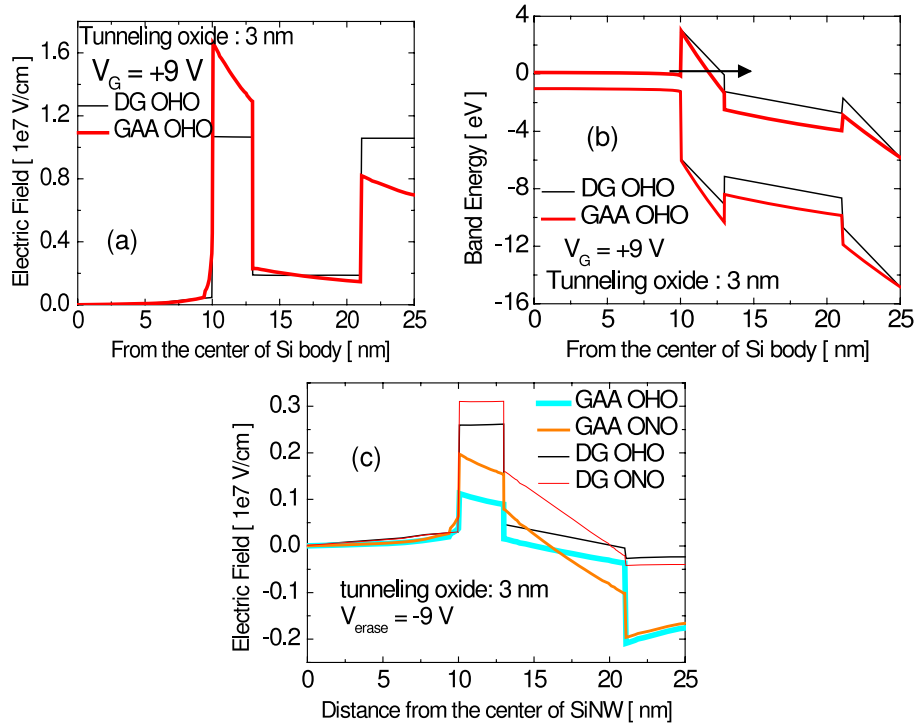

Figure 11. (a) Simulated electric field and (b) energy band profiles of the DG and GAA structures with HfO_2 trapping layer at program voltage = +9 V. (c) Simulated electric field at erase voltage = −9 V for each cell when the trapping layers are fully filled by electrons.

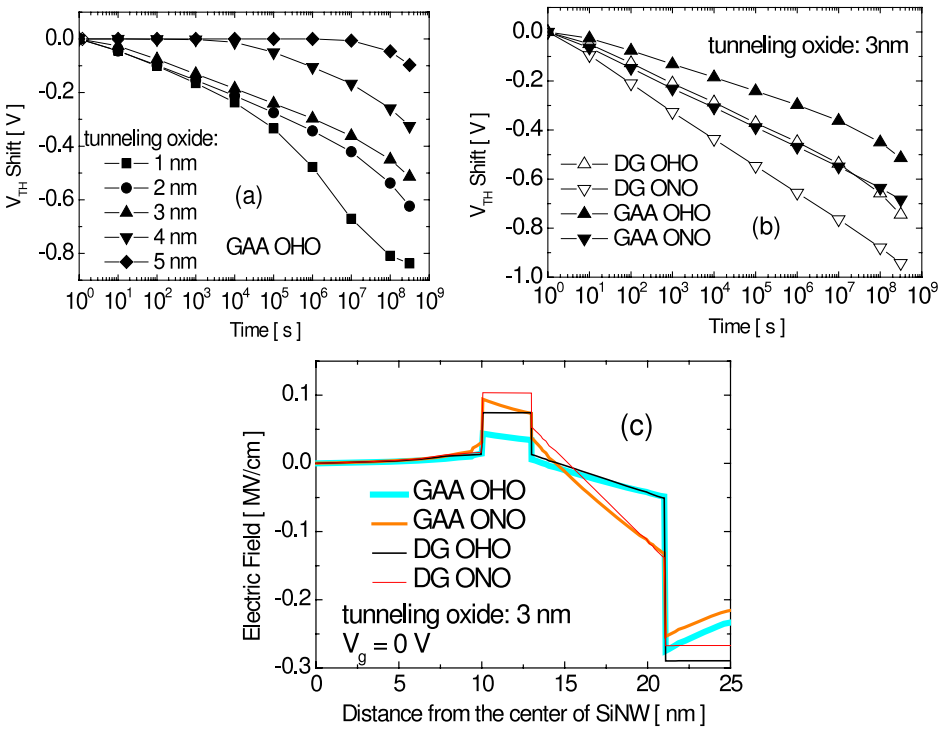

Figure 12. Simulated retention characterizations of memory cells with (a) different tunneling oxide thickness and (b) different device structure. (c) Simulated electric fields when gates are grounded.

oxide of GAA cells is much lower due to the cylindrical geometry.

Generally, the program/erase speed of Flash-like memory is much slower than SRAM or DRAM, which can be programmed/erased at nanosecond speeds. In order to replace these fast volatile memories (the local memory) in the microprocessor, the Flash-like NVM should be able to be programmed/erased in nanoseconds or less. Several solutions has been proposed to improve the program/erase speed without reduced tunneling oxide thickness and high

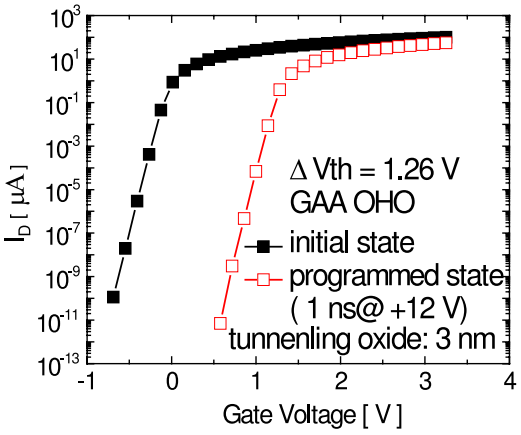

Figure 13. Simulated initial and programmed states of GAA memory cell with HfO_2 trapping layer.

program voltage, while maintaining sufficient performance and reliability [18, 19]. Our simulation result shows that a GAA SiNW memory cell with an HfO_2 trapping layer has a fast program speed at the nanosecond level. This is because the GAA structure and high-*k* charge trapping layer significantly enhance the electric field in the tunneling oxide region. Figure 13 shows the simulated initial and programmed states of a GAA memory cell with an HfO_2 trapping layer. A memory window of 1.26 V and a high on/off current ratio of 10^{13} are obtained after programming at +12 V for 1 ns. The threshold voltage shift between the two states is large enough to be identified as two discrete levels by the sense amplifier. By using a novel erase mechanism based on increased hole generation via impact ionization, fast erase operations can be obtained, overcoming the slow erase characteristics described above [20]. These simulations show that the NVM cells with a nanowire cylindrical GAA structure and HfO_2 trapping layer could be attractive for next-generation fast memory cells.

5. Conclusions

In this paper we studied high performance, novel non-volatile memory cells with an SiNW channel and $Al_2O_3/HfO_2/SiO_2$ gate insulation/storage stacks. Our results show that, by combining a gate-all-around structure with an SiNW channel and an HfO_2 charge storage layer, non-volatile memory characteristics are significantly improved relative to more traditional planar structures. While varying the thickness of the HfO_2 changes the charge trap density, the HfO_2 thickness does not affect the P/E speed and the retention times. Modeling predicts that this Si nanowire Flash-like NVM could be programmed with memory windows larger than 1 V by nanosecond, 12 V write pulses. Due to the intrinsic scalability of self-assembled nanowires and the advantage of the gate-all-around structure, a nanowire SONOS-like memory with HfO_2 charge storage layer may be a strong candidate for next-generation electronics.

Acknowledgments

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