Wafer-level Hall Measurement on SiC MOSFET

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Mobility is the indicator of the intrinsic performance of MOSFETs. An important question during the development of MOSFETs with new materials is that "What is the best achievable mobility?" However, mobility measurements are not simple, particularly when the gate dielectric and its interface are full of defects that can trap charges. SiC based MOSFETs are certainly in this category. The often-reported quantity, effective mobility, is misleading because it significantly over estimates the inversion charge [1]. However, the Hall mobility (μ_{Hall}) measurement is free from this problem since only free electrons in the channel contribute. Consequently, Hall mobility measurements are widely used in the study of SiC MOSFETs to imply various properties of the device quality [2-4].

Hall mobility measurements are very useful but tedious. In addition to a bulky, expensive and dedicated setup, wafer dicing, wire bonding and device packaging inhibit frequent measurements. A wide-ranging survey using large number of samples requires heroic measurement efforts. In this work, we demonstrate a wafer-level Hall measurement method, which requires neither packaging nor the specialized Hall measurement system. This method greatly reduces the efforts needed for Hall measurements and makes device characterization and development more convenient.

In these experiments, a donut-shaped permanent magnet with 3 mm inner diameter is placed, using a micro-positioner, above the device under test to provide the magnetic field (the device is placed directly under the center hole of the magnet). Fig. 1 shows a schematic of this setup. The distance of the magnet from the wafer can be adjusted with 25 μm resolution. The magnetic field as a function of distance is calibrated by a small (0.016 mm^2 active area) Hall Sensor. The maximum field this magnet can provide is approximately 3200 Gauss. 4H-SiC MOS-gated Van der Pauw/Hall bar structures, are used for this work. The size of the gated area is 150 μm × 150 μm.

In order to get μ_{Hall}, inversion sheet charge density (n_s) and sheet resistance (R_s) are measured separately. In the n_s measurement, the gate is kept at a certain potential, the source and substrate are grounded and the drain voltage is modulated from 0.2 V to 0.4 V by a 127 Hz voltage pulse with $t_{rise} = t_{fall} = 300$ μs. The differential voltage between the two Hall terminals is measured using a differential amplifier (10 MΩ input impedance) and monitored with an oscilloscope. The source current is monitored at the same time. This setup is shown in Fig. 2. The advantage of using drain voltage AC modulation is that the noise due to instrumentation can be averaged out within a short period of time. Consequently, the properties of the device under test are less likely to drift during the measurements. This is especially important when measuring SiC MOSFETs, which are known to have significant as-processed charge trapping and de-trapping [5].

Since the structure cannot be perfectly symmetric, the differential voltage measured contains the offset voltage, as expressed in equation (1) where V_{diff} is the voltage difference between the Hall terminals, V_o is the offset voltage, B is the magnetic field, I is the drain or source current and q is the electron charge. Fig. 3 plots I_s and V_{diff} (AC coupled) corresponding to the drain voltage modulation. As the magnetic field increases, the voltage difference between the two flat regions (dV_{diff}) gets larger. Fig. 4 plots dV_{diff}/dI as a function of B field. According to equation (2) the inversion sheet charge density n_s can be directly extracted from the slope of Fig. 4.

$$V_{diff} = V_o + \frac{BI}{qn_s} \quad (1), \qquad \frac{dV_{diff}}{dI} = \frac{dV_o}{dI} + \frac{B}{qn_s} \quad (2)$$

R_s is measured using Van der Pauw procedures. In Fig. 5, R_s and n_s are plotted as a function of gate voltage. The Hall mobility can be calculated from $\mu_{Hall}=1/(qn_sR_s)$. Fig. 6 shows the Hall mobility as a function of gate bias. It is almost independent of the gate voltage in the range investigated. This is not the expected behavior of a MOSFET with few defects in the gate dielectric and its interface. On the other hand, similar gate bias dependencies of Hall mobility have been reported on SiC devices measured by regular Hall systems [1, 2]. The measured mobility is very small compared to bulk value. In contrast to Si MOSFETs, the inversion-layer mobility of SiC MOSFETs is limited by factors other than acoustic-phonon scattering. Under such a condition, the usual expectations in Si MOSFETs do not apply.

In summary, we have demonstrated a wafer-level Hall measurement method that does not require any wafer dicing, wire bonding, packaging nor the regular Hall measurement system. This method makes the device characterization and development more convenient.

References

[1] N.S. Saks et al, Applied Physics Letters, **77**, 3281-3283 (2000).
[2] T. Hatakeyama et al, Materials Science Forum, **483-485**, 829-832 (2005).
[3] V. Tilak et al, IEEE Transactions on Electron Devices, **54**, 2823-2829 (2007).
[4] N.S. Saks et al, Applied Physics Letters, **80**, 3219-3221 (2002).
[5] M. Gurfinkel et al, IEEE Transactions on Electron Devices, **55**, 2004-2012 (2008).

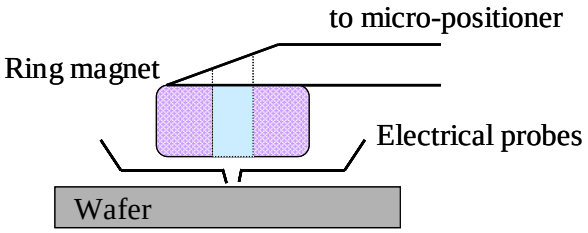

Fig. 1. Wafer-level Hall measurement setup. The magnetic field is provided by a permanent ring magnet. The distance from the wafer is controlled by a micro-positioner.

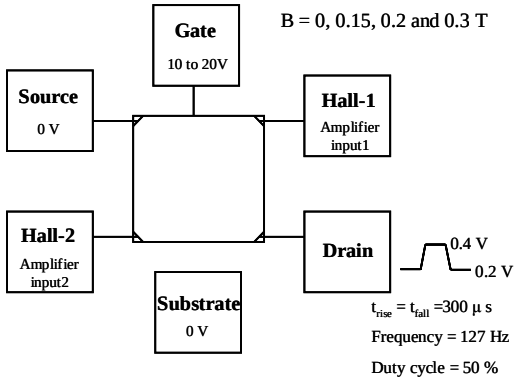

Fig. 2. The 4H-SiC Van der Pauw structure measured, which has an active gate area of 150 μm × 150 μm. The setup shown here is for the inversion sheet charge density (n_s) measurement.

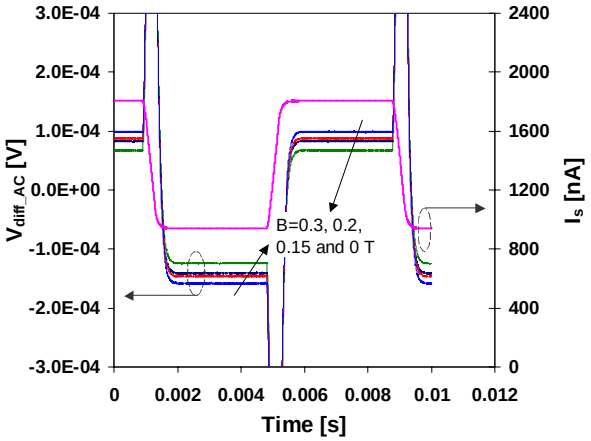

Fig. 3. Source current and AC coupled differential voltage corresponding to the drain voltage modulation. Four magnetic fields are used. As B increases, dV_{diff} gets larger.

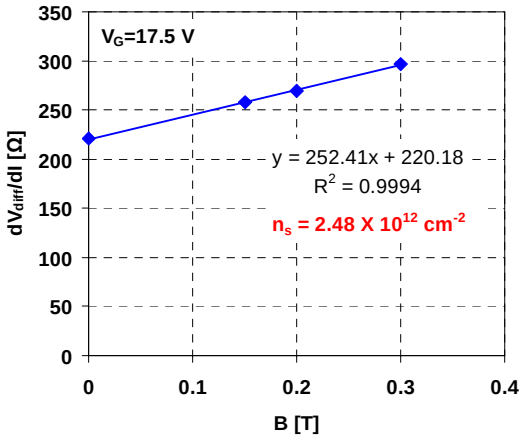

Fig. 4. Inversion sheet charge density (n_s) extraction at V_G=17.5 V.

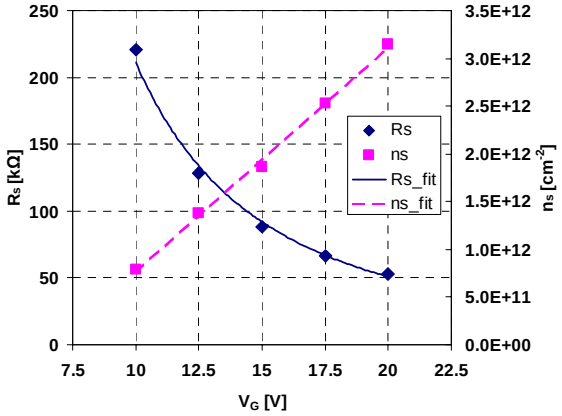

Fig. 5. Sheet resistance and inversion sheet charge density measured at different gate voltages.

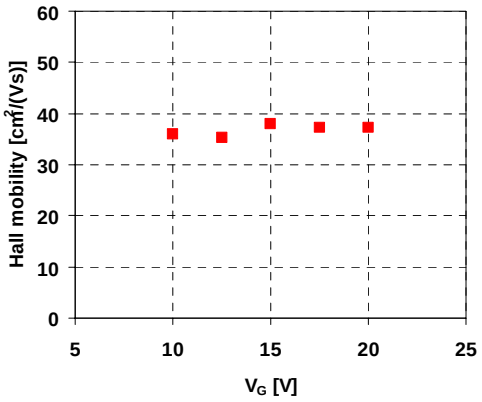

Fig. 6. Hall mobility calculated from R_s and n_s as a function of gate voltage.