Demonstration of a Wafer-level Hall-Mobility Measurement Technique

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In this work, we demonstrated a wafer-level Hall-mobility measurement technique that allows for a rapid survey of many devices. We further explore the possibility of extending this technique into a fast-pulsed Hall measurement to investigate the transient behavior of mobility.

Accurate characterization of channel inversion mobility is important for understanding carrier transport in MOSFETs. In the development of advanced/novel devices, such as high-k based MOSFETs, III-V channel material based devices, or even SiC power MOSFETs, improving channel mobility is often the first and foremost challenge. The ability to measure mobility accurately is the prerequisite for a clear understanding on the degradation mechanisms. Split-CV is the most frequently used mobility measurement method. It is not an easy measurement and its accuracy decreases when the device is ultra small[1] or when there is a high level of charge-trapping[2]. While correction methods exist for split-CV in those situations[1,2], the complexity of implementation is further increased. Hall-mobility measurement is an appealing alternative which is immune to the aforementioned shortcomings. However, other than being used as a calibration for the corrected split C-V measurement[1], it is not often used. Regular Hall mobility measurements are tedious. In addition to a bulky, expensive and dedicated setup, wafer dicing, wire bonding and device packaging inhibit frequent measurements. Any wide-ranging survey using a large number of samples requires a heroic measurement effort. In this work, we demonstrated a wafer-level Hall measurement method, which requires neither packaging nor a bulky/expensive system. It greatly reduces the efforts needed for Hall measurements and makes device characterization much more convenient. Using this technique, a fast pulse-gated Hall measurement is also possible, opening a new way to study the transient charge-trapping behavior in the gate dielectric and its interface.

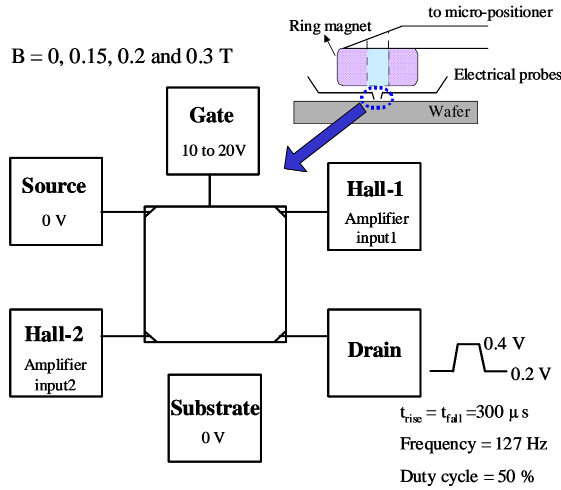

Fig. 1 Wafer-level Hall measurement set-up for the inversion sheet charge density (n_s). 4H-SiC gated Van der Pauw structure is used, which has an active gate area of 150 µm × 150 µm.

In Hall measurements, a strong and uniform magnetic field is required. The key of our approach is the realization that such requirement can be satisfied by bringing a permanent magnet very close to the device. In our experiment, a donut-shaped permanent magnet with 3 mm inner diameter is placed above the device under test using a micro-positioner with high precision (25 µm resolution), as shown in the inset of Fig. 1. The relationship between the magnetic field and the vertical separation distance is calibrated by a small (0.016 mm^2 active area) Hall Sensor. The maximum field achievable is about 3200 Gauss. We utilize this Hall set-up to examine 4H-SiC MOS-gated Van der Pauw/Hall bar structures with 150 µm × 150 µm gated area.

In order to get μ_{Hall}, inversion sheet charge density (n_s) and sheet resistance (R_s) are measured separately. In the n_s measurement, the gate is kept at a certain potential, the source and substrate are grounded and the drain voltage is modulated from 0.2 V to 0.4 V by a 127 Hz square wave with $t_{rise} = t_{fall} = 300$ µs. The differential voltage between the two Hall terminals is measured using a differential amplifier (10 MΩ input impedance) and monitored with an oscilloscope along with the source current. The set-up is shown in Fig. 1. The use of drain voltage modulation allows the signal-to-noise ratio to be improved rapidly by averaging. The short measurement time prevents complications due to device drift during the measurements. This is especially important when measuring SiC MOSFETs, which are known to have significant as-processed charge trapping and de-trapping[3].

Fig. 2 shows the measured waveforms from the Hall terminals. The peaks at each transition are due to displacement current arising from some asymmetry in the device geometry. The asymmetry also produces an offset voltage in the measured differential voltage, as expressed in equation (1) where V_{diff} is the voltage difference between the Hall terminals, V_o is the offset voltage, B is the magnetic field, I is the drain or source current and q is the electron charge. While the voltage difference between the two flat regions (dV_{diff}) is the sum of the actual Hall voltage change and the offset voltage change, only the change of Hall voltage gets larger as the magnetic field increases. Measuring the voltage difference at a few magnetic fields can separate the two contributions. Fig. 3 plots dV_{diff}/dI as a function of B field. According to equation (2) the inversion sheet charge density n_s can be directly extracted from the slope in Fig. 3.

$$V_{diff} = V_o + \frac{BI}{qn_s} \quad (1), \qquad \frac{dV_{diff}}{dI} = \frac{dV_o}{dI} + \frac{B}{qn_s} \quad (2)$$

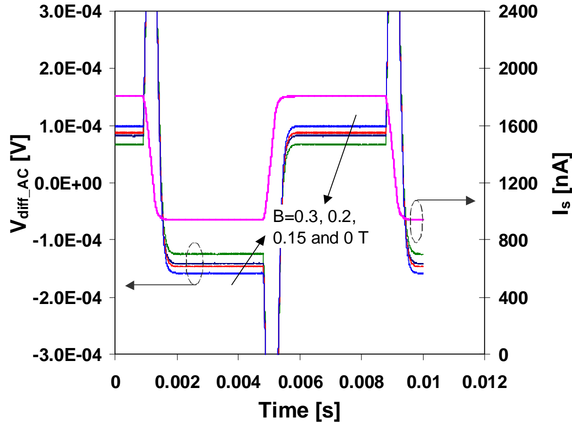

Fig. 2 Source current and AC coupled differential voltage corresponding to the drain voltage modulation. Four magnetic fields are used.

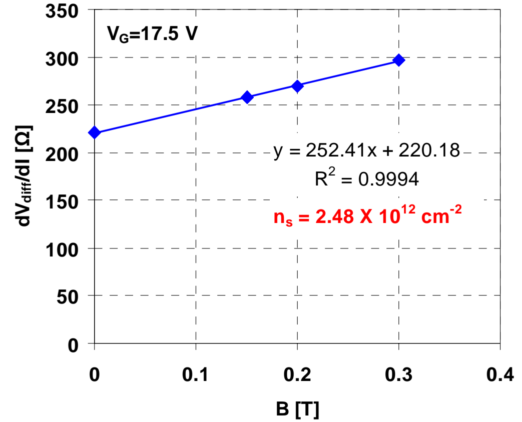

Fig. 3 Inversion sheet charge density (n_s) extraction at V_G=17.5 V.

R_s is measured using Van der Pauw procedures[4]. In Fig. 4, R_s and n_s are plotted as a function of gate voltage. The Hall mobility can be calculated from $\mu_{Hall}=1/(qn_sR_s)$. Fig. 5 shows the Hall mobility as a function of gate bias. It is not what one would expect for a high-quality MOSFET. It is almost independent of the gate voltage in the range investigated. Similar dependency has been reported on SiC devices measured by regular Hall systems[5]. The measured mobility is very small compared to the bulk value. This is also well known for SiC MOSFETs.

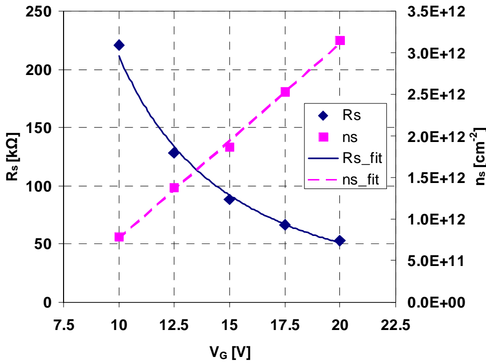

Fig. 4 Sheet resistance and inversion sheet charge density measured at different gate voltages.

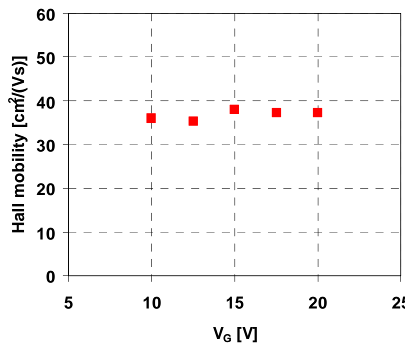

Fig. 5 Hall mobility calculated from R_s and n_s as a function of gate voltage.

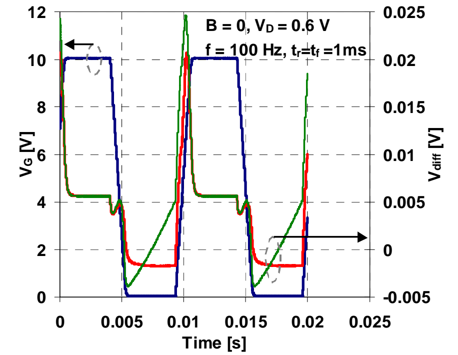

Fig. 6 V_{diff} corresponding to a V_G pulse. The two V_{diff} traces are measured with one-minute separation.

One can also pulse the gate instead of the drain in the Hall mobility measurement. High-speed pulsing can potentially allow us to use Hall mobility as a probe for transient charge-trapping. Fig. 6 shows the preliminary results of V_{diff} corresponding to a 100 Hz gate pulse from 0 to 10 V with rise and fall time of 1 ms. The two traces are measured with a one-minute separation. As discussed before, imperfection in device symmetry produces large displacement current induced peaks during switching and there is a long time constant associated with the V_{diff} when the device is off due to high channel resistance. Obviously, several modifications must be made before fast measurement is possible. Smaller devices will help reduce the transients and are currently being fabricated. Keeping the gate voltages above V_{th} can also help by avoiding very high channel resistance.

In summary, we have demonstrated a wafer-level Hall-mobility measurement method that does not require any wafer dicing, wire bonding, packaging nor the regular Hall measurement system. This method makes the device characterization and development much more convenient. With this method, transient behavior of the interaction between interface traps and channel carriers is studied by pulsing the gate. Modifications are suggested to further explorations.

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