A Fast, Simple Wafer-level Hall-Mobility Measurement Technique

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ABSTRACT

Mobility is a good indicator of device reliability. High channel mobility is one of the biggest challenges especially in novel devices such as high-k based MOSFET, III-V devices and SiC power MOSFET etc. Accurate measurement of channel mobility is required for studying the limiting mechanism of mobility. Hall mobility is more favorable than effective mobility or field effect mobility because it takes into account only the mobile charges, which is essential for measuring novel devices that have a very high trap density. However, regular Hall measurement involves a bulky system and tedious sample preparation, which inhibit frequent use. In this paper, we demonstrate a fast and easy to implement wafer-level Hall-mobility measurement technique that allows for large survey of many devices under various conditions.

INTRODUCTION

The performance and reliability of MOSFET are strongly limited by the quality of the gate-dielectric/substrate interface. Low quality interface can lead to shifted threshold voltage, high leakage current and low channel mobility. In the development of advanced/novel devices, such as high-k based MOSFETs, III-V channel material based devices, or even SiC power MOSFETs, improving channel mobility is often the first and foremost challenge. The ability to measure mobility accurately is the prerequisite for a clear understanding on the degradation mechanisms. Split-CV is the most frequently used mobility measurement method. It is not an easy measurement and its accuracy decreases when the device is ultra small [1] or when there is a high level of charge trapping [2]. While correction methods exist for split-CV in those situations [1,2], the complexity of implementation is further increased. Hall-mobility measurement is an appealing alternative, which is immune to the aforementioned shortcomings. However, other than being used as a calibration for the corrected split C-V measurement [1], it is not often used due to the expensive regular Hall measurement system and tedious sample preparation. In addition to a bulky, expensive and dedicated setup, wafer dicing, wire bonding and device packaging inhibit frequent measurements. Any wide-ranging survey using a large number of samples requires a heroic measurement effort. In this work, we demonstrated a wafer-level Hall measurement method, which requires neither packaging nor a bulky/expensive system. It greatly reduces the efforts needed for Hall measurements and makes device characterization much more convenient.

EXPERIMENT

In Hall measurements, a strong and uniform magnetic field is required. The key of our approach is the realization that such requirement can be satisfied by bringing a permanent magnet very close to the device. In our experiment, a donut-shaped permanent magnet with 3 mm inner diameter is placed above the device under test using a micro-positioner with high precision (25 μm resolution), as shown in the inset of Fig. 1. The area of the device is orders of magnitude smaller compared to the size of the permanent magnet, which allows the magnetic field to be very uniform across the device. By bringing the magnet very close to the device, a maximum field of

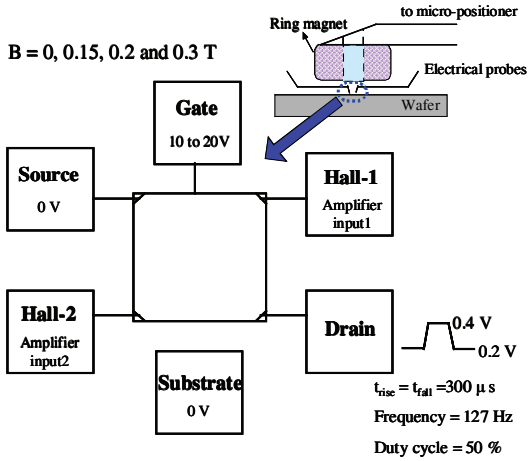

Fig. 1 Wafer-level Hall measurement set-up for the inversion sheet charge density (n_s). 4H-SiC gated Van der Pauw structure is used, which has an active gate area of 150 μm × 150 μm.

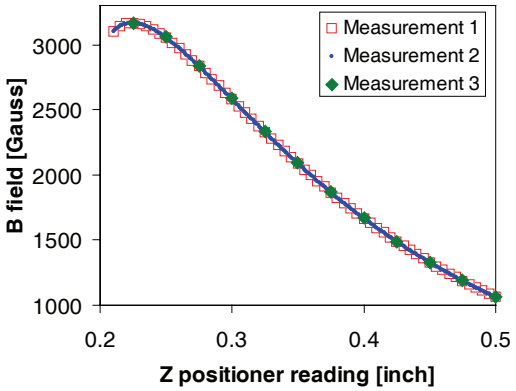

Fig. 2 Magnetic field calibration as a function of z positioner readings. Three measurements performed on different days and different time of the day agree very well. The variation is well within 10 Gauss.

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3200 Gauss is achievable. The relationship between the magnetic field and the vertical separation distance is calibrated by a small (0.016 mm^2 active area) Hall Sensor. As shown in Fig. 2, three calibrations are performed on different days and different time of the day. The variation between them is well within 10 Gauss (as shown in Fig. 3), which is comparable to commercial Hall measurement system. This variation takes into account the control error of the micro-positioner and the effect of temperature change in the lab. The magnetic field controlled by the micro-positioner is very repeatable.

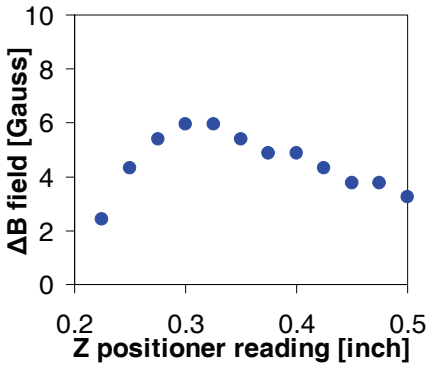

Fig. 3 B field variation within three measurements performed on different days and at different time of the day.

In this work, we utilize this Hall set-up to examine 4H-SiC n-channel MOS-gated Van der Pauw structures with 150 µm × 150 µm gated area.

In order to get μ_{Hall}, inversion sheet charge density (n_s) and sheet resistance (R_s) are measured separately. In the n_s measurement, the gate is kept at a certain potential, the source and substrate are grounded and the drain voltage is modulated from 0.2 V to 0.4 V by a 127 Hz square wave with t_{rise} = t_{fall} = 300 µs. The differential voltage between the two Hall terminals is measured using a differential amplifier (10 MΩ input impedance) and monitored with an oscilloscope along with the source current. The set-up is shown in Fig. 1. The use of drain voltage modulation allows the signal-to-noise ratio to be improved significantly by averaging. The short measurement time prevents complications due to device drift during the measurements. This is especially important when measuring SiC MOSFETs, which are known to have significant as-processed charge trapping and de-trapping [3].

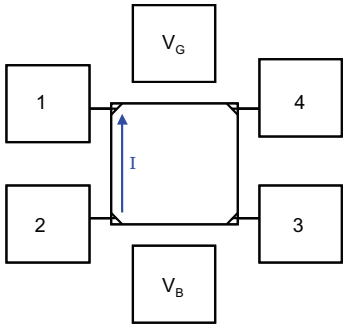

Fig. 4 Van der Pauw procedure for measurement of sheet resistance (R_s)

The sheet resistance (R_s) is measured with standard Van der Pauw procedures [4]. As illustrated in Fig. 4, under a certain gate bias, a constant current is forced from terminal 2 to terminal 1 (I_{21}) and the voltage difference between terminal 3 and 4 (V_{34}) is measured. $R_{21,34} = V_{34} / I_{21}$ is calculated. Repeat this measurement on different edges of the device and with different directions. R_s can be determined by the following equations.

$$R_A = (R_{21,34} + R_{12,43} + R_{43,12} + R_{34,21})/4$$
$$R_B = (R_{32,41} + R_{23,14} + R_{14,23} + R_{41,32})/4$$
$$\exp(-\pi R_A/R_s) + \exp(-\pi R_B/R_s) = 1$$

With n_s and R_s, Hall mobility can be easily calculated using $\mu_{Hall} = 1 / (n_s \times R_s)$.

RESULTS AND DISCUSSIONS

Fig. 5 shows the measured waveforms from the Hall terminals corresponding to the drain voltage modulation at four different magnetic fields. The source current is also plotted on the secondary axis, measured by a current amplifier. The peaks at each transition are due to displacement current arising from the asymmetry in the device geometry. The asymmetry also produces an offset voltage in the measured differential voltage, as expressed in equation (1) where V_{diff} is the voltage difference between the Hall terminals, V_o is the offset voltage, B is the magnetic field, I is the drain or source current and q is the electron charge. While the voltage difference between the two flat regions (dV_{diff}) is the sum of the actual Hall voltage change and the offset voltage change, only Hall voltage gets larger as the magnetic field increases. Measuring the voltage difference at a few magnetic fields can separate the two contributions. Fig. 6 plots dV_{diff}/dI as a function of B field. According to equation (2) the inversion sheet charge density n_s can be directly extracted from the slope in Fig. 6.

$$V_{diff} = V_o + \frac{BI}{qn_s} \quad (1)$$

$$\frac{dV_{diff}}{dI} = \frac{dV_o}{dI} + \frac{B}{qn_s} \quad (2)$$

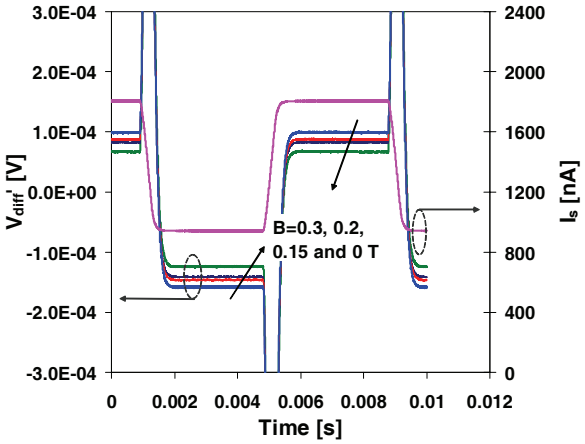

Fig. 5 Differential voltage waveforms between the Hall terminals corresponding to the drain voltage modulation at four magnetic fields. Source current is measured with a current amplifier and plotted on the secondary y-axis.

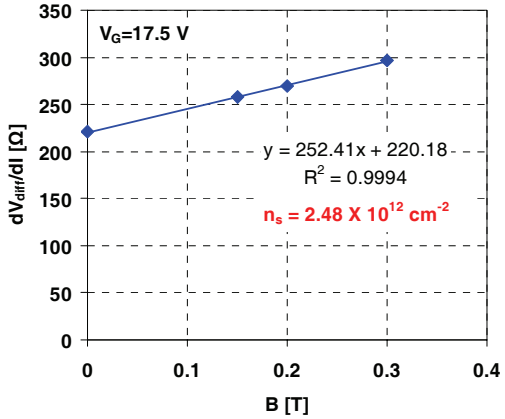

Fig. 6 n_s extraction from the differential voltage waveforms measured at four magnetic fields. dV_{diff}/dI is plotted as a function of B field. n_s is extracted from the slope. This measurement is done with V_G = 17.5 V.

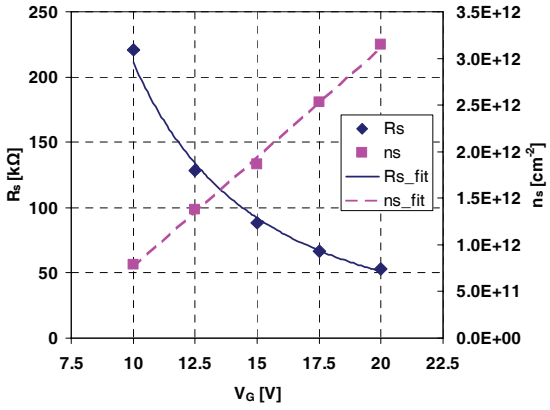

Fig. 7 Sheet resistance and inversion sheet charge density measured at different gate voltages.

Same measurements and extractions are done with five gate voltages (from 10 to 20 V). Sheet charge density is plotted as a function of gate voltage in Fig. 7. R_s is also plotted in the same figure, measured by the standard Van der Pauw procedures. The Hall

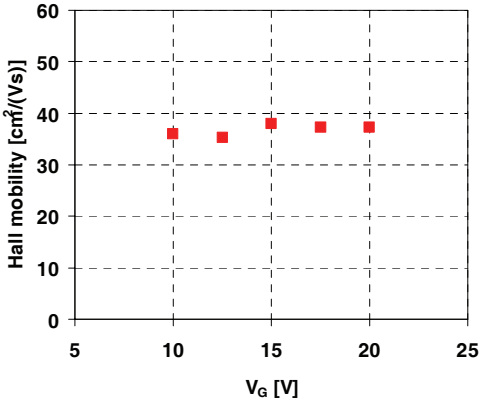

Fig. 8 Hall mobility calculated from R_s and n_s as a function of gate voltage.

mobilities are calculated from $\mu_{Hall}=1/(qn_sR_s)$. Fig. 8 shows the Hall mobility as a function of gate bias. It has very weak dependence on the gate voltages investigated. This is not what one would expect for a high-quality Si-based MOSFET. However, for novel devices based on SiC, it is common. Similar dependency has been reported on SiC devices measured by regular Hall measurement systems [5,6]. The measured mobility is very small compared to the bulk value. This is also well known for SiC MOSFETs.

SUMMARY

We have demonstrated a fast wafer-level Hall-mobility measurement method that does not require any wafer dicing, wire bonding, packaging nor the bulky, expensive regular Hall measurement system. This method is very simple and cost-effective that it can be employed by university labs. Device characterization and development are much more convenient by using this technique. With this method, further explorations of interactions between interface traps and channel carriers as well as device degradation mechanisms become possible.

ACKNOWLEDGEMENT

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Questions and Answers

Q1: Did you use an alternative purely electrical IBM Research and Development method to extract the mobility?

A1: The purpose of Hall mobility measurement is determining the mobility contributed truly by the mobile electrons. The mobility extraction based on purely electrical measurement is affected by the charge trapping in the oxide. This influence is even more severe in novel devices with alternative channel / dielectric materials such as SiC, InGaAs and high-k dielectrics etc, which are known to be full of traps.

Q2: Did you look into charge trapping hysteresis?

A2: No, we have not characterized the hysteresis due to charge trapping yet.

Q3: Did you find that hall mobility and effective mobility were different or the same?

A3: The effective mobility is much smaller than the Hall mobility. The effective mobility extracted was ~25% of the Hall mobility.

Q4: Do you think the voltage drift is too big? Isn't voltage drift going to be a small effect and something you don't have to worry about?

A4: The bigger-than-expected voltage drift could be caused by a combination of device drift and differential amplifier drift. For the measurement of small Hall voltages, a differential amplifier with high input impedance is required. On the other hand, high input impedance means longer time constant and thus more time to stabilize. However, for the purpose of sheet charge density extraction, the DC voltage drift is not something we are concerned about, because the voltage difference in response to the AC drain voltage modulation is what we are after, and it does not drift.

Q5: Why do people use Van der Pauw over a simpler geometry?
A5: In a very simple rectangular-shaped Hall plate, in order to achieve a geometrical correction factor close to 1, the sense contacts must be made very small. While in Van der Pauw structure, a geometrical correction factor very close to 1 can easily be achieved.

Q6: What is the distance between magnet and sample and how much did you have to change the probe tips to get it to fit?
A6**:** The probe tips are bended so that the magnet can be placed about 1.5 mm above the sample without touching the probe tips in between.

Q7: Have you done this on a plain material and not a MOSFET?
A7: No, we have not done it on a plain material.

Q8: What is the temperature effect on the magnetic field?
A8: Temperature has very small effect on the magnetic field. We measured the magnetic field on different days and different times of the day. This takes into account the magnetic field variation due to temperature change in the lab. The variation is well within 10 Gauss, which is less than 1% of the field we applied.

Q9: What is the lowest inversion charge density you can measure?
A9: We are still optimizing our measurement system. At this moment, we are not sure what is the lowest inversion charge density we can measure.

Q10: How do you measure (calibrate) the height of the magnet above the sample?
A10: The absolute distance between the magnet and the sample is not necessary for the measurement. In the B field calibration, the magnetic field is measured as a function of the micropositioner reading. With this relationship and the chip thickness offset, the magnetic field is readily controllable. The actual distance is the micropositioner reading offset by the distance between the sample and the reference point of the micropositioner.