Effect of surface roughness and metal/substrate interfaces on loss in superconducting resonant circuits

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Abstract

Loss in superconducting resonant cavities can be significantly increased as microscopic two level systems become unsaturated at low power and low temperature. In this work we studied coplanar waveguide structures to find the correlation between this loss and sample processing. We find that the loss is dependent on both the substrate-superconductor interface and the methods used to process the devices. In particular, a more carefully prepared interface reduced the loss due to two-level systems significantly. On the other hand, processing methods that left the gap between the central waveguide and the ground plane relatively rough did not cause more two-level system loss, but the overall loss was significantly increased for the roughest surfaces.

Superconducting circuits are poised to make a significant contribution to the development of quantum computing [1]. However, the main hindrance to realizing a functional quantum bit from these materials is the loss at the low powers and low temperatures that are required to conduct operations and inhibit thermally induced transitions in the devices. There are a number of potential contributors to the total loss, including intrinsic loss due to the superconductor loss tangent, surface loss, radiation, and other effects [2]. These losses can originate from many sources in the circuit. For example, a significant loss mechanism in the low power, low temperature regime is due to unsaturated two levels systems (TLSs) in the dielectrics, interfaces, and surface oxides [3]. In general, at low powers the total loss decreases with temperature down to about 2 K, then loss starts to increase as the temperature continues to go down. This has been attributed to polar molecules such as OH^- or other impurities, with electric dipole moments that act as TLSs in the presence of an RF electric field [4].

Recently, Gao, *et al.* [5] studied the loss in superconducting coplanar waveguide (CPW) structures. Remarkably, they found that the TLS loss was not in the bulk of the substrate. Rather, the TLS's are located at the surfaces, either on the metal (i.e. the top, oxidized region or the interface between the metal and the substrate) or on the exposed substrate surface in the gap. Prosllier, *et. al,* showed data supporting the interpretation of the metallic surface being the source of TLSs [6]. They coated the surface of bulk Nb resonators with ALD-Al_2O_3, and after annealing the electronic states of Nb_xO_y became less pronounced, while the metallic Nb states where sharpened, similar to pristine Nb not exposed to atmosphere. Improving the surface in this manner greatly reduced the total loss in their superconducting radio frequency resonators. However, the question as to whether the TLSs reside primarily on the metal surfaces, the dielectric in the gap, or on both, has not yet been answered.

In this paper we show that both the roughness of the dielectric in the CPW gap and the interface between the superconducting metal and the substrate can have a large effect on the total loss of microwave resonators. However, the TLS part of the loss is not affected by the gap roughness, while it is significantly reduced if we carefully prepare the interface between the Nb and the Si substrate. We take this as evidence that TLSs reside primarily at the metal/substrate interface.

The CPW resonators were constructed made out of Nb on Si. We used ¼-wave geometry, capacitively coupled to a continuous stripline launch. Similar CPW structures are ubiquitous in superconducting circuits, acting as memory, buses, and a wide range of other applications [7]. These structures are well understood and are commonly used to study the loss in materials in this application [8]. Gao et. al [5] showed that as the surface area increases of the center line of the CPW increases (with a proportional increase of the gap to keep the impedance constant at 50 ohms) the TLS loss decreases. This is because as the gap increases, the filling factor, i.e. the concentration of electric field in the gap, decreases significantly [9]. Therefore, for the CPW geometry, we chose a relatively narrow center line, with width of 3 μm and a gap of 2 μm, as shown in

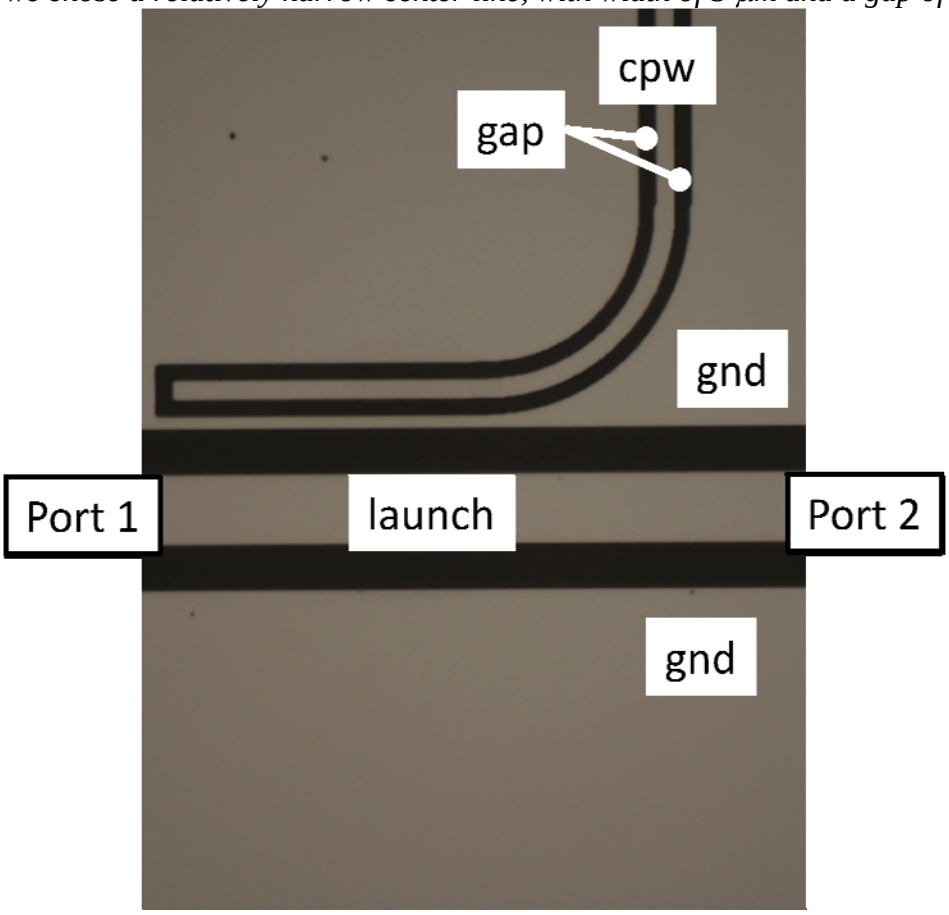

Figure *1*. This increases the effects of the CPW surfaces and also reduces the tendency to trap magnetic flux on the line [10].

The first test we conducted was to investigate the effect of processing induced roughness of the CPW gap on the RF properties. We accomplished this by using different etch recipes to define the CPWs. Three different dry etch recipes of the Nb where used: (1) SF6 at high RF power; (2) SF6 at low RF power, and (3) CF4 +O_2 at medium power. The substrates were high quality intrinsic Si(001) wafers, resistivity of ~17 kΩ cm. For these first three samples, the silicon substrates were use as they came from the box, with a light ion mill to prepare the surface before depositing 200 nm of Nb. The results of AFM imaging of the gap between the CPW centerline and the ground are shown in the third column of Table *1*. We find that the high power SF6 etch resulted in the roughest gap, while the low power SF6 gave a factor 4 lower RMS roughness. However, this did not translate into a lower loss, as discussed below.

The second test we conducted was to take the process that gave the lowest loss (SF6 low power) and improve the Si/Nb interface using a H-terminated Si surface with no ion mill before the Nb depostion. The recipe for the HF dip consisted of 20 mL HF and 200 mL H_2O for three minutes and rinsing in dionized for three minutes. The sample was placed in the vacuum within 5 minutes of removing from the HF water mixture to minimize oxidation of the surface.

An adiabatic dilution refrigerator (ADR) was used to conduct the low temperature measurements. The base temperature of the ADR was less than 50 mK, as measured using a RuOx sensor attached to the sample holder. During experiments, the temperature of the sample was typically held at 100 mK. The RF measurements consisted of measuring the transmitted power, S_{21}, through the launch line, which was capacitively coupled to the CPWs. Measurements where done using a 1 – 20 GHz vector network analyzer (VNA). The microwave feedline was

fitted with 70 dB of attenuation, and the transmitted signal went to the 4K stage into a directional isolator, a grounded bias tee in the opposite direction to cool the center line, and then to a HEMT, which gave about 40 dB amplification. Another 30 dB amplification was achieved with an external, room temperature amplifier.

Measurement where performed at temperatures 65 mK to 1 K in an adiabatic dilution refrigerator (ADR) using a vector network to measure the real and imaginary parts of the S_{21} parameter. Because the ¼ wave CPW resonator is coupled to a continuous stripline, we measure a dip in the transmitted power at the resonance frequency. The power and temperature dependence of the resonance frequency and quality factor were then measured.

The measured loss of a resonator, δ_m, can be separated into

$$\delta_m = \delta_i + \delta_C, \qquad Eq.\ 1$$

the sum of the internal loss and the coupling, i.e. leakage between the resonator and the launch. The internal loss, δ_i includes the material dependent loss. This is the relevant quantity that we are interested in measuring. Note, however, that it the measured value for the material is convoluted with the field distribution around the CPW, resulting in an effective filling factor, F, that represents the percentage of the cavity that is filled with the material of interest. Because we do not want to make any assumptions in this work about the location of the TLSs, in this work we measure the normalized loss, $F\delta_i$, for various processing and surface preparation techniques.

To accomplish this, we start with the definition

$$\delta \equiv 1/Q. \qquad Eq.2$$

Using this, the measured loss can be found from Q_m, where

$$Q_m = \frac{f_r}{\Delta f}. \qquad \textit{Eq. 3}$$

Here, f_r is the resonance frequency of the cavity, and Δf is the frequency width at -3 dBm below the background. Using Eq. 1 and Eq. 2, we write

$$\frac{1}{Q_m} = \frac{1}{Q_c} + \frac{1}{Q_i}. \qquad \text{Eq. 4}$$

To deconvolve Q_i from Q_C and Q_m we use the relation

$$S_{21} = ae^{-2\pi i f \tau}\left[1 - \frac{Q_m/Q_C e^{i\varphi}}{1+2iQm\left(\frac{f-f_r}{f_r}\right)}\right], \qquad \text{Eq. 5}$$

the fitting procedure given in Ref. [11], and Eq. 4 to find $\delta_i = 1/Q_i$.

This procedure was followed on the four samples as described above for a range of high to low powers of microwave injection and at temperatures less than 100 mK. The results are presented in Figure 2, where it can be seen that the sample with the roughest gap has the highest total loss. However, as mentioned before, the gap roughness is not the determining factor, as evidenced by the fact that the SF6 low power etch, with 11 nm gap roughness, gave a lower loss than the CF4, with only 0.8. This indicates that the total loss has other contributions, for example the edge roughness. The final sample, (HF-dipped substrate, SF6 low power etch with no RF clean before Nb deposition), showed the lowest total loss of the set, indicating that the interface between the Si and Nb is an important contributor to loss. This also gives a clue as to the location of lossy TLSs in the structures.

The behavior of δ_i for each resonator shown in Figure 2 as the power decreases varies as expected by the TLS model, showing an increased loss as the power is decreased due to the TLSs become unsaturated [12]. Qualitatively, for each sample the contribution of the TLSs to the loss can be estimated by comparing the increase of the loss from high to low power. While these loss vs. power curves can be fit to back out the TLS density, it is necessary to make assumptions in

those fits. For example, a power independent background loss must be assumed, which is not well justified for samples such as these, where the background loss is on the order of the TLS loss, δ_{TLS}.

Therefore, in this work we utilize the temperature dependence of the resonant frequency, f_r, to determine the contribution of TLSs in these samples. We follow the method used by Gao, et. al [5], where the normalized TLS loss at zero temperature, $F\delta_{TLS}^{0}$, can be found by measuring f_r (T) at high power and fitting to the equation:

$$\frac{f_r(T)-f_0(0)}{f_r} = F\delta_{TLS}^{0}\left[Re\Psi\left(\frac{1}{2}-\frac{\hbar\omega}{k_BT}\right)-log\left(\frac{\hbar\omega}{k_BT}\right)\right] \quad \text{Eq. 6}$$

where Ψ is the digamma function. The data from the four samples and corresponding fits are shown in Figure 3. The resulting values of $F\delta_{TLS}^{0}$ are given in Table 1, showing a surprising result. We find that the TLS losses in the first three samples very close, despite the fact that they have significantly different total losses. This indicates that the surface in the gap and the edges of the CPW are not the most important factors for TLS of loss. This could be explained in various ways, e.g. possibly the Si surface has been passivated by the F-based etch. We find that the SF6 etch processes is slightly better than the CF4 etch from the TLS perspective, with the low power process being optimal.

In addition to the trend that more gentle processing with the SF6 leads to lower total loss as well as a lower TLS loss, we also find that the sample with the HF dip had a significantly lower TLS loss contribution. This shows that the TLSs live primarily at the substrate-metal interface.

In conclusion, we have shown that the interface between the dielectric substrate and the metal plays an important role in the RF loss of superconducting CPW structures. More careful processing is important, but the roughness of the gap is shown to be a necessary but not exclusive condition to obtain high Q devices. By treating the surface of intrinsic Si(100) wafers

with HF and using the SF6 low power etch we minimized both the total and the TLS loss in these devices.

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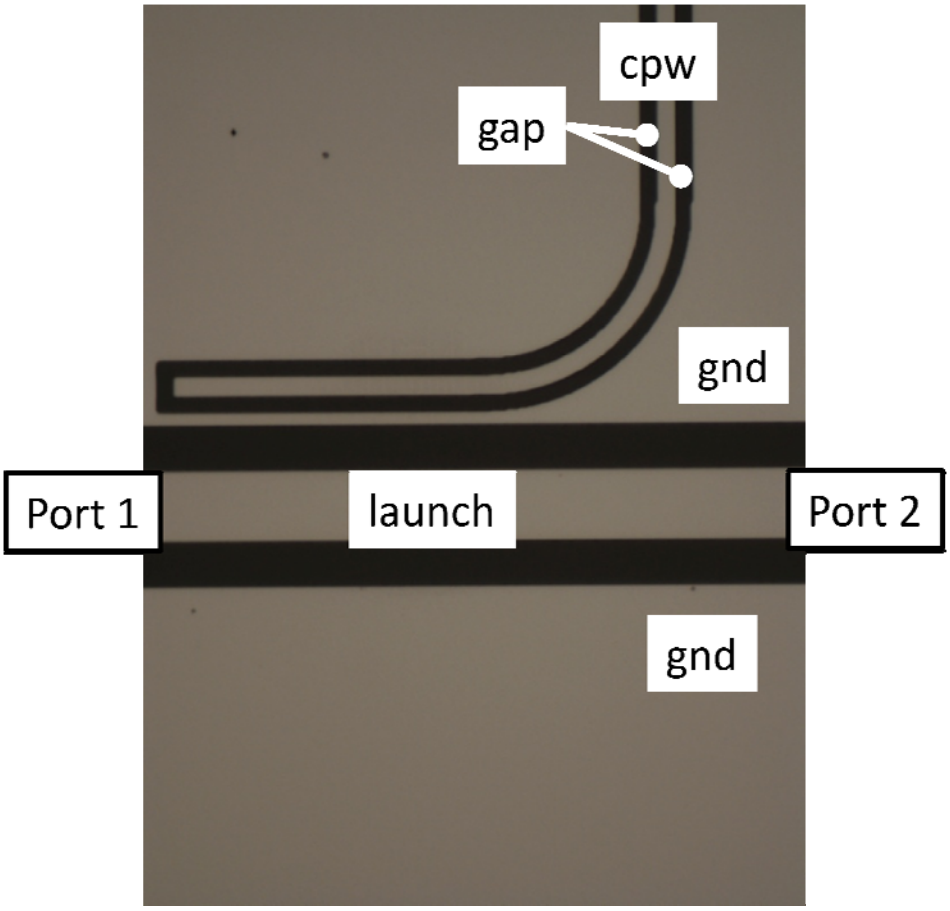

Figure 1. Area of niobium coplanar waveguide next to the RF launch. The launch line is 10 μm wide with a gap of 6 μm to the ground plane. The center line of the CPW is 3 μm wide with a gap of 2 μm. The CPWs are fabricated from 200 nm Nb on c-sapphire chips. The chips are mounted in a small box, and wirebonded to the RF connectors. The RF is injected on one side (port 1) and transmitted power measured on the other (port 2), yielding the S21 parameter. The CPW is capacitively coupled to the stripline, with the strength of the coupling determined by the geometry of the stripline next to the launch (length, separation, widths, etc.).

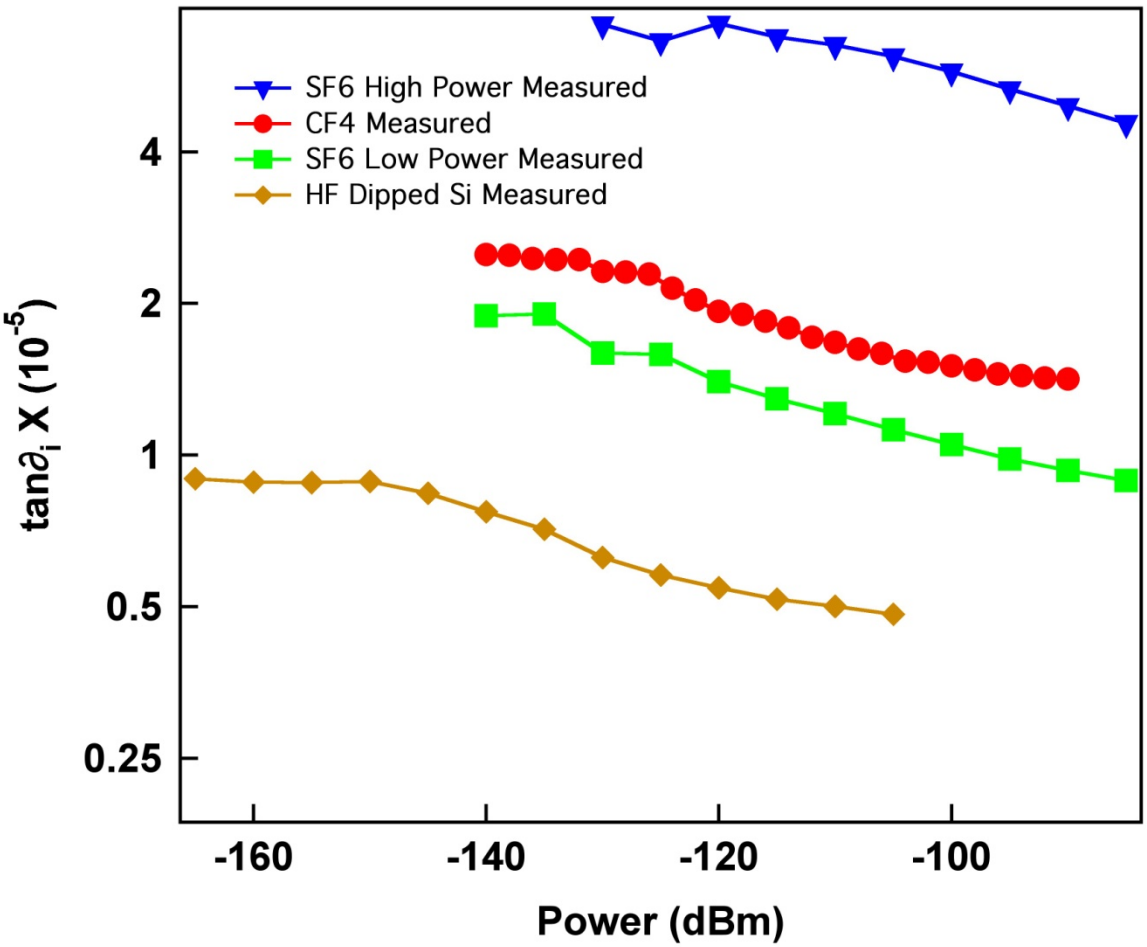

Figure 2. Loss tangent as a function of microwave power for 200 nm Nb CPWs grown on Si(100) with different types of processing. Top curve (blue traingles) is the loss tangent for a CPW processed with SF6 at high power, top middle (red circles) processed with CF4, bottom middle (green squares) processed with low power SF6, and the bottom (orange hourglasses) is for a CPW grown on intrinsic Si(100) dipped in HF and processed using low power SF6.

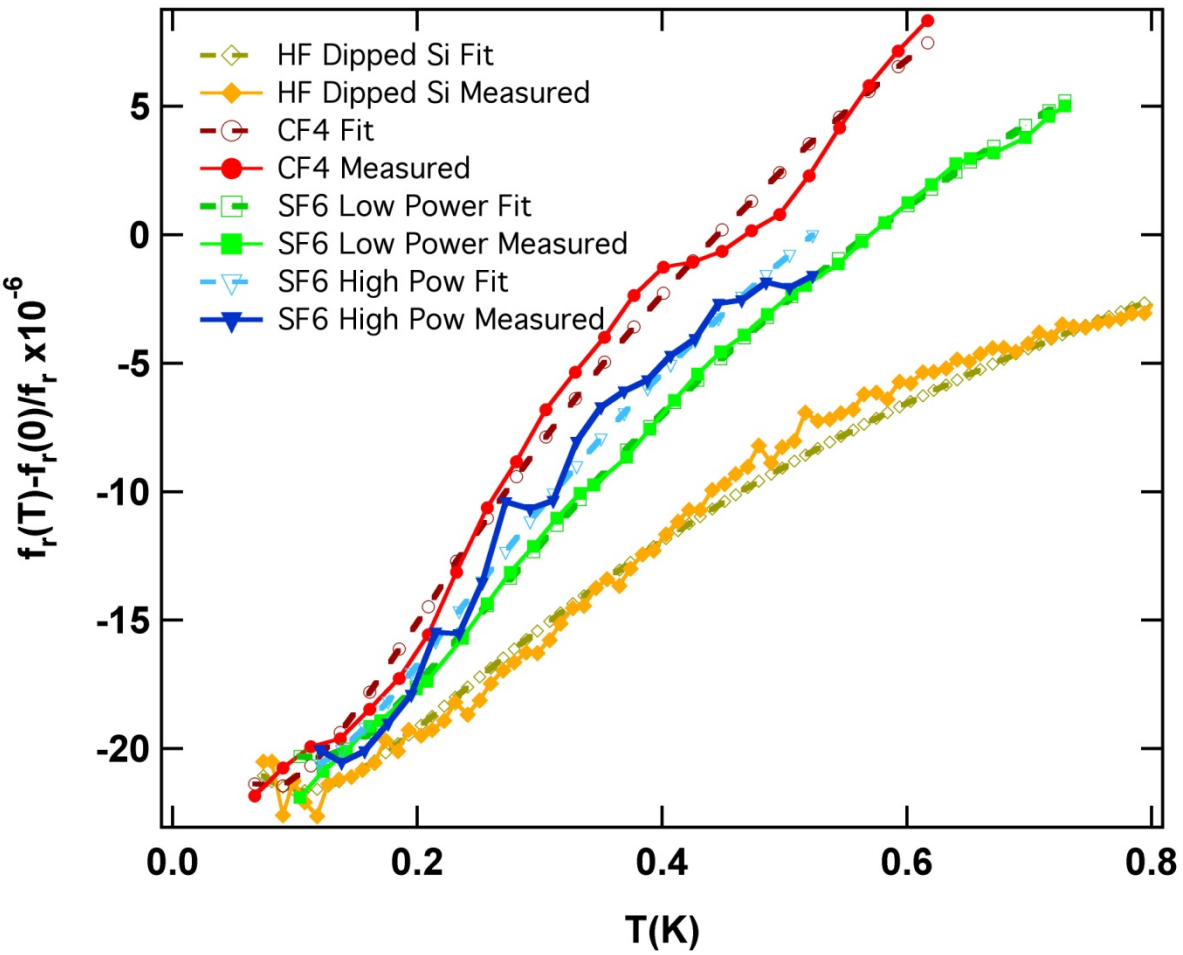

Figure 3. Resonance frequency versus temperature for niobium (Nb) coplanar waveguides (CPW) with different substrate processing and different etches. Experimental and fit data using equation (1) for Nb etched with CF4 are (●) and (○) respectively, for Nb processed at high power with SF6 are (▼) and (▽) respectively, for Nb etched at low power are (■) and (□) respectively, and for the Si(100) substrate dipped in HF and processed with SF6 at low power are (●) and (●) respectively.

Nb/Si Processing	Substrate processing	RMS Roughness in gap (nm)	Total loss $F\delta_i^0$ ($x10^{-5}$)	TLS loss $F\delta_{TLS}^0$ ($x10^{-5}$)
CF4	Ion mill	0.8	3.0	1.7
SF6 high power	Ion mill	45	9	1.6
SF6 low power	Ion mill	11	2	1.3
SF6 low power	HF dip	11	0.9	0.9

Table 1. Results for different Nb on intrinsic Si(100) CPW. The type of processing is listed under Nb/Si Processing for each sample measured. The root means square roughness is given for each process in nanometers. Fit $F\delta_{TLS}$ is the intrinsic loss due purely to TLSs times the filling factor.

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