MICROWAVE OPTIMIZATION OF 10 V PJVS CIRCUITS

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Abstract

Proper operation of programmable Josephson voltage standard arrays depends on the uniform distribution of microwaves to a large number of Josephson junctions. Too much or too little microwave power will change the current range of a junction's constant voltage step so that an entire array of junctions will have a smaller total current margin. In this paper we discuss the important aspects of microwave power distribution including splitting the microwaves to different arrays, keeping the microwave bias uniform within an array, and minimizing the total input power to the circuit.

Introduction

In a canonical programmable Josephson Voltage Standard (PJVS), the power from a microwave source is split to drive multiple arrays of Josephson junctions (JJs) in parallel. The arrays are capacitively coupled to the microwave source. In order to add the dc voltages produced by each array, the neighboring arrays are connected in series through low-pass filters. There is a limit to the maximum number of JJs in an array based on the attenuation and/or distortion of the incoming microwaves; this limit is typically a few thousand JJs and depends on transmission line impedance [1]. There is also a limit to the maximum number of microwave splits that is based on the chip area needed for the splits and the total input power needed.

There are presently three different designs of 10 V PJVS systems: a PTB design with 69,632 junctions based on 70 GHz microwaves [2], an AIST system with 327,680 junctions biased at 16 GHz [3], and a NIST system using 268,800 junctions that operates at 18 GHz [4]. All of these systems balance various design considerations to maximize the dc current range over which the array maintains a constant voltage, i.e., "flat step". An array should have the largest possible number of junctions in order to maximize the total voltage produced by the array. Unfortunately, too many junctions undesirably attenuate the microwave power within the array, which reduces the current range of the flat step.

The number of arrays and splitters used to divide the microwave power depends on the available power, the power required to achieve the largest current range, and the junction attenuation. The total number of JJs required to produce 10 V is inversely proportional to the chosen bias frequency. The number of JJs per array can be reduced to increase the current range, but this requires more splitters and simultaneously increases the total power required.

The main advantage of the PTB design is that the higher microwave frequency allows the use of fewer Josephson junctions (JJs), which makes both fabrication easier and yield higher, with the disadvantage of the use of narrow-band microwave designs and costly components. The AIST design uses a 64-way microwave split to drive 64 arrays of 8,192 NbN/TiN_x/NbN JJs operating at a higher temperature of 10 K. Because the AIST design uses quarter-wave splitters, a significant amount of the chip area is used for microwave distribution. Two advantages of operating at 10 K with a cryocooled package are that the microwave path can be shorter, which minimizes cable losses, and more total bias power can be dissipated during chip operation.

NIST has designed two 10 V PJVS circuits that use either 16-way or 32-way division of the microwaves. They were chosen to experimentally determine the design that would produce the system with the best performance. The 16-way design uses four stages of two-way Wilkinson dividers [5] to drive coplanar waveguide (CPW) transmission lines, each having an impedance that is tapered from 85 Ω to 19 Ω and contain an array of 15,600 JJs. Tapering the impedance partially compensates for attenuation and allows more junctions per array than possible with an untapered line. The 32-way design contains an additional divider stage to drive 8,400 JJ arrays embedded in a line that is tapered from 50 Ω to 8 Ω.

Because a JJ is a current-driven device, it is important to keep the microwave current, but not necessarily the power, constant for each JJ in the array. The maximum 85 Ω impedance is limited by the largest practical impedance for a CPW on a Si substrate. Since the 32-way design required fewer JJs per array, the tapering was reduced. By starting the 32-way design at 50 Ω, the applied microwave current at the start of the array is roughly the same as the input current on the 16-way design.

We have also reduced the critical current of the JJs compared with lower-voltage NIST PJVS designs in an attempt to reduce the required microwave power while still maintaining an operating current range greater than 1 mA. Larger critical currents lead to a larger current range on the constant-voltage step. However, the applied microwave

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power also scales as the square of the critical current. For these circuits, the critical current was kept below 10 mA.

At some point, the applied power is too much for the circuit to operate at the 4 K bath temperature. For our circuits, this power is ~ 500 mW, and includes both DC and microwave power dissipated on chip. At applied powers greater than this, the chip warms above the bath temperature, and the current range of the voltage step decreases. To reduce the circuit temperature, we have maximized the thermal transfer from the circuit to the chip by fabricating the junctions directly on the Si by use of trenches in the wafer native oxide [6].

Power Dividers

The use of lumped-element Wilkinson dividers provides two major advantages [5]: (1) they are a factor of 10 smaller than quarter-wave dividers for the same frequency band, and (2) a Wilkinson divider has isolation between its output ports. The latter feature is important because the divider dissipates any power reflected from any impedance discontinuities in an array transmission line and prevents it from disrupting neighboring arrays. To improve input-power matching, there is a 90° phase shifter on one of the otherwise symmetric binary-division arms to destructively interfere any systematic reflections in the design through poor parameter targeting.

A drawback of the lumped element design is that it is more sensitive to fabrication process tolerances as compared to designs with distributed microwave components. For instance, the deposited capacitor oxide thickness needs to be within a few percent of the design thickness in order to achieve the designed divider performance.

Tapering

One of the goals in the NIST 10V PJVS designs was to efficiently use the microwave power. Because we realized that reducing the total required microwave power would be a challenge, the design needed to make the most of every milliwatt. The large number of junctions demands power, and, in general, PJVS systems are limited by the total power that can be applied. In the 70 GHz version, most of the power is dissipated in long lossy distributed transmission lines, whereas in the AIST design, most of the power is dissipated in the termination resistors.

By tapering the CPW impedance within the array, the NIST design can yield more JJs per array, and also reduce the number of divider stages. The lower termination impedance that results from the tapered design also reduces the total power dissipated in the terminations. The tapered designs, therefore, optimize the power that is used in the arrays.

Conclusion

Design of microwave circuits is an important part of optimizing the performance of 10 V PJVS systems. By minimizing reflections from and/or dissipation in all of the microwave elements, we have optimized the microwave power that reaches the arrays. A number of different microwave techniques and design considerations, including splitters, tapers and lower critical currents, were necessary to achieve optimization.

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