An improved fast I_d-V_g measurement technology with expanded application range

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ABSTRACT

Fast I_d-V_g measurements on very high performance devices (very low channel ON-resistance) and larger area devices (therefore large gate capacitance) are subject to serious distortions. Methods to minimize these distortions are introduced in this paper; thus expanding the applicable range of this important measurement technique.

I. INTRODUCTION

For advanced device research and development, charge trapping in the gate dielectric and its interface are common when the technology is less than mature. To investigate the transient charge trapping problem, the fast I_d-V_g method has become very popular and therefore very important [1-6]. Although many works using the fast I_d-V_g method were published, the method's shortcomings have not been discussed, especially when it is applied to very high performance devices as well as large devices. Direct application of the fast I_d-V_g measurement to these situations can lead to serious errors.

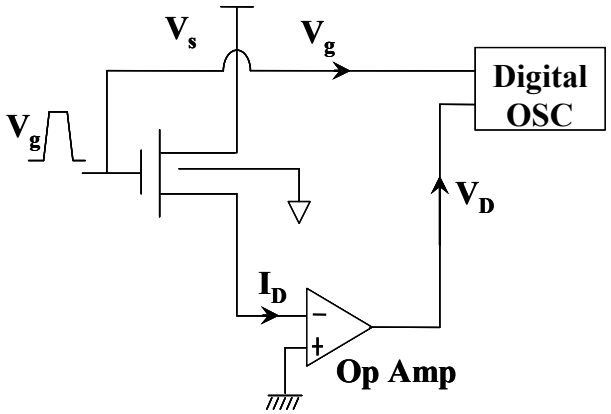

Fig 1: Schematic of experimental setup. V_g and V_D signal paths are illustrated with arrows. Delay time between them is measured exactly during our experiment. A common ground is built in our circuit. Digital oscilloscope with 1 GHz bandwidth and 4 GS/s sampling rate is used to capture the fast slope signals.

Figure 1 shows the experimental setup of the fast I_d-V_g method. A voltage pulse is applied to the gate with controlled rise and fall time, as well as duration. A constant bias is applied to the source. The corresponding drain current is amplified with an operational amplifier, which maintains the drain contact at ground potential.

II. EXPERIMENTAL METHODS

In this common setup, the measured drain current includes the displacement current due to the fast changing gate voltage and the gate-to-channel capacitance. When the displacement current represents a non-negligible fraction of the total current, the result is a distorted I-V curve. The displacement current derived from gate-channel capacitance and fast V_g change is illustrated in figure 2. This current is superimposed on the drain current. The common solution is usually ignored because of small-area devices or just slowing down measurement.

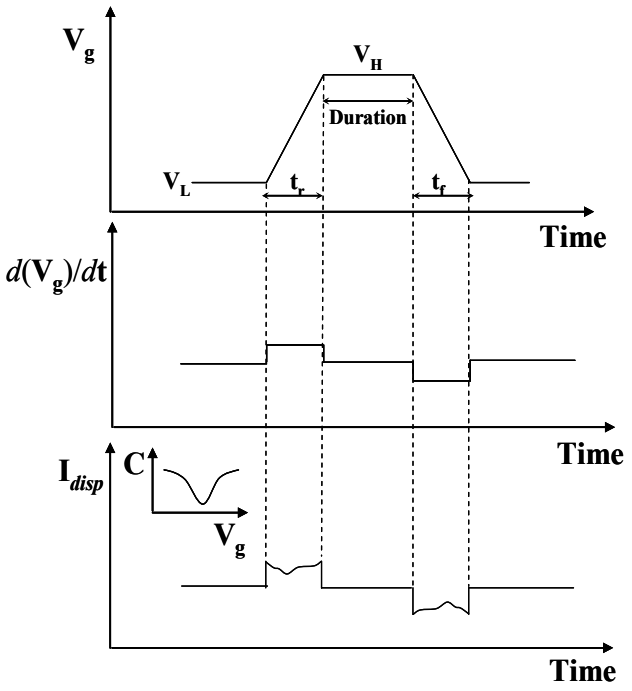

Fig 2: Illustration of displacement current, which is derived from fast V_g change (dV_g/dt) and gate-channel capacitance(C-(V_g)).

Another source of drain current waveform distortion comes from the power droop effect in a high-speed circuit [7]. When the transistor turns on, it draws current at a very high speed. If the bias voltage is supplied by a remote power source through a cable and a wafer probe, there is an inevitable amount of reactive impedance. When this reactive impedance is comparable to or larger than the channel resistance, significant reduction of the effective bias voltage occurs. This transient lowering of source or drain bias directly distorts the I_d-V_g curve. Take an extreme example: if the drain current is 10 mA and the transistor is turned on with a rise time of 1

ns, the rate of current change is 10^7 A/s. The finite inductance in the cable and probe can drop the bias all the way to zero, even if some bias gets through, it will rise at a much slower pace, leading to significant distortion in the drain current waveform. However, the solution is never mentioned before in fast I_d-V_g works. It is possibly because of high-speed devices seldom being studied by fast I_d-V_g measurement.

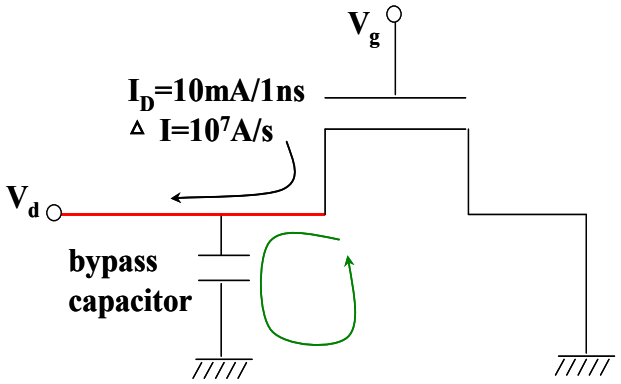

Fig 3: Illustration of bypass capacitor. Red line, which stands for cable and wafer probe, has inevitable reactive impedance and causes reduction of the bias voltage on our device; green line is a lower impedance path supplied by bypass capacitor for high frequency transient current to flow.

To correct for the power droop, the standard method is to insert a bypass capacitor as close as possible to the device as shown in figure 3. The bypass capacitor is used to provide a low impedance path through which the high frequency transient current to flow. Based on some analysis, which is explained in detail in the next section, a 10 μF bypass capacitor is chosen.

III. RESULTS & DISCUSSION

Displacement current To demonstrate the effect of displacement current, submicron inversion-mode $Al_2O_3/In_xGa_{1-x}As$ MOSFETs (8 nm oxide, 75 um^2 transistor size) were used in fast I_d-V_g experiment [8]. In addition to a 10 μF bypass capacitor at the probe providing the source bias, a 50 Ω termination is placed as near as possible at the gate probe to ensure an undistorted gate waveform.

Figure 4 shows the gate pulse waveform (100 ns rise/fall time), the as measured drain current waveform (Vs= -5 mV), the measured displacement current waveform and the drain current waveform after correction for displacement current (right vertical axis). It should be noted that all the current waveforms are shown in voltage because they have been converted by a current amplifier. The similarly corrected drain current waveform for the Vs= -50 mV is also shown (right vertical axis), and it overlaps completely with the Vs= -5 mV waveform. The displacement current waveform was measured with Vs= 0 V. In this case, the displacement current is as big as the drain current. Without the correction, the distortion is extreme as can be seen.

Since the displacement current is measured with the identical setup and gate waveform, it is a simple, convenient, very good correction. It is not completely accurate because the drain bias is not the same. This small error tends to overcorrect the displacement current. Careful inspection will reveal a small dip of the drain current before leveling off. This dip is the result of the over correction.

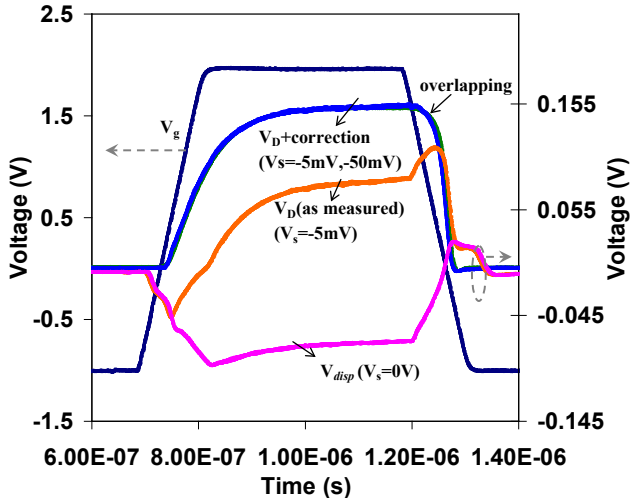

Fig 4: Measured V_g, V_{disp}, V_D, V_D+correction under -50 mV source bias and V_D+correction under -5 mV source bias as a function of time using a trapezoidal wave applied to the gate with 100 ns rise/fall time under less than 400 ns duration time.

The perfectly overlapping corrected drain current waveform for the two drain biases provide verification that, at least for the 100 ns rise/fall time case, the power droop is completely eliminated.

Power-droop Choosing a bypass capacitor is not simple. The bypass capacitor must be chosen carefully to ensure that low impedance current is supported at all frequencies. This is important because, in the fast I_d-V_g measurement, both fast edge as well as long pulse are used, covering a wide frequency range. On the other side, capacitance impedance must also be accounted for cable impedance as well. The characteristic inductance of a coaxial cable connecting the power source and the device can be in the range of 200 nH/m to 300 nH/m. Thus, the inductance impedance rises rapidly with frequency. Figure 5 shows the impedance of the inductance and the bypass capacitance.

Clearly, a larger capacitor is more capable of providing low impedance for a wider range of frequency. How low is low enough? It depends on how low the channel impedance is. If the channel impedance is 30 Ω (as the case of the device uses in this study), then we need the power source impedance to be less than 0.3 Ω to ensure less than 1 % distortion. From figure 5, it is clear that none of the cases with capacitance lower than 1 μF can do the job. A larger capacitance is needed, like 10 μF. As can be seen in figure 5, for a cable inductance of 300 nH, the overall impedance is below 0.2 Ω.

In our experiment, a homemade termination, with a 10 μF chip capacitor being placed as close to the probe tip as possible, is used as the power source tip.

However, the larger doesn't mean the better. Much larger capacitor with cable inductance creates worse ringing problems in the circuit. Even with the 10 μF bypass capacitor, a small ringing is found in the output signal of long period in the circuit. Some special circuit has to be applied to suppress this problem.

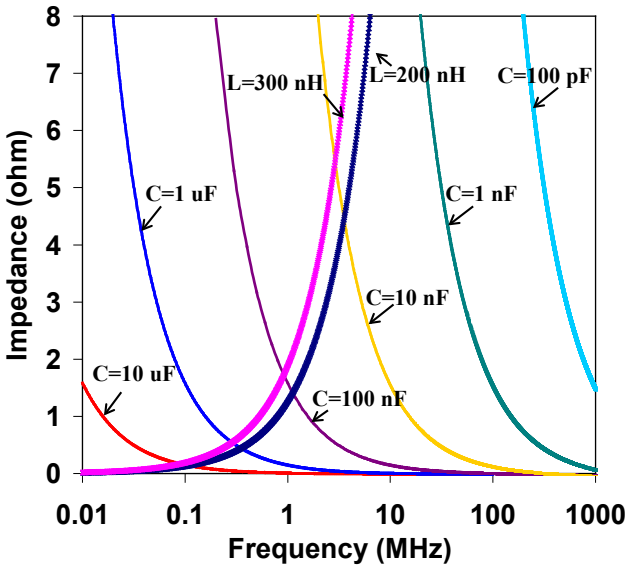

Fig 5: Calculated impedance for inductances of 200 nH, 300 nH and capacitances of 100 pF, 1 nF, 10 nF, 100 nF, 1 μF, 10 μF. For 10 μF, at frequencies less than 0.1 MHz, current goes through the cable as if has less than 0.2 Ω impedance; at higher frequencies, current is drawn by bypass capacitor due to less than 0.2 Ω capacitance impedance.

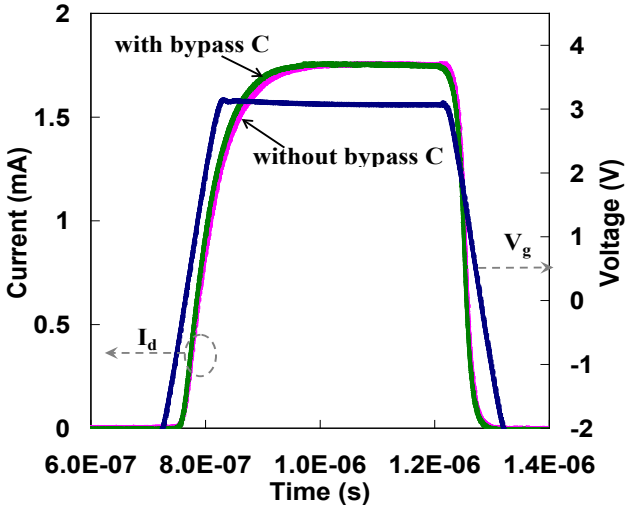

Fig 6: Measured V_g and I_d with and without a bypass capacitor under -50 mV source bias as a function of time using a trapezoidal wave applied to the gate with 100 ns rise/fall time and 500 ns duration time.

Figure 6 shows two cases: with and without a bypass capacitor. The gate pulse rise time is 100 ns. The procedure for displacement current correction is the same. Notice the clear slowing down of the corrected drain current waveform rising edge without the bypass capacitor. The power droop sets in at about halfway through the gate pulse. The departure from a smooth rising edge is due to a temporary drop in the bias voltage. On the falling edge, a small slower decreasing is shown in the drain current curve without bypass capacitor. That is because the on-level current was blocked to discharge by huge inductance impedance of the cable.

As can be seen in figures 5 and 6, the corrected drain current rising edge is not ideal after displacement and power droop correction. That comes from some parasitic capacitor, especially the comparatively large drain pad capacitor in this device. A feedback capacitor is usually used to suppress some small input capacitor's effect on the amplifier. However, for a 130 pF drain pad capacitor, it seems there is no way to suppress it through only some compensation in the circuit. The field oxide is really indispensable to ensure the parasitics are not beyond the reliable range.

CONCLUSION

We identified potential sources of error in the fast I_d-V_g measurement technique and introduced methods to correct for them. These corrections are particularly important for measuring devices that are either large or have high ON-current or both. With the correction technique, the applicable range of the fast I_d-V_g measurement technique is extended.

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