NISTIR 7648

Representation of a Thermal Resistor Network Model of a Packaged Component in STEP AP210 Edition 2

Jamie Stori
SFM Technology, Inc.
Urbana, Illinois

Kevin Brady
National Institute of Standards and Technology
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Rockwell Collins,
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Gary Locke, Secretary

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Patrick D. Gallagher, Director

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INTRODUCTION

STEP AP210 (ISO-10303:210) is the first international standard capable of representing both ECAD and MCAD data of packaged components within a unified model. In order to promote AP210 as a standards-based mechanism for the representation of component data, it is desired to demonstrate the ability of AP210 to support a variety of domain-specific data requirements in the design and product-realization process for electronic assemblies and products.

Prior work and existing implementations have validated the ability of AP210 to serve as a neutral format for the representation of conventional ECAD data for individual components as well as bare boards (PCB / PWB) and assemblies (PCA / PWA). To date, AP210 has not been validated as a representation mechanism for communicating the analytical models and/or data necessary to support mechanical analysis (i.e. thermal and vibration) of electronic assemblies.

Being able to predict the package and die temperatures of components to a reasonable degree of accuracy in an assembly under expected operating conditions is critical to the effective design of modern electronic products. In order to support the thermal analysis requirements of designers, while balancing the concerns of component suppliers to protect proprietary details of their products, there has been an increasing emphasis on the role of compact thermal models of components.

The JEDEC JC-15.1 Committee on Thermal Characterization Techniques for Electronic Packages and Interconnects has been actively involved in the specification of methods to determine and report the thermal performance of integrated circuit packages (JESD51 series of specifications). Most recently, the JC-15.1 committee has focused efforts on the development of standards for thermal modeling, with an emphasis on compact thermal models through the JESD15 specifications:

JESD15, *Thermal Modeling Overview*
JESD15-1, *Compact Thermal Modeling Overview*
JESD15-2, *Terms and Definitions for Modeling Standards*
JESD15-3 *Two-resistor compact thermal model guideline*
JESD15-4, *DELPHI Compact Thermal Model Guideline*

The first of the thermal modeling standards, JESD15-3 was recently (July 2008) published. At the time of this writing (October 2008), the remaining standards in the JESD15 family have not yet been published.

The focus of the JESD15 standards is the use of thermal resistor networks as compact thermal models for packaged components (JESD15-3 and 15-4). Notably, the JEDEC standards do not provide nor prescribe a machine-interpretable representation for the thermal networks.

The purpose of this document is to provide a recommended practice for the representation of thermal resistor networks of packaged components in STEP AP210.

COMPACT THERMAL MODELS

A compact thermal model (CTM) is a behavioral model that attempts to predict temperature at a number of discrete points on the package. A CTM is not based on the geometry or material

properties of the component, but is rather an abstract response to various boundary conditions.[1] The objective is to develop a CTM capable of generating reasonably accurate temperature predictions over a suitable range of operating conditions. JESD 15-2 and 15-3 describe two approaches based on using networks of thermal resistors at CTM descriptions of packaged components. In a thermal resistor network, power is analogous to current, temperature is analogous to voltage, and a thermal resistance has units of temperature / power. Ambient conditions are assumed to be isothermal at steady state, and power is applied to a junction node representing power dissipation at the die.

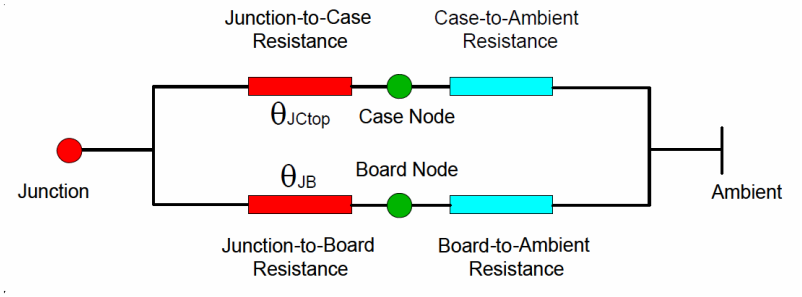

Figure 1. Equivalent thermal resistance diagram of the two-resistor model on a PCB [from JESD 51-12].[2]

The two-resistor model (see JESD 15-3) is generally accepted as the least complicated (and most intuitive) model that captures a reasonable description of thermal performance[3]. A two-resistor model has three network nodes (junction, board, and case) and two thermal resistances (junction-to-board and junction-to-case). In a two-resistor model, the die is assumed to be at a single temperature. Figure 1 (reproduced from JESD51-12) diagrams the structure of the two-resistor model.

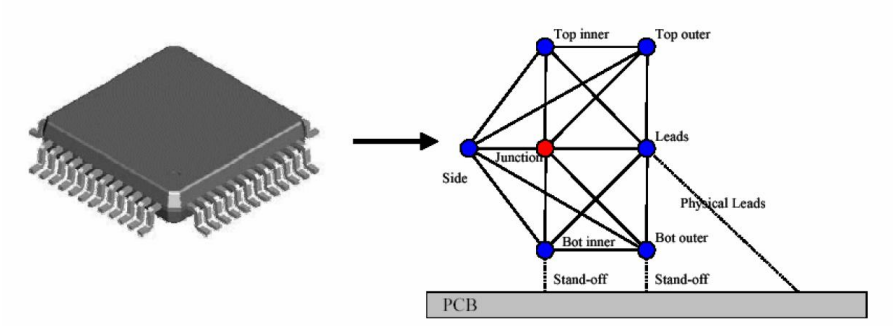

Figure 2. Possible DELPHI node topology for a PQFP package [from JESD 51-12]. [4]

In those cases where higher predictive capabilities than provided by the two-resistor model are desired, more detailed resistor network models may be employed. The JC-15.1 committee is also nearing publication of JESD15-4 which describes the DELPHI approach to development and application of CTMs. In a DELPHI model, in addition to thermal resistors between die and surface nodes, thermal links are also permitted between surface nodes (shunt resistors)[1]. Figure 2

[1] Shidore, S., and Sahrapour, A., ñDELPHI Compact Models Revolutionize Thermal Design,ò http://www.flomerics.com/files/casestudies/661/t287.pdf

[2] This figure is reproduced from the JEDEC standard JESD 51-12. In JESD 51-12, it appears as Figure 2.

[3] Joiner, B., "Use of Junction-to-Board Thermal Resistance in Predictive Engineering," *Electronics Cooling Magazine*, Vol.5, No. 1, (January, 1999), pp. 14-17.

[4] This figure is reproduced from the JEDEC standard JESD 51-12. In JESD 51-12, it appears as Figure 3.

(also reproduced from JESD 51-12) illustrates a possible thermal network topology for a PQFP package model.

In the following section, the ARM entities suitable for modeling a CTM such as the two-resistor or DELPHI model are described.

ARM MAPPING

The portion of a thermal resistor network representing a CTM of a packaged component is not a complete network. In order to utilize the CTM for predictive purposes, boundary conditions must be applied to the appropriate network notes, and/or the portion of the network representing the CTM must be embedded into an expanded thermal network model representing the larger system.

In terms of ARM representation within the AP210 schema, the portion of the thermal network representing the CTM is to be modeled as a `Functional_product`. The details of the CTM network are contained in the `Thermal_network_definition` of the `Functional_product`.

It is important to note that the representation of the CTM includes a definition of a thermal network, but does not include an instantiation of a thermal network. Generating an instantiation (a Functional_unit) is only appropriate at the time that a complete (solvable) network can be constructed, which requires knowledge of the boundary conditions and ambient environment.

The `Thermal_network_definition` is related to a `Packaged_part` through a `View_definition_relationship` with `.relation_type = 'thermal model assignment.'` By associating the thermal network definition with a packaged part it is implied that the thermal network is valid for alternate packages of the packaged part. These are generally minor package variations that are not expected to have significant impact on the thermal model. If it is necessary to support distinct thermal models for alternate packages, the white box model of the packaged part could be referenced.

The external interface of the `Functional_product` is a `Functional_unit_usage_view`, which provides a definition of only those nodes of the network which are intended to serve as an interface to the external system. To support independent versioning of the usage view and network definition each is related to the same `Functional_product` through a `Functional_version`, which need not be the same.

Each of the externally facing (usage view) nodes are defined by a `Functional_unit_usage_view_terminal_definition`. In the case of a thermal network, each of these terminals would be a `Scalar_terminal_definition`, a subtype of `Functional_unit_usage_view_terminal_definition`. Each of the nodes of the network (both internal and external) is defined by a `Thermal_functional_unit_network_node_definition`, a subtype of `Functional_unit_network_node_definition`. Each terminal in the usage view must be related to a node in the network definition through a `Functional_unit_network_terminal_definition_node_assigment` relationship.

There are several supported mechanisms for relating a node in the thermal network to something physical in the packaged part. In many applications, the location of the network node may be provided only through a textual description as in Figures 1 and 2 above. However, in the event that a more precise and/or formal association with an aspect of the packaged part is desired and/or required, `Thermal_functional_unit_network_node_definition` has two optional attributes: `location` and `used_model`. Since a CTM is used to predict location at specific points in physical space, it is possible to associate the network node definition with a `Cartesian_point` in a geometric model (`Shape_model`). Alternately, it is possible to associate the location of the network node model with either a `Non_feature_shape_element` (such as the seating plane) or a

Component_feature. Each of these associations is supported through the location attribute which references an entity of the select type tnd_location_select.

The functional unit representing the CTM of the packaged component is composed of a series of thermal resistors. Each of these thermal resistors is itself a Functional_unit. The ARM entities, relationships, and attributes discussed above in the definition of the thermal network are described in Figure 3.

The key ARM entities and relationships in the modeling of a thermal resistor are described in Figure 4. A thermal resistor is also modeled as a Functional_product. It is recommended that the Functional_product be assigned to a Class of ñthermal resistor.ò A thermal resistor has two terminals. The definition of a thermal resistor will include a Functional_unit_usage_view with a definition (Scalar_terminal_definition, a subtype of Functional_unit_usage_view_terminal_definition) for each of the two terminals. A particular instance of a thermal resistor is modeled as a Functional_unit. The resistor instance will have two terminals (Functional_unit_terminal) whose definition is the corresponding Scalar_terminal_definition from the usage view.

A thermal resistor network will typically contain multiple thermal resistors. Each of these resistors would be modeled as a discrete Functional_unit of the same Functional_product. In other words, the Functional_product is a generic thermal resistor. There is only one relevant parameter, the thermal resistance value. It is recommended that a default value of thermal resistance be associated with the Functional_product through a Product_specific_parameter_value_assigment. Individual thermal resistor instances can populate their specific thermal resistance value by overriding the original Parameter assignment through a Parameter_assignment_override. These relationships are documented in Figure 4. The Representation of the Parameter_assignment will contain one representation item used to populate the specific parameter value, a complex instance of both Numerical_item_with_unit and Thermal_resistance_data_element.

MIM MAPPING

For implementation purposes, the application reference model (ARM) application objects (AOs) and relationships must be mapped to the module interpreted model (MIM) level. Figures 5 and 6 contain the MIM mapping of the ARM objects and relationships pertaining to the Thermal_network_definition described above and documented in Figure 3. In the figures, and the accompanying description, the convention will be adopted that all ARM AOs begin with a capital letter, and MIM entities are presented in all lower-case notation. For MIM entities that represent a direct mapping of a critical ARM AO, both the ARM and MIM names are presented in the figure, with the ARM AO name in parentheses following the MIM entity name. For example, with reference to Figure 5, functional_unit_terminal_definition is the MIM mapping of the ARM AO Functional_unit_usage_view_terminal_definition. At the time of this writing, the MIM mapping for the location and used_model attributes of the Thermal_functional_unit_network_node_definition were not available, as these were very recent additions to the ARM schema.

Figures 7 and 8 contain the MIM mappings for the ARM AOs and relationships pertaining to the representation of a thermal resistor as a Functional_unit. The MIM representation of the physical quantity of thermal resistance is detailed in Figure 8.

REPRESENTATIVE INSTANTIATION OF THE TWO-RESISTOR NETWORK

In order to illustrate the MIM representation of a two-resistor network, a representative sample physical file (Part 21) is attached as an appendix to this document. Figure 9 illustrates some of the

key entity instance mappings in the physical file example. With reference to Figure 1, the thermal network has three nodes: junction, case, and board. Each of these three nodes is modeled as a `thermal_network_node_definition`. In this particular network, all three nodes must be included in the usage view for the network definition, so there is a corresponding `functional_unit_terminal_definition`. There are two thermal resistors, junction-to-case and junction-to-board. Each of these is a `component_functional_unit` with two terminals (`component_functional_terminal`). As discussed above, multiple instances of a thermal resistor can share a single usage view and represent instances of the same `Functional_product`, as is the case in this particular example. There are a couple of minor differences between the MIM entity mappings in the physical file and the entity mappings described in the figures. This is a result of the fact that certain additions and changes have recently been made to the schema, and are not yet available in implementation libraries. In the event that a discrepancy exists, the figures and textual descriptions are to take precedence over the physical file example.

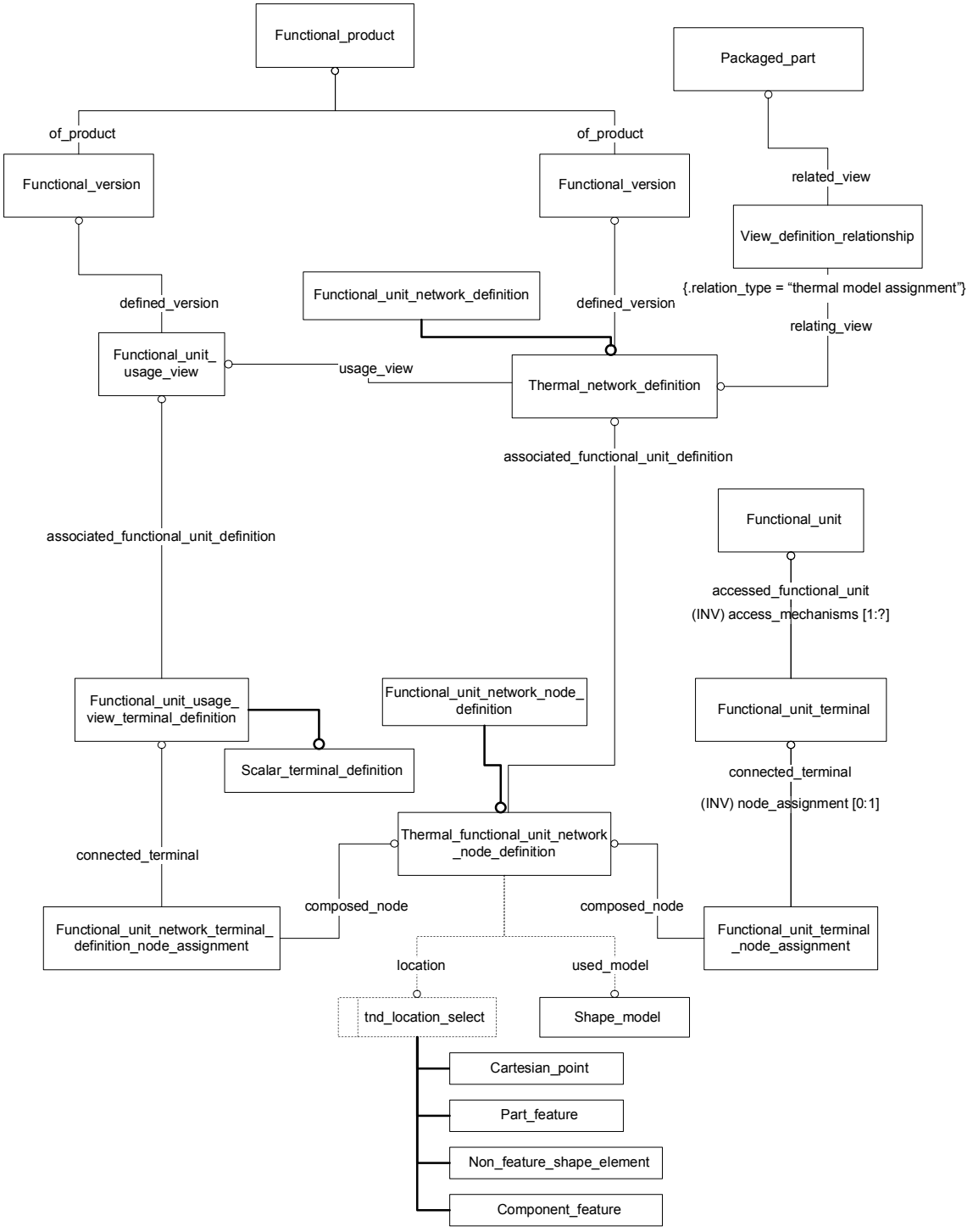

Figure 3. Key ARM entities and relationships in the representation of a Thermal_network_definition.

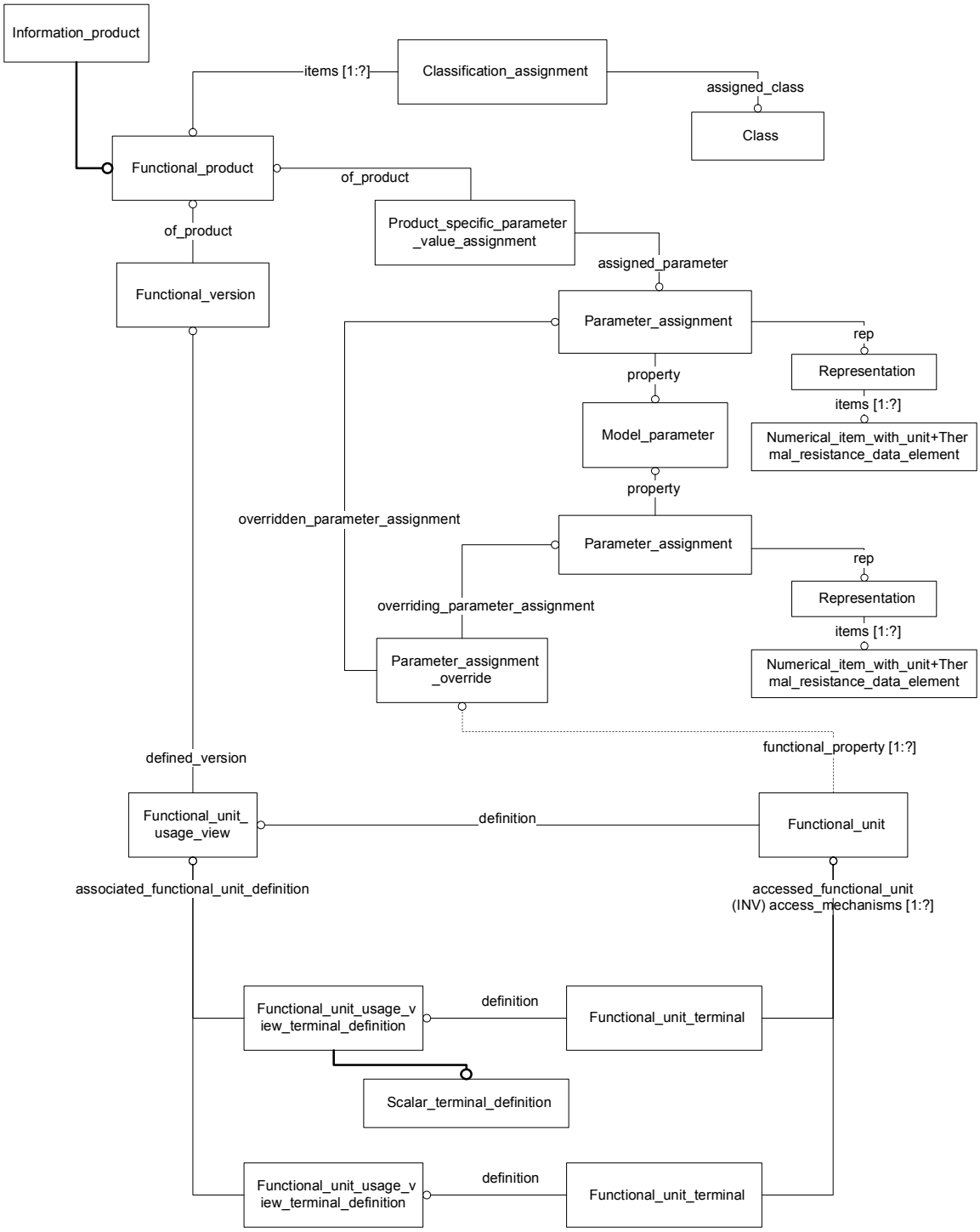

Figure 4. Key ARM entities and relationships in the representation of a thermal resistor.

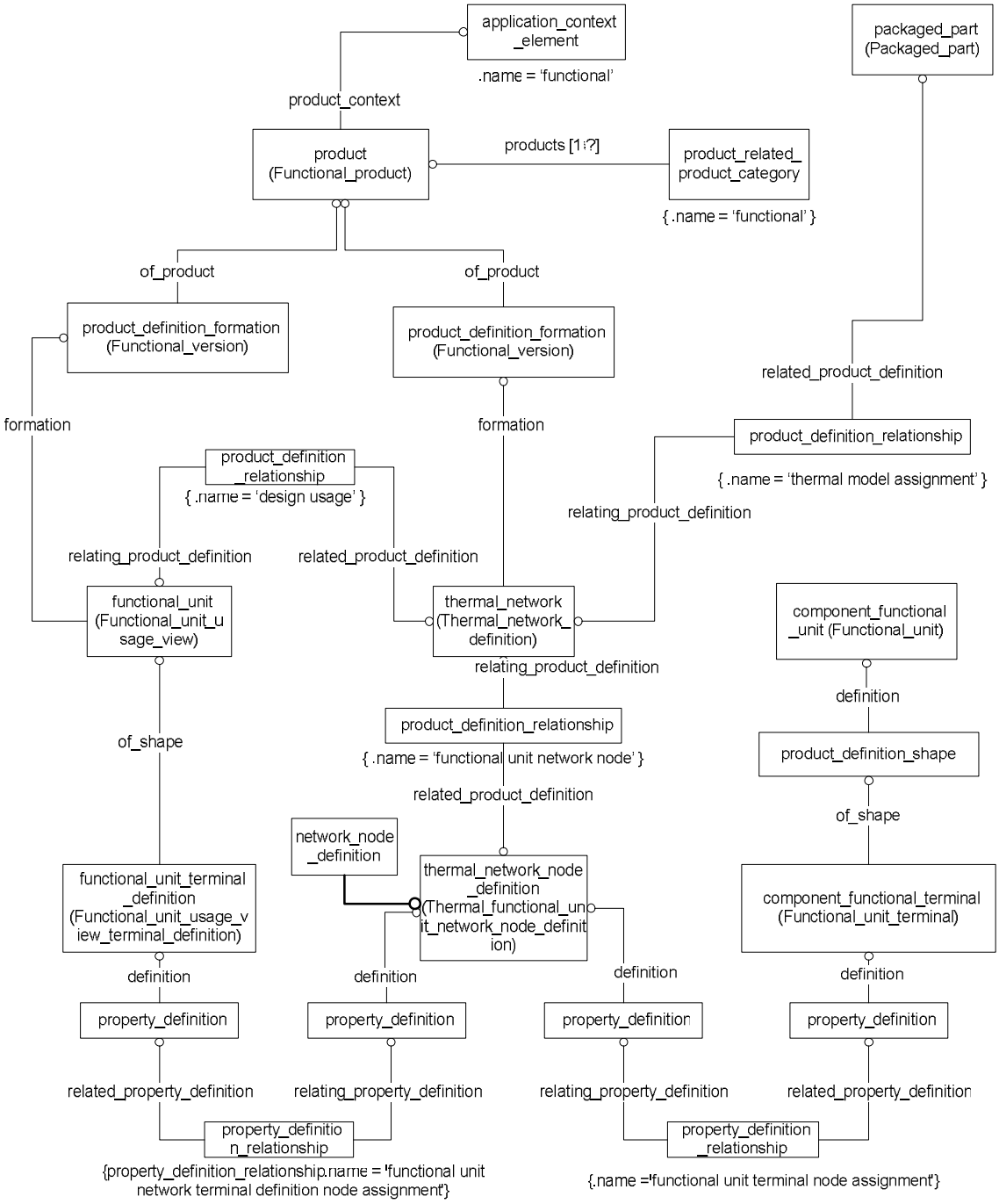

Figure 5. MIM mapping of the entities and relationships in the representation of a Thermal_network_definition

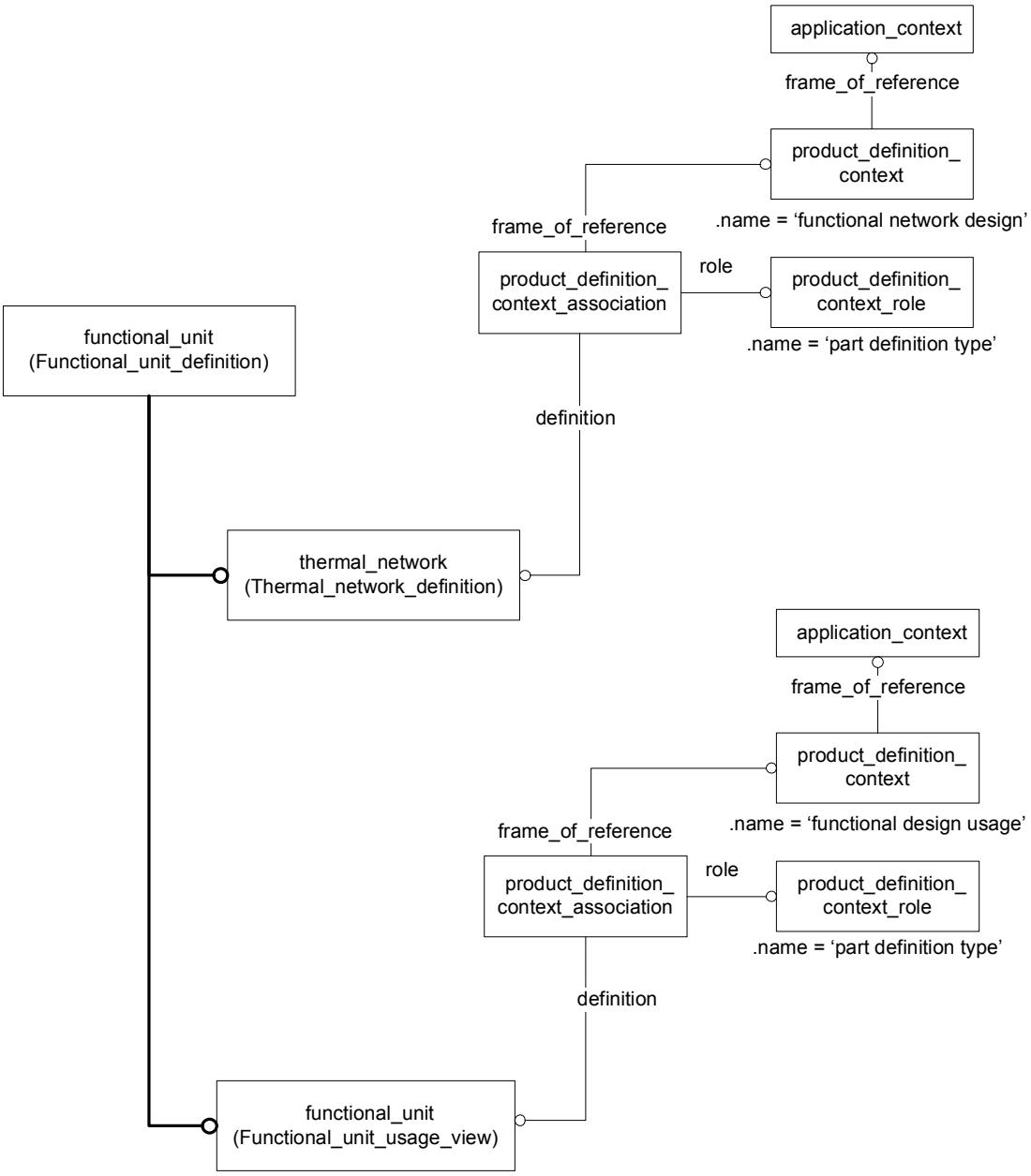

Figure 6. MIM mapping of the Functional_unit_definition entities in the representation of a Thermal_network_definition

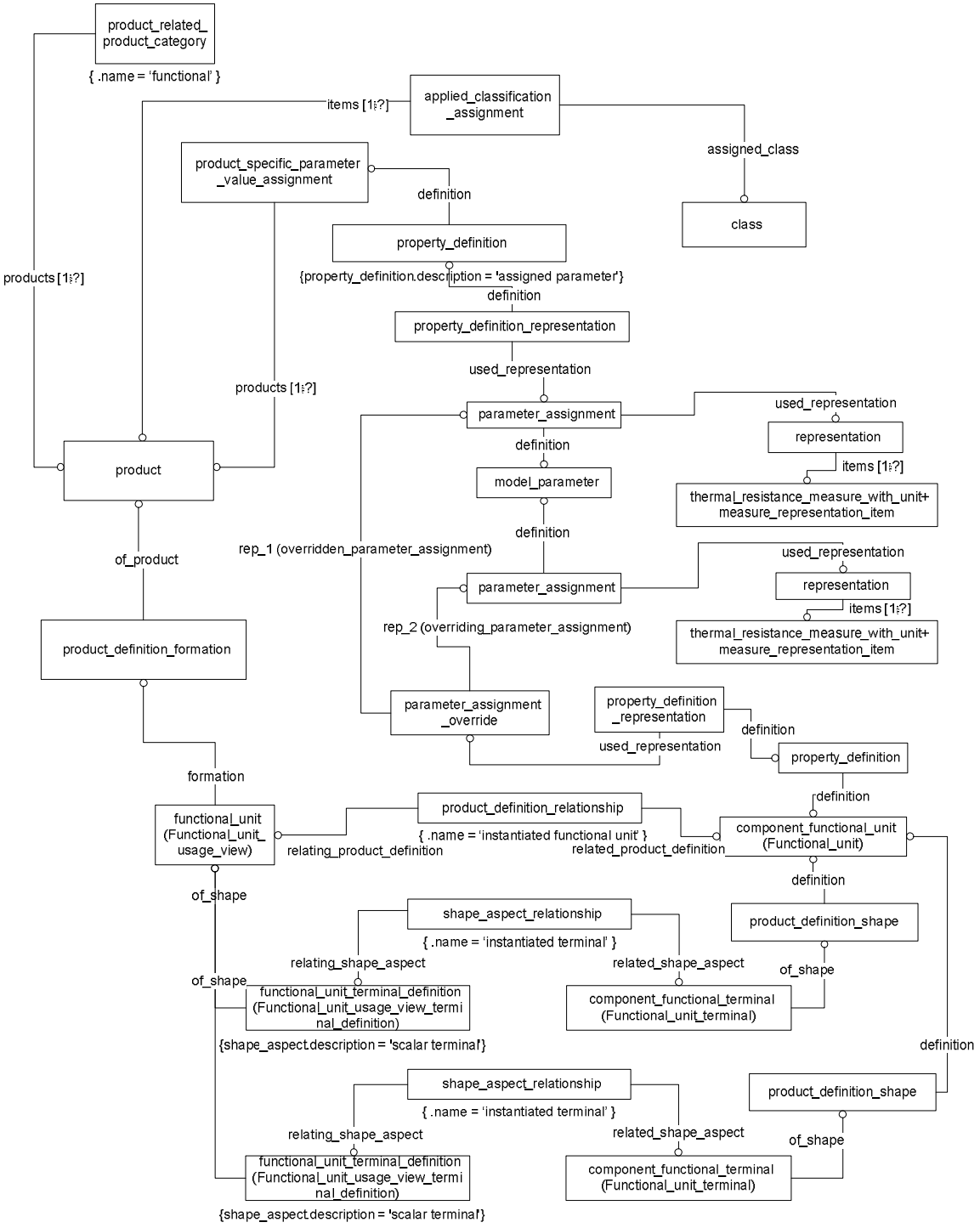

Figure 7. MIM mapping of the key ARM entities and relationships in the representation of a thermal resistor

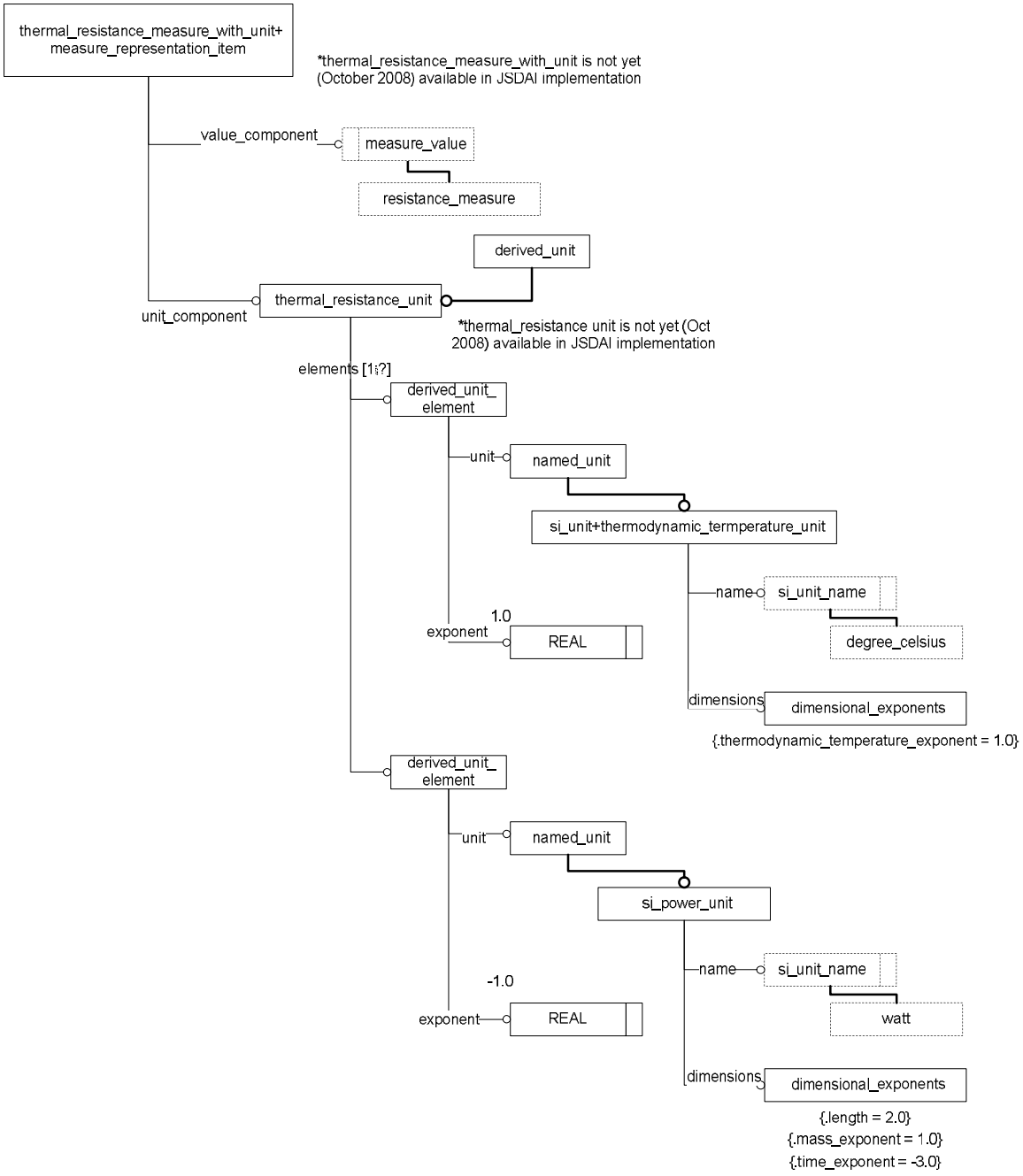

Figure 8. MIM mapping of the entities and relationships used in the representation of a thermal resistance.

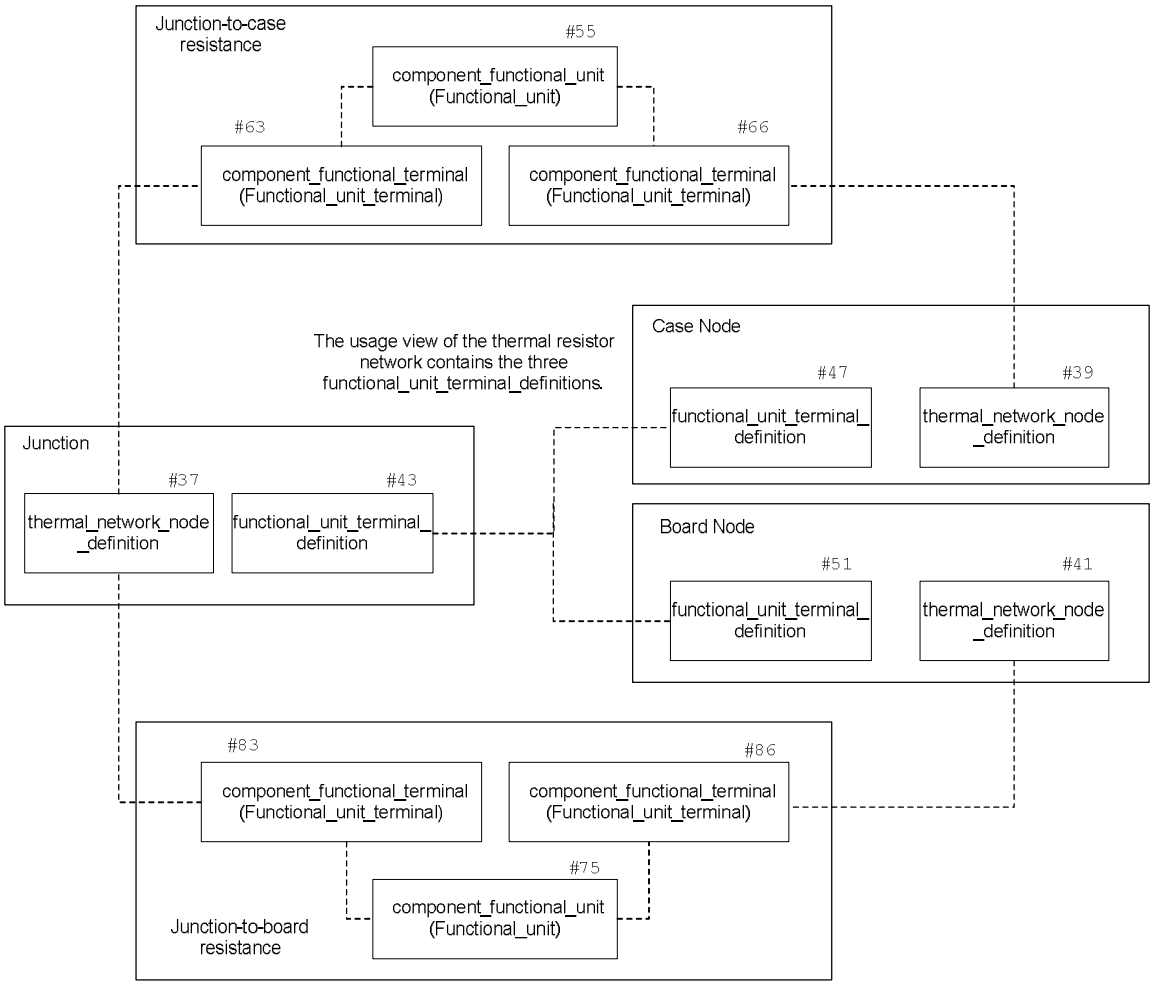

Figure 9. MIM instantiation of the two-resistor network of Figure 1.

APPENDIX. MIM instantiation of entities and relationships in the two-resistor network of Figure 1.

```
ISO-10303-21;
HEADER;
/* Generated by software containing
 * JSDAI (TM) from LKSoft (www.lksoft.com, www.jsdai.net)
 * JSDAI Runtime Version 4.0.0 (Build 270, 2008-08-07T12:17:32)
 * JSDAI XIM Full Library Version 1.126.0 2008-08-07_12-21-15
 */
FILE_DESCRIPTION(
/* description */ ('Sample thermal network definition.'),
/* implementation_level */ '2;1');
FILE_NAME(
/* name */ ' ',
/* time_stamp */ '2008-11-02T17:26:36',
/* author */ ('James Stori'),
/* organization */ ('SFM Technology, Inc.'),
/* preprocessor_version */ ' ',
/* originating_system */ 'JSDAI MULTIPLE Version 4.0.0 (Build 270, 2008-08-
07T12:17:32)',
/* authorization */ 'Lothar Klein');
FILE_SCHEMA(('AP210_ELECTRONIC_ASSEMBLY_INTERCONNECT_AND_PACKAGING_DESIGN_MIM {
1 0 10303 410 1 1 4}'));
ENDSEC;
DATA;
#1=APPLICATION_CONTEXT('CONFIGURATION MANAGEMENT');
#2=APPLICATION_PROTOCOL_DEFINITION('INTERNATIONAL
STANDARD','Ap210_electronic_assembly_interconnect_and_packaging_design_mim',
1994,#1);
#3=APPLICATION_CONTEXT('component thermal model demonstration');
#4=PRODUCT_DEFINITION_CONTEXT('functional network design',#3,$);
#5=PRODUCT_DEFINITION_CONTEXT('functional design usage',#3,$);
#6=PRODUCT_DEFINITION_CONTEXT_ROLE('part definition type',$);
#7=PRODUCT_RELATED_PRODUCT_CATEGORY('functional',$,(#8,#18));
#8=PRODUCT('network','thermal network',$,(#9));
#9=PRODUCT_CONTEXT('functional',$,$);
#10=PRODUCT_DEFINITION_FORMATION('1',$,#8);
#11=FUNCTIONAL_UNIT('network',$,#10,$,$,$,*);
#12=PRODUCT_DEFINITION_CONTEXT_ASSOCIATION(#11,#5,#6);
#13=PRODUCT_DEFINITION_FORMATION('1',$,#8);
#14=THERMAL_NETWORK('network',$,#13,$,$,$,*);
#15=PRODUCT_DEFINITION_CONTEXT_ASSOCIATION(#14,#4,#6);
#16=PRODUCT_DEFINITION_RELATIONSHIP($,'design usage',$,#11,#14);
#17=PRODUCT_DEFINITION_FORMATION('1',$,#18);
#18=PRODUCT('default thermal resistor','thermal resistor',$,(#19));
#19=PRODUCT_CONTEXT('functional',$,$);
#20=CLASS('thermal resistor',$);
#21=APPLIED_CLASSIFICATION_ASSIGNMENT(#20,$,(#18));
#22=PARAMETER_ASSIGNMENT(#23,#24,$,$,$);
#23=MODEL_PARAMETER('theta','thermal resistance',$);
#24=REPRESENTATION($,(#25),$);
#25=(MEASURE_REPRESENTATION_ITEM()MEASURE_WITH_UNIT(RESISTANCE_MEASURE(1.0),#26
)REPRESENTATION_ITEM($)RESISTANCE_MEASURE_WITH_UNIT());
#26=RESISTANCE_UNIT((#28,#30));
#27=SI_UNIT(*,$,.DEGREE_CELSIUS.);
#28=DERIVED_UNIT_ELEMENT(#27,1.0);
#29=SI_POWER_UNIT($,*,$,.WATT.);
#30=DERIVED_UNIT_ELEMENT(#29,-1.0);
#31=PROPERTY_DEFINITION_REPRESENTATION(#33,#22);
#32=PRODUCT_SPECIFIC_PARAMETER_VALUE_ASSIGNMENT($,$,$,$,(#18));
#33=PROPERTY_DEFINITION($,'assigned parameter',#32);
#34=FUNCTIONAL_UNIT('default thermal resistor',$,#17,$,$,$,*);
#35=FUNCTIONAL_UNIT_TERMINAL_DEFINITION('A','scalar terminal',#34,$);
```

```
#36=FUNCTIONAL_UNIT_TERMINAL_DEFINITION('B','scalar terminal',#34,$);
#37=NETWORK_NODE_DEFINITION('junction',$,$,$);
#38=PRODUCT_DEFINITION_RELATIONSHIP('junction','functional unit network
node',$,#14,#37);
#39=NETWORK_NODE_DEFINITION('case',$,$,$);
#40=PRODUCT_DEFINITION_RELATIONSHIP('case','functional unit network
node',$,#14,#39);
#41=NETWORK_NODE_DEFINITION('board',$,$,$);
#42=PRODUCT_DEFINITION_RELATIONSHIP('board','functional unit network
node',$,#14,#41);
#43=FUNCTIONAL_UNIT_TERMINAL_DEFINITION('junction',$,#11,$);
#44=PROPERTY_DEFINITION_RELATIONSHIP('functional unit network terminal
definition node assignment','',#45,#46);
#45=PROPERTY_DEFINITION('junction',$,#37);
#46=PROPERTY_DEFINITION('junction',$,#43);
#47=FUNCTIONAL_UNIT_TERMINAL_DEFINITION('case',$,#11,$);
#48=PROPERTY_DEFINITION_RELATIONSHIP('functional unit network terminal
definition node assignment','',#49,#50);
#49=PROPERTY_DEFINITION('case',$,#39);
#50=PROPERTY_DEFINITION('case',$,#47);
#51=FUNCTIONAL_UNIT_TERMINAL_DEFINITION('board',$,#11,$);
#52=PROPERTY_DEFINITION_RELATIONSHIP('functional unit network terminal
definition node assignment','',#53,#54);
#53=PROPERTY_DEFINITION('junction',$,#37);
#54=PROPERTY_DEFINITION('board',$,#51);
#55=COMPONENT_FUNCTIONAL_UNIT('r_1','junction-to-case',$,$);
#56=PRODUCT_DEFINITION_RELATIONSHIP($,'instantiated functional
unit',$,#34,#55);
#57=PARAMETER_ASSIGNMENT_OVERRIDE($,$,$,$,$,#22,#58);
#58=PARAMETER_ASSIGNMENT(#23,#59,$,$,$);
#59=REPRESENTATION($,(#60),$);
#60=(MEASURE_REPRESENTATION_ITEM()MEASURE_WITH_UNIT(RESISTANCE_MEASURE(0.1),#26
)REPRESENTATION_ITEM($)RESISTANCE_MEASURE_WITH_UNIT());
#61=PROPERTY_DEFINITION_REPRESENTATION(#62,#57);
#62=PROPERTY_DEFINITION($,$,#55);
#63=COMPONENT_FUNCTIONAL_TERMINAL('A',$,#64,$);
#64=PRODUCT_DEFINITION_SHAPE('A of r_1',$,#55);
#65=SHAPE_ASPECT_RELATIONSHIP('instantiated terminal',$,#35,#63);
#66=COMPONENT_FUNCTIONAL_TERMINAL('B',$,#67,$);
#67=PRODUCT_DEFINITION_SHAPE('B of r_1',$,#55);
#68=SHAPE_ASPECT_RELATIONSHIP('instantiated terminal',$,#36,#66);
#69=PROPERTY_DEFINITION_RELATIONSHIP('functional unit terminal node
assignment','',#70,#71);
#70=PROPERTY_DEFINITION('junction',$,#37);
#71=PROPERTY_DEFINITION('A',$,#63);
#72=PROPERTY_DEFINITION_RELATIONSHIP('functional unit terminal node
assignment','',#73,#74);
#73=PROPERTY_DEFINITION('case',$,#39);
#74=PROPERTY_DEFINITION('B',$,#66);
#75=COMPONENT_FUNCTIONAL_UNIT('r_2','junction-to-board',$,$);
#76=PRODUCT_DEFINITION_RELATIONSHIP($,'instantiated functional
unit',$,#34,#75);
#77=PARAMETER_ASSIGNMENT_OVERRIDE($,$,$,$,$,#22,#78);
#78=PARAMETER_ASSIGNMENT(#23,#79,$,$,$);
#79=REPRESENTATION($,(#80),$);
#80=(MEASURE_REPRESENTATION_ITEM()MEASURE_WITH_UNIT(RESISTANCE_MEASURE(0.2),#26
)REPRESENTATION_ITEM($)RESISTANCE_MEASURE_WITH_UNIT());
#81=PROPERTY_DEFINITION_REPRESENTATION(#82,#77);
#82=PROPERTY_DEFINITION($,$,#75);
#83=COMPONENT_FUNCTIONAL_TERMINAL('A',$,#84,$);
#84=PRODUCT_DEFINITION_SHAPE('A of r_2',$,#75);
#85=SHAPE_ASPECT_RELATIONSHIP('instantiated terminal',$,#35,#83);
#86=COMPONENT_FUNCTIONAL_TERMINAL('B',$,#87,$);
```

```
#87=PRODUCT_DEFINITION_SHAPE('B of r_2',$,#75);
#88=SHAPE_ASPECT_RELATIONSHIP('instantiated terminal',$,#36,#86);
#89=PROPERTY_DEFINITION_RELATIONSHIP('functional unit terminal node
assignment','',#90,#91);
#90=PROPERTY_DEFINITION('junction',$,#37);
#91=PROPERTY_DEFINITION('A',$,#83);
#92=PROPERTY_DEFINITION_RELATIONSHIP('functional unit terminal node
assignment','',#93,#94);
#93=PROPERTY_DEFINITION('board',$,#41);
#94=PROPERTY_DEFINITION('B',$,#86);
ENDSEC;
END-ISO-10303-21;
```