Transport Characterization in Nanowires Using an Electrical Nanoprobe

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Abstract

Electrical transport in semiconductor nanowires is commonly measured in a field effect transistor configuration, with lithographically defined source, drain, and in some cases, top gate electrodes. This approach is labor intensive, requires high-end fabrication equipment, exposes the nanowires to extensive processing chemistry, and places practical limitations on minimum nanowire length. Here we describe a simple method for characterizing electrical transport in nanowires directly on the growth substrate, without any need for post growth processing. Our technique is based on contacting nanowires using a nano-manipulator probe retrofitted inside of a scanning electron microscope. Using this approach we characterize electrical transport in GaN nanowires grown by catalyst-free selective epitaxy, as well as InAs and Ge nanowires grown by Au-catalyzed vapor solid liquid technique. We find that in situations where contacts are not limiting carrier injection (GaN and InAs nanowires), electrical transport transitions from Ohmic conduction at low bias, to space-charge limited conduction at higher bias. Using this transition and a theory of space charge limited transport which accounts for the high aspect ratio nanowires, we extract the mobility and the free carrier concentration. For Ge nanowires, we find that the Au catalyst forms a Schottky contact resulting in rectifying current-voltage characteristics, and which are strongly dependent on the nanowire diameter. This dependence arises due to increase in depletion width at decreased nanowire diameter and carrier recombination at the nanowire surface.

1. Introduction

Nanowires continue to fascinate researchers, who are often motivated by the combination of high crystalline quality and nanoscale dimensions not easily accessible by ‘top-down’ lithographic means. Potential applications of nanowires include electronics, photonics, and

sensors [1, 2]. In addition, many nanostructured materials currently investigated for energy storage and conversion applications, such as lithium-ion battery cathodes and anodes [3, 4], and photoelectrochemical water splitting electrodes [5] are films made up of nanowires. Fundamental understanding and control of electrical transport in these nanomaterials is essential for their eventual integration into practical applications. A key challenge that nanowires continue to pose is the lack of simple, reliable techniques to determine the carrier concentration and mobility. The small dimensions of nanowires make bulk techniques such as Hall effect measurement difficult or impossible to implement. Carrier type, concentration and mobility in nanowires are thus frequently determined from the transfer characteristics of a nanowire field-effect transistor (NWFET) device [6]. This approach requires extensive fabrication, exposes the nanowires to various process chemistries, provides channel rather than bulk mobility, and can be strongly affected by surface and interface states [7, 8]. A further drawback is the challenge of making low resistance reproducible Ohmic contacts to nanowires. The common practice of heavily doping the source and drain contacts to achieve low resistance remains difficult to implement in nanowires due to the small dimension.

In this article we review our recent work focused on transport in GaN nanowires grown by selective epitaxy. Using our in-situ nanoprobe technique, in conjunction with 'top-down' lithographic approach, we show how finite dimensions of nanowires, far from the quantum confinement limit, affect bulk mediated transport. Specifically, we show that due to reduced carrier screening, the onset of space charge limited conduction (SCLC) in nanowires occurs at a much lower critical voltage compared to bulk specimens. Using a theory of SCLC specifically developed to handle nanowire geometry we extract carrier concentration and mobility. We also present new result on transport in InAs nanowires, where we compare the carrier concentration

and mobility extracted using the nanoprobe to the values obtained using the NWFET geometry. Finally, we address the situation where charge transport is determined by the metal/semiconductor junction formed between the Au catalyst and the Ge nanowire. The nanoprobe is ideally suited to characterizing such systems, since making Ohmic contacts to the large area substrate is straight forward. Surprisingly, these nanoscale Schottky contacts show increased small bias conductivity with decreasing diameter. Theoretical calculations suggest that this effect arises because electron-hole recombination in the depletion region is the dominant charge transport mechanism, with a diameter dependence of both the depletion width and the electron-hole recombination time.

2. Transport in GaN nanowires grown by selective epitaxy

Group III-N nanowires are attractive due to their desirable optoelectronic properties, high crystalline quality, and the cylindrical geometry that is ideally suited for nanoscale laser sources [9, 10]. The nanowire morphology is also advantageous over thin films for achieving homogeneous $In_xGa_{1-x}N$ alloys [11]. VLS growth has been the most popular, with nanowire high electron mobility transistors and light emitting diodes already demonstrated [10-13]. Recently, vertical arrays of GaN nanowires have been demonstrated using selective epitaxy [14]. In this technique, a nano-patterned silicon nitride layer is used as a mask to precisely determine the location and diameter of GaN nanowires deposited by metal organic chemical vapor deposition (MOCVD) onto a thin GaN layer pre-grown on a sapphire substrate. This approach does not require a metal catalyst and occurs at a similar growth temperature to that used for thin film GaN, i.e. 980°C. The resulting nanowires are dislocation-free, have a [0001] crystal orientation with non-polar $\{1\bar{1}00\}$ sidewalls, diameters that range from 90 nm – 900 nm (as determined by the growth mask) and lengths of up to tens of microns, as determined by the growth time. The long range order and uniformity possible with selective epitaxy are ideal for photonic applications, but first the transport characteristics of these GaN nanowires have to be investigated in detail and simple homojunction devices demonstrated. The deposition conditions that favor quasi-1 dimensional growth differ from conventional,

thin film GaN growth in a number of key parameters such as growth rate and III/V ratio. These growth parameters are also likely to affect the electrical and optical properties [12]. Another important factor is the small diameter and high aspect ratio of the nanowires which alters the electrostatics associated with typical device geometries and leads to reduced Coulombic screening of injected carriers [15-17]. Finally, the high surface to volume ratio of nanowires leads to increased sensitivity to surface states, which can deplete the carriers.

The growth and microstructural characterization of the GaN nanowires has been described in detail elsewhere [14]. Briefly, the nanorods were grown in a commercial metal organic chemical vapor-deposition system on sapphire substrates using selective epitaxy. A 700 nm thick film of GaN was deposited onto (0001) oriented sapphire substrates followed by a 30 nm thick Si_3N_4 film with growth apertures defined by laser interference lithography, and which serves as a mask for the nanorod growth. For this work, the nanorod aspect ratio *R/L* ranged from 0.05 to 0.5, and the nanorods were up to a few microns in length. Doping of the nanowires was achieved during growth by flowing SiH_4 for n-doping, and $Mg(Cp)_2$ for p-doping.

Electrical measurements were performed in two manners. In the first approach, Au/Ti (300 nm/10 nm) electrodes were defined over nanowires randomly dispersed over Si/SiO_2 (100 nm) wafers using optical lithography, followed by electron beam evaporation and lift-off. Prior to metal evaporation, O_2 plasma was used to remove residual photoresist, and a 30 sec dip in 1:1 HCl/H_2O was used to etch the exposed surface of the GaN nanowires. The sample was annealed at 550°C for 15 min. The second approach for electrical measurements involved contacting nanorods directly on the growth substrate with a tungsten STM tip retrofitted inside of a SEM, with a large area Ag paint serving as the second electrode (two Ag paint contacts were made and transport between these was Ohmic). In some of the measurements, the tungsten probe was coated with a thin film of Au (~2nm). However, we found that as long as the STM tip was recently etched and quickly introduced into the vacuum chamber, the results we the same as those with a Au coated probe.

An SEM image of the Au/W probe contacting one of the GaN nanorods is shown in Fig. 1a. This image was collected near the edge of the wafer, where non-uniformity in the silicon nitride mask lead to nanowires with non-uniform dimensions. An SEM image of a nanowire with Au/Ti contacts is shown in Fig. 1b, together with a micro-photoluminescence image of the same nanowire. Photoluminescence spectra showed virtually no yellow luminescence in these nanowires suggesting low level of defects associated with these transitions. Current-voltage (I-V) characteristics for nanowires contacted by the Au/W probe, and with Au/Ti metallurgical contacts are shown in Fig. 2a. It should be noted that in some cases, when first contacted by the Au/W probe, some nanowires exhibited rectifying or highly non-symmetrical I-V characteristics; however, after repeated scans, or by slightly pressing the probe against the nanowire tip, the curves became nearly symmetrical. One of the more extreme cases is shown in the Fig. 2. I-V characteristics for nanowires with Au/Ti contacts were generally stable from the start. In Fig. 2b, I-V curves from six different nanowires are plotted on a log-log plot. These curves show two transport regimes, with $I \propto V$ below ~0.2 V and $I \propto V^2$ for higher voltages. The dependence of the current on the square of the voltage is a clear indication of SCLC. This regime is often observed in situations where carriers can be efficiently injected from the contacts, but the material has either a low free carrier concentration (typical of high band gap semiconductors and insulators) or low carrier mobility, such as often observed in polymers.

SCLC in bulk solids was first analyzed in detail by Mott, who derived the following expression for the current density

$$J = \frac{9}{8}\varepsilon\mu\frac{V^2}{L^3} \qquad (1),$$

where L is the channel length, ε is the dielectric constant, μ is the mobility, and V is the applied voltage. This equation can be easily derived by taking the usual expression for drift current density, $J = en(x)\mu E(x)$, substituting for $n(x)$ using the one dimensional Poisson's equation, $dE/dx = en(x)/\varepsilon$, and integrating.

Equation (1) works well for describing SCLC in a thin specimen with a low aspect ratio, such as a bulk material between two metallic electrodes. However, when applied to our data, the resulting mobility extracted from Eq. (1) would be μ ~10,000 cm^2/Vs, or about 10 times higher than typically observed for very high quality thin film GaN [19]. Mark and Lampert, in their classic text on charge injection in solids, pointed out that equation (1) is not valid for a small diameter, high aspect ratio conductors, such as a semiconductor whisker, but did not provide an explicit model [20].[12] Recently, we have developed a model to describe SCLC in nanowires [17, 21]. By solving the Poisson equation for the electrostatic potential inside a thin wire using the appropriate Green's function and substituting the result into the expression for the drift current, we have shown that SCLC in a specimen where $R/L << 1$ follows the expression

$$J_{nw} = \zeta_0 \left(\frac{R}{L}\right)^{-2} \varepsilon\mu \frac{V^2}{L^3} \qquad (2).$$

In other words, SCLC current density in a nanowire exceeds the current density in a thin film specimen by the ratio of the length to radius squared. (The constant ζ_0 is approximately unity). The reason for the higher-than-expected SCLC current density in a nanowire is the poor electrostatic screening that the injected carriers experience in a high aspect ratio conductor (which is surrounded by air or vacuum). Practically, the relation in equation 2 works well down to an aspect ratio of ~5. Thus, the mobility extracted from SCLC I-V characteristics using equation 1 has to be divided by $(L/R)^2$, which gives an average mobility of 400 cm^2/Vs for the undoped GaN nanowires described in this work. Equation (2) does not contain an explicit expression for the carrier concentration, since in SCLC regime the current density is limited by the rate at which *injected* carriers traverse the semiconductor. However, at the transition between Ohmic and SCLC regimes, the two current densities are equal, and one can solve for the carrier concentration once the crossover voltage (V_c) is known [20]. For the nanowire geometry, the expression for the intrinsic carrier concentration is [17]

$$n = \frac{\varepsilon V_c}{eR^2} \qquad (3).$$

Using equation 3, gives a carrier concentration of ~10^{15} – 10^{16} cm^{-3} for the undoped GaN nanowires, consistent with the observation of SCLC.

The presence of symmetric and nonlinear I-V curves in nanowires has been reported extensively in the literature, and has been ascribed to the presence of Schottky barriers at the contacts. Our measurements and theory suggest that SCLC is a likely explanation for this behavior. Contact effects can be further ruled out by controlling the doping of the nanowires and thus the shape of the I-V curve. To this end, we measured the electronic transport across n-doped nanowires and nanowire p-n junctions. As shown in Fig. 3, the I-V curves for heavily n-doped and pn junction GaN nanowires display linear and diode behavior, respectively, as expected based on the doping (these curves are stable, and do not show significant change with repeated cycling of the bias). The inset in Fig. 3 shows the forward portion of the pn-junction I-V data on a log-linear scale, indicating that the I-V characteristics are exponential, as expected for a diode. These measurements indicate that the nanowire itself governs the electronic transport properties, and not the contacts.

3. Transport in InAs nanowires grown by VLS

Interest in InAs nanowires is motivated primarily by the high carrier mobility and the direct band gap characteristic of this semiconductor system; potential applications of InAs nanowires include high speed FETs and infrared detectors [22-24]. Virtually all InAs nanowires to date have been synthesized using Au-catalyzed VLS growth or a similar mechanism (i.e. VSS). A number of group carried out extensive characterization of the transport characteristics, and reported mobilities that ranged from few tens to few thousands cm^2/Vs, values which are substantially below those observed for bulk InAs and which decreased with decreasing diameter [26, 27]. Furthermore, InAs nanowires grown without intentional dopants, generally exhibit n-type conductivity [27]. Both of these observations, i.e the

decreasing mobility and the n-type conductivity, have been linked to the tendency of InAs surfaces to be accumulated, leading to increased carrier-surface scattering as the nanowire diameter decreased [28].

Single crystal InAs nanowires were grown in a process that is detailed elsewhere [29]. Briefly, a (111) GaAs(B) substrate was coated with a 1 nm Au layer and heated in the presence of AsH_3. This caused the formation of AuGa seed particles on the substrate surface. Upon exposure to $(CH_3)_3In$, InAs nanowires grew from the AuGa seeds. The nanowires had an average length of ~ 15 μm, a diameter tapering from ~150 to ~50 nm, and a surface coverage of ~ 0.2 μm^2.

Electrical characterization of the InAs nanowires was performed by contacting individual nanowires directly on the growth substrate with the SEM-retrofitted nanoprobe, as well as using bottom-gate FET geometry. FET devices were prepared by dispersing InAs nanowires onto n+ Si substrates with 100 nm of thermal oxide. Negative photoresist (Futurex) was used to define an intedigitated, individually addressable electrode pattern with widths of 2 mm and gaps of 2 and 4 mm. Prior to metal deposition, the nanowires were briefly etched in 10 % HF. Au/Ti (10 nm/300 nm) electrodes were evaporated followed by lift off in acetone, and a rinse in isopropanol and nitrogen dry. Electrical characterization of the FET devices was carried out using a computerized data acquisition board (National Instruments PCI), and a current amplifier (Ithaco 1211). Source drain current versus gate bias curves were collected at a source-drain bias of 0.1 V, and a gate bias scan rate of 0.1 V/sec.

Source-drain current (I_{sd}) versus source-drain bias (V_{sd}) curves collected at three different gate voltages for one InAs nanowire are shown in Fig. 4a, together with an SEM image of the NWFET. These curves show that the nanowire is indeed n-type and that the I-V characteristics are indeed linear in this low-voltage regime (≤100 mV). The I_{sd} versus gate voltage (V_g) plot is shown in Fig. 4b. The carrier mobility was calculated from the slope of the I_{sd}-V_g curves using the equation (4),

$$\mu = \frac{L^2}{CV_{sd}}\left(\frac{dI_{sd}}{dV_g}\right) \qquad (4)$$

Where L is the channel length, and C is the capacitance calculated according to equation (5),

$$C = 2\varepsilon\varepsilon_o \frac{L}{\ln\left(2t/R\right)} \qquad (5)$$

where t is the oxide thickness (100 nm) and R is the nanowire radius. The free carrier concentration was calculated from the threshold voltage (the voltage necessary to turn off the NWFET) according to $n_0=CV_{th}/e$. These values agreed well with the carrier concentration calculated using the mobility and the 2-probe conductivity based on the I_{sd}-V_{sd} curves.

Nanoprobe I-V curves collected for three different nanowires are shown on a log-log plot in Fig. 5, with an image of the probe contacting one of the nanowires shown as an inset. The current scales linearly with the voltage at low bias, and as voltage squared at higher bias, as was observed for GaN nanowires. Although the InAs nanowires are expected to have higher free carrier concentration due to the lower band gap and an accumulated surface, the very high aspect ratio of the InAs nanowires, ~200, substantially reduces the cross over voltage from Ohmic to SCLC. The carrier concentration and mobility calculated using equations (2) and (3) are shown in Fig. 6a. The carrier concentration ranges from $0.5\times10^{17}/cm^3$ to $2.5\times10^{17}/cm^3$, while the mobility ranges from ~10 cm^2/Vs to ~3500 cm^2/Vs. The carrier concentration and mobility measured using the FET geometry for nanowires from the very same growth specimen are shown in Fig. 6b, with an inset of one of the FET devices. Comparison of the two sets of data immediately reveals that while they agree in magnitude, the scatter in the FET results precludes any conclusion regarding trends. The nanoprobe data, on the other hand, does indicate a trend of increasing mobility and decreasing carrier concentration with increasing radius. The nanoprobe data as well as the trend are in reasonable agreement with recent measurements reported by Dayeh et al. who investigate transport in VLS InAs nanowires using field effect transistor geometry [27]. The considerably higher scatter in the FET data is likely due to nanowire surface contamination, which can substantially affect the FET transfer characteristics. It is further worth noting that presence of a conducting gate in close proximity to the nanowire will partially shield the carriers, thus increasing the V_c to higher values (at

which point Joule heating or other effects may play a role), which is why SCLC may not be observed for gated nanowire specimens.

The observed increase in n as r decreases is consistent with the fact that the Fermi level in InAs is pinned in the conduction band, leading to an accumulation layer near the surface of the nanowire. Using a simple geometrical argument, we fit n versus r data using the expression $n = N_{bulk} + 2N_{SS} / r$, where N_{bulk} is the bulk density of ionizable impurities (or defects) and N_{SS} is the surface state density responsible for pinning the Fermi level. The fit yields N_{bulk}~$1.5\times10^{16}/cm^3$ and N_{SS}~$2\times10^{11}/cm^2$.

4. Au catalyst-Ge nanowire Schottky diodes

The electronic structure and transport in metal/semiconductor contacts has been the subject of intense investigation for almost a century, and continues to draw attention today, motivated by fundamental scientific questions about the nature of buried heterointerfaces and their technological importance in applications such as high speed rectifiers, mixers, and detectors. As device dimensions shrink below 45 nm, and as new materials with novel composition and geometry are explored for 'next generation applications, the underlying physics of contact formation and carrier transport needs to be re-examined. Indeed, models based on solutions to Poisson's equation for the metal making an end contact to a nanowire concluded that the junction conductivity should decrease with decreasing diameter [31]. Testing these models using top-down fabrication requires high end lithography, etching, and other specialized processing which invariably results in some damage to the resulting nanostructure surface. The VLS nanowire growth, on the other hand, naturally results in a vertical, quasi-1 dimensional semiconductor nanostructures with a top metal contact, and sidewalls which are free from processing damage and chemistry. Our nanoprobe is ideally suited for characterizing the transport in such a system. The ability to manipulate and position the nanoprobe on particular nanowires inside of a SEM allows one to record the I-V curves of a large number of nanowires and at the same time measure the nanowire dimensions. Thus, one can correlate the measured I-V characteristics with the nanowire diameter, length and aspect ratio. Furthermore, a reliable, low resistance back Ohmic contact can be made to the large

area substrates, thus ensuring that the I-V curves are dominated by the characteristics of the metal-nanowire interface.

The synthesis of Ge nanowires is described in detail elsewhere [32]. Briefly, the growth was performed in a cold wall CVD system at a temperature of ~375 ^{o}C and total pressure of 1.5 Torr. A 30% GeH_4 precursor in H_2 along with 100 ppm PH_3 in H_2 as the source of the n-type dopant was used with the gas flows set for a 1:2×10^{-3} P to Ge atom ratio. Au colloids were used as the catalytic growth seeds on heavily n-doped Ge (111) substrates with acidified deposition of the colloids immediately prior to introduction into the growth chamber to achieve predominately vertical nanowire growth. Based on previous results [33], we estimate that the carrier concentration is on the order of 10^{18}–10^{19} cm^{-3}.

A SEM image of the Au coated W nanoprobe near as-grown Ge nanowires is shown in the inset of Fig. 7(a). Most nanowires are ~100 nm in height and have diameters from 20–150 nm. A hemispherical Au nanoparticle caps most of the nanowires. The I-V characteristic for one of the nanowire (diam. 54 nm) is shown in Fig. 7a. The characteristics are those of a diode, as observed in almost all of the nanowires. This rectifying behavior is consistent with that observed at bulk Au/Ge interfaces [34], where a large Schottky barrier of 0.59 eV is present, and is nearly independent of the type of metal due to strong Fermi level pinning close to the Ge valence band. Our observations are also consistent with atom-probe tomography measurements [33] and with high-resolution transmission electron microscopy which indicated an abrupt interface between the Au-catalyst nanoparticle and the Ge nanowires [35]. Fig. 7b shows I-V curves for four other nanowires plotted on a log-normal plot. Inspection of the data in Fig. 7b leads to two surprising observations: (1) the current at zero bias increases and (2) the slope of the forward current versus bias decreases with decreasing diameter. The inset in Fig. 7b shows the diode ideality factor plotted versus diameter for a large number of nanowires, and captures the decreasing slope behavior evident in the I-V curves. This is contrary to most models of transport in nanowires, where the increased importance of surface scattering reduces the small-bias conductance density when the diameter is decreased. In addition, the phenomenon cannot be explained based on a reduction of the effective

Schottky barrier height due to increased tunneling at smaller dimensions because the depletion width actually increases with decreasing diameter [31, 36].

The trend in low bias conductivity for the entire set of Au/Ge nanowire contacts in described here is summarized in Fig. 8. To understand the results presented in Fig. 8, we consider the main carrier transport mechanisms characteristic of metal/semiconductor junctions: thermionic emission, tunneling, recombination in the space-charge region, and recombination in the neutral region [30]. As we already mentioned, tunneling can discounted as the main transport mechanism in our case since the depletion width increases with decreasing diameter, thus lowering the tunneling probability. Thermionic emission, too, can be discounted, since the zero bias conductivity calculated by differentiation of the thermionic emission formula and setting V=0, $dJ / dV_{V=0} = \left(eA^{*}T^{2} / kT \right) \exp\left(-\phi_{b} / kT \right)$ where A* is the Richardson's constant for Ge (50 A/cm^2K^2), is the temperature, k is the Boltzmann constant, and ϕ_b is the Schottky barrier (0.59 eV), predicts a current density of ~0.01 A/cm2, or ~100× lower than what we observe experimentally. Recombination in the neutral region also gives a zero bias conductivity that is at least two orders of magnitude too low [36]. Thus, the only mechanism left is electron-hole recombination in the depletion region. This transport mechanism, which is frequently observed in situations with a relatively high Schottky barrier height and a low band gap [37] as is true for Au/Ge contacts, is characterized by the expression,

$$J_{rw} = J_{o} \left[\exp\left(\frac{eV}{2kT} \right) - 1 \right] \quad (6),$$

where J_o depends on the depletion width, W, and the minority recombination time, τ, according to $J_{0} = eN_{d}W / \tau$. It is also worth noting that the denominator in the exponential brackets of eq. (6) is 2kT, which corresponds to an ideality factor of 2, consistent with our large diameter limit.

One route to obtain further insight into the trends illustrated by Figures 7 and 8, is to evaluate the following expression for the small bias conductivity [30],

$$\left. \frac{dJ_{rd}}{dV} \right|_{V=0} = \frac{e}{kT} \frac{1}{\tau(d)} \int_{0}^{L} \frac{n_{i}^{2}}{n(z) + p(z) + 2n_{i}} dz$$

(7),

where n(z) and p(z) are the electron and hole concentrations as a function of distance into the semiconductor normal to the interface, and τ is written explicitly as a function of diameter. The key to solving this equation is finding an expression for the charge carriers as a function of z. This in turn requires a self-consistent solution to Poisson's equation and an expression for the nanowire local charge density shifted by the electrostatic potential. The appropriate boundary conditions for this calculation are (1) the electric field at the nanowire surface is discontinuous by the difference of the Ge dielectric constant and that of vacuum; (2) the nanowire/protrusion interface is governed by Fermi level pinning such that the Fermi level is 0.59 eV below the conduction band edge; (3) at the nanowire/substrate interface the potential is such as to give a charge neutrality with a doping of 10^{18} cm^{-3}; (4) far from the nanowire in the radial direction the electric field vanishes. Since this calculations has already been discussed in detail elsewhere, here we just present the results, which are illustrated in Fig. 9. Specifically, the Fig. 9 shows that the depletion width W increases from ~30 nm for a 90nm nanowire to almost 100 nm for a 30 nm nanowire. Thus, the increase in junction conductivity with decreasing diameter can be partially accounted by the increase in the depletion width. The dashed line in Fig. 8 represents the zero bias conductivity which includes the increase in W with decreasing diameter. To account for the much larger increase in zero bias conductivity observed experimentally, the contribution of the recombination time t has to be considered. It is well known that unpassivated semiconductor surfaces represent excellent sinks for minority carriers [30]. In bulk systems, the surface-to-volume ratio is a constant, however, in nanowire, the surface-to-volume ratio increases as the diameter becomes smaller, thus leading to a dependence of the recombination time on the nanowire diameter. Formally, this problem can be solved by considering an infinitely long nanowire into which carriers of density n_0 are injected initially. These carriers relax by diffusing through the nanowire and recombining at the surface and in the bulk. The carrier time and spatial dependence satisfy the diffusion equation $\partial n / \partial t = D\nabla^2 n - n / \tau_{bulk}$ where D is the

diffusion constant [38]. Solution to this equation in the limit of s<<D/d, where s is the surface recombination velocity (for D~50 cm^2/s, D/d~10^7cm/s, or $\times 10^2$ typical s values for Ge), is the following [36],

$$\frac{1}{\tau} = \frac{1}{\tau_{bulk}} + \frac{4s}{d} \qquad (8).$$

A numerical fit of equation (8) to the experimental data in Fig. 8 yields a recombination velocity of 2×10^5 cm/s, in excellent agreement with a value recently measured by ultrafast pump-probe spectroscopy on nanowires prepared in the same growth chamber [39].

In addition to increasing conductivity, our results also show a clear trend in the ideality factor (inset, Fig. 7a). In other words, as the nanowire diameter decreases below ~80 nm, the bias dependence in the exponential changes such that n>2. For bulk semiconductors, the depletion width depends on the square of the applied bias, i.e., $W_{bulk} = \sqrt{2\varepsilon\varepsilon_o \left(V_{bi} - V\right) / N_d e}$, where V_{bi} is the built-in voltage and N_d is the dopant concentration. However, in the quasi 1-dimensional regime, $W_{nw} \approx d \exp\left(8\varepsilon_o W_{bulk}^2 / \varepsilon d^2\right)$, or $W_{nw}(V) \sim \exp\left(-16\varepsilon_o V / eN_d\right)$, leading to $J_{rw} \sim \exp\left(eV / n_{eff} kT\right)$, where $n_{eff} = 2 / \left(1 - l^2/d^2\right)$, and where $l = \sqrt{32kT\varepsilon_o / e^2 N_d}$ [36]. A fit of this last expression to the experimental data yields l=22 nm, which compares reasonably well with the theoretically predicted value of 7 nm.

Summary

We have demonstrated how transport in different types of nanowires can be characterized using a nanoprobe, a relatively simple tool which can be retrofitted into most modern scanning electron microscopes. Furthermore, we have shown that transport of carriers in nanowires is strongly dependent on dimensions, and become space charge limited even at moderate current densities due to reduced screening. Finally, we have shown that Au catalyst/Ge nanowire contacts are rectifying, and that their

characteristics are also strongly dependent on the nanowire diameter due to increasing depletion width and surface carrier recombination.

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Figure captions

1.(a) A Au coated W nanoprobe contacting a GaN nanowire; (b) A GaN nanowire contacted with Au/Ti metallization, with an inset showing photoluminescence collected with He-Cd 325 nm excitation.

2. (a) I-V characteristics collected for a GaN nanowire with lithographically defined and annealed Au/Ti electrodes and one contacted using the Au/W nanoprobe, showing both initial I-V and one collected after numerous cycles; (b) several I-V curves collected using either Au/Ti electrodes or the nanoprobe plotted together with lines corresponding to $I \propto V$ (slope=1) and $I \propto V^2$ (slope=2)

3. I-V curves for a pn-junction and n^+-doped GaN nanowires. The inset shows the forward bias diode I-V on log-normal plot.

4. (a) Source-drain current versus source-drain bias for an InAs NWFET (SEM inset); (b) Source-drain current versus gate bias for the same device (source-drain bias=100 mV).

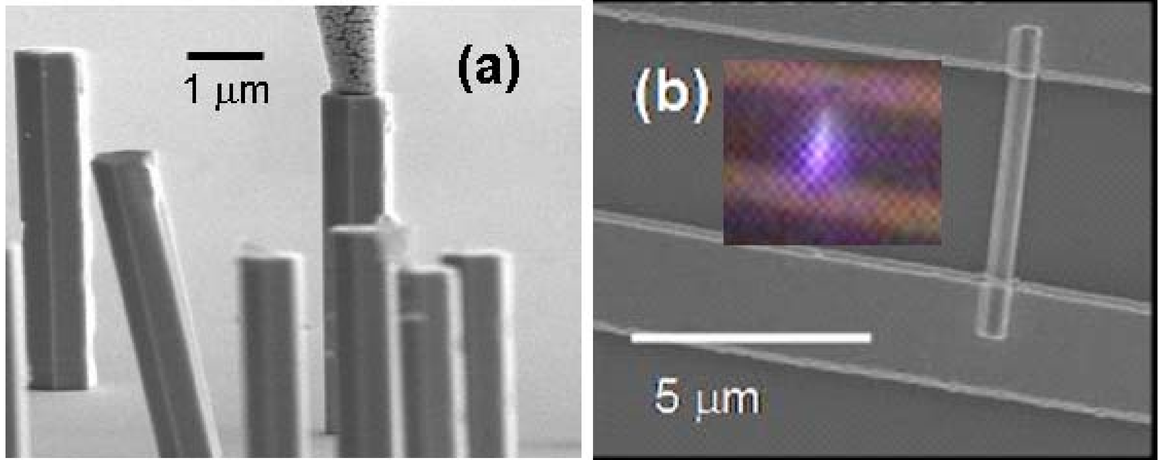
5. I-V curves for three different InAs nanowires plotted on a log-log plot with insets showing SEM of one of the wires contacted with a W probe (upper), and an inset showing the I-V data on a linear current-voltage scale (lower).

6. (a) Carrier concentration for InAs nanowires versus the nanowire radius determined using the nanoprobe from the Ohmic-to-SCLC crossover voltage and equation (3). Inset shows the mobility versus the radius; (b) Carrier concentration determined from the FET threshold voltage

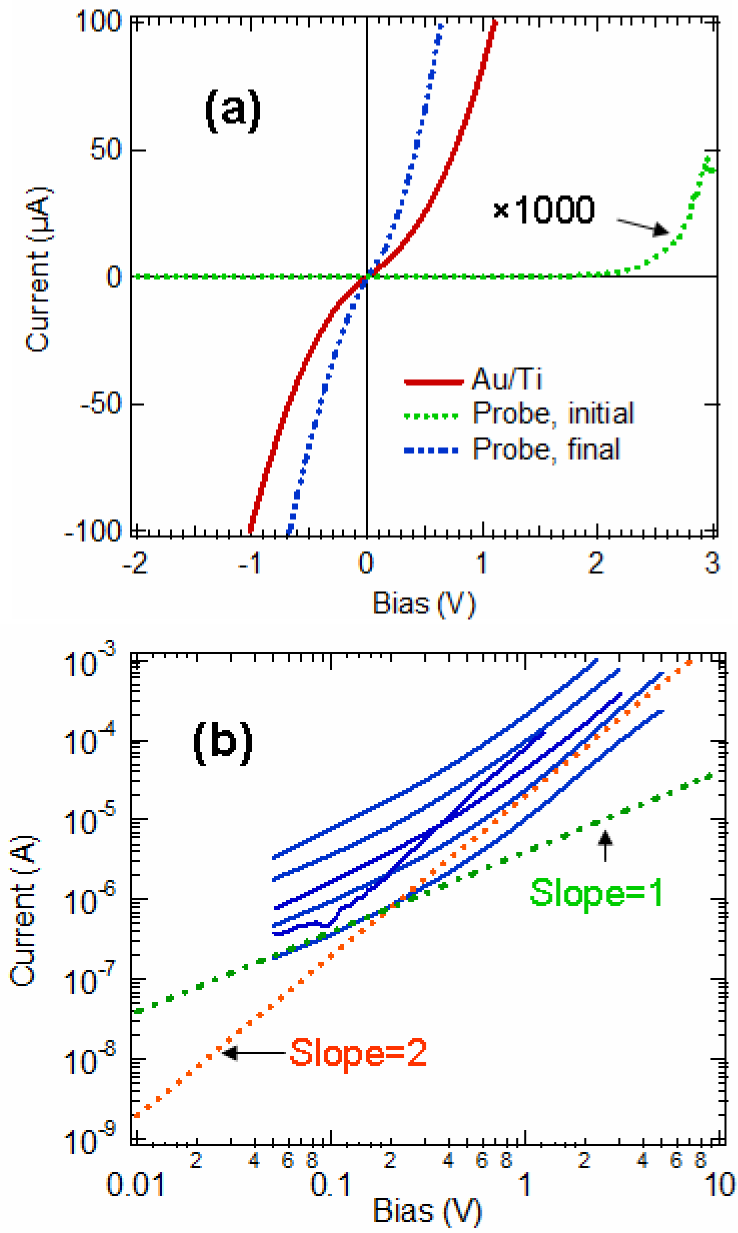
7. (a) Current-voltage characteristics for a Ge nanowire of 54 nm diameter. The inset is a SEM image of the Au-coated W tip and several Ge nanowires. (b) Current-voltage curves on a log scale, for four nanowires of different diameters. The inset shows the ideality factor measured at forward bias as a function of nanowire diameter (from ref. 36)

8. Small-bias conductance density of the Au-nanoparticle/Ge-nanowire interface as a function of the nanowire diameter. The dashed (solid) line is calculated with a diameter independent (diameter-dependent) recombination time (from ref. 36)

9. (a) Sketch of the system used for the numerical calculations; see text for details. The calculated electric field lines are shown for a nanowire of 30 nm diameter. (b) Calculated charge in the center of the nanowire as a function of distance along the nanowire. (c) Calculated band bending. In (b) and (c) the curves from top to bottom correspond to nanowire diameters of 30, 50, 60, 80, and 90 nm (from ref. 36).



Talin et al., Fig. 1



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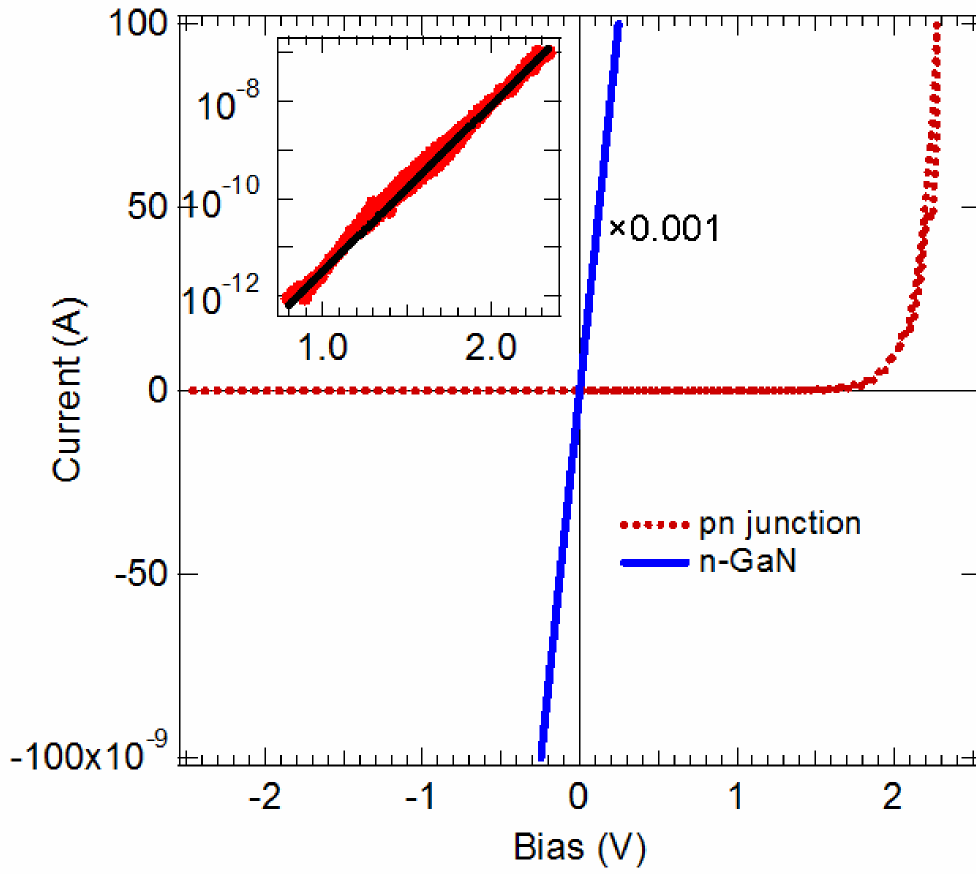

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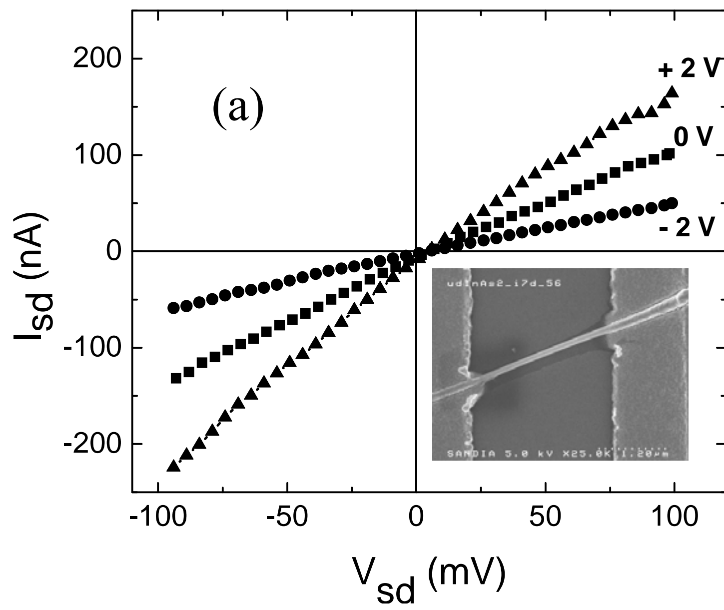

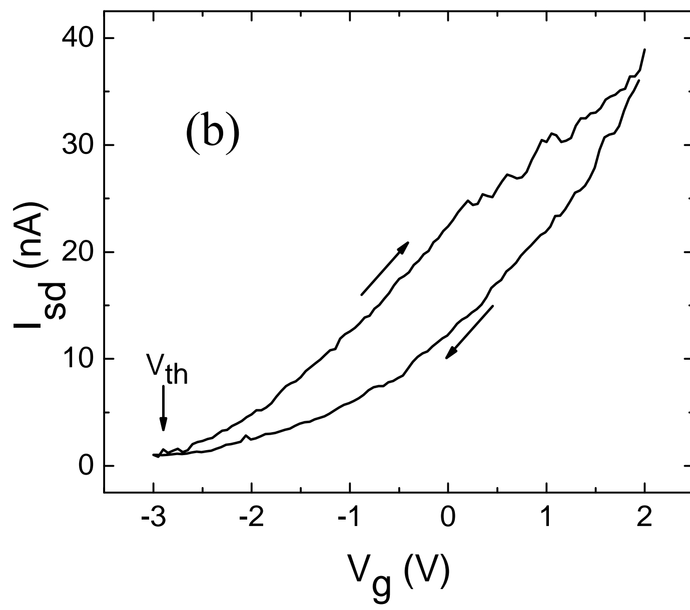

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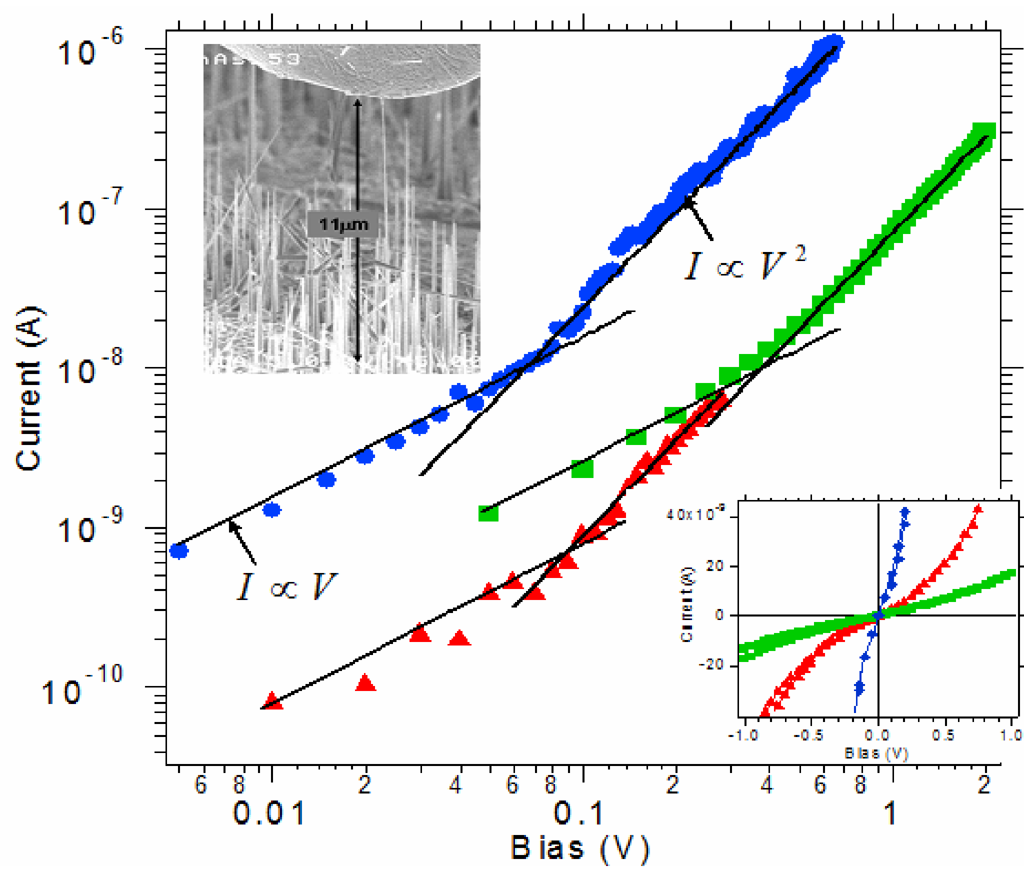
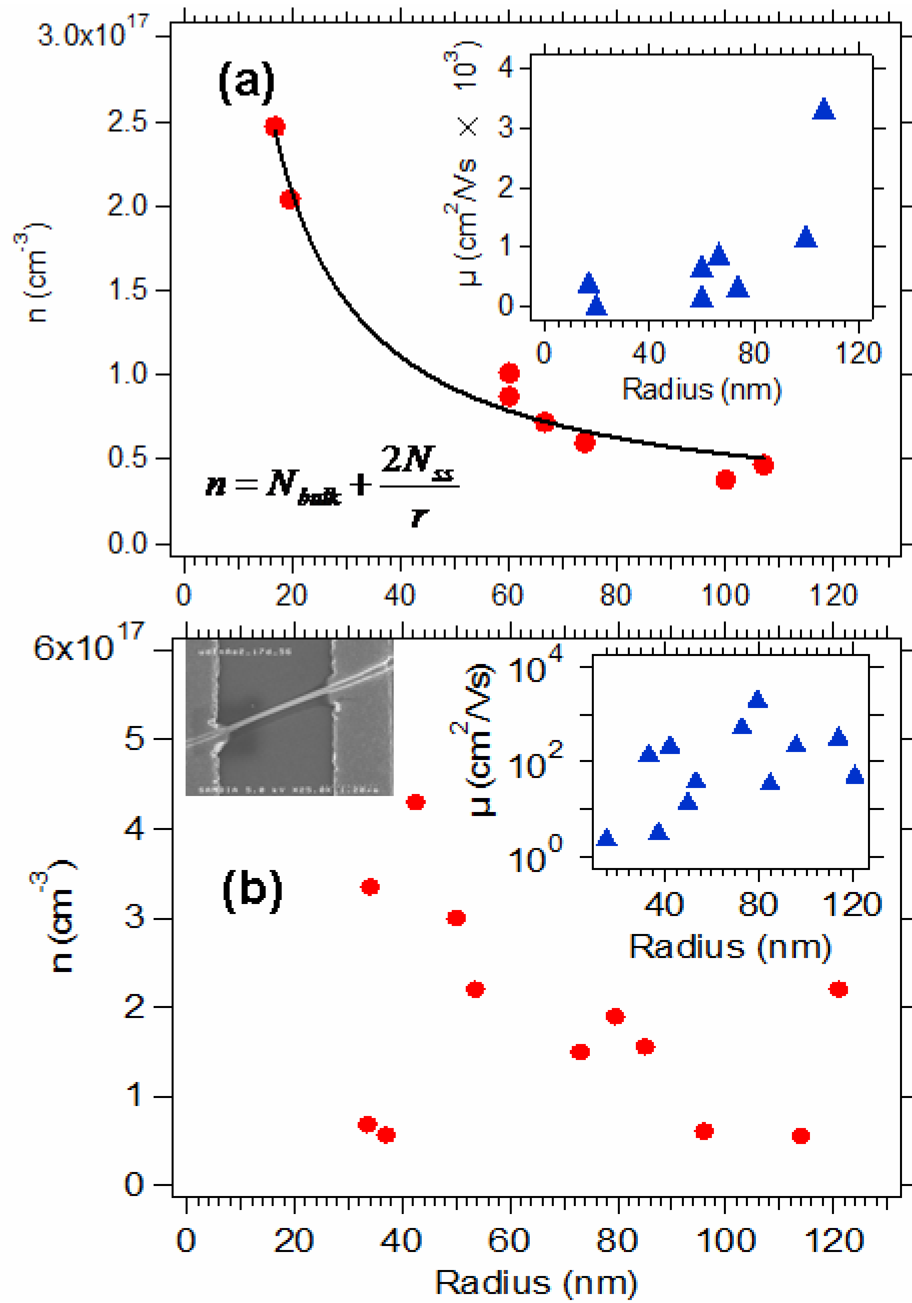


Talin et al., Fig. 5



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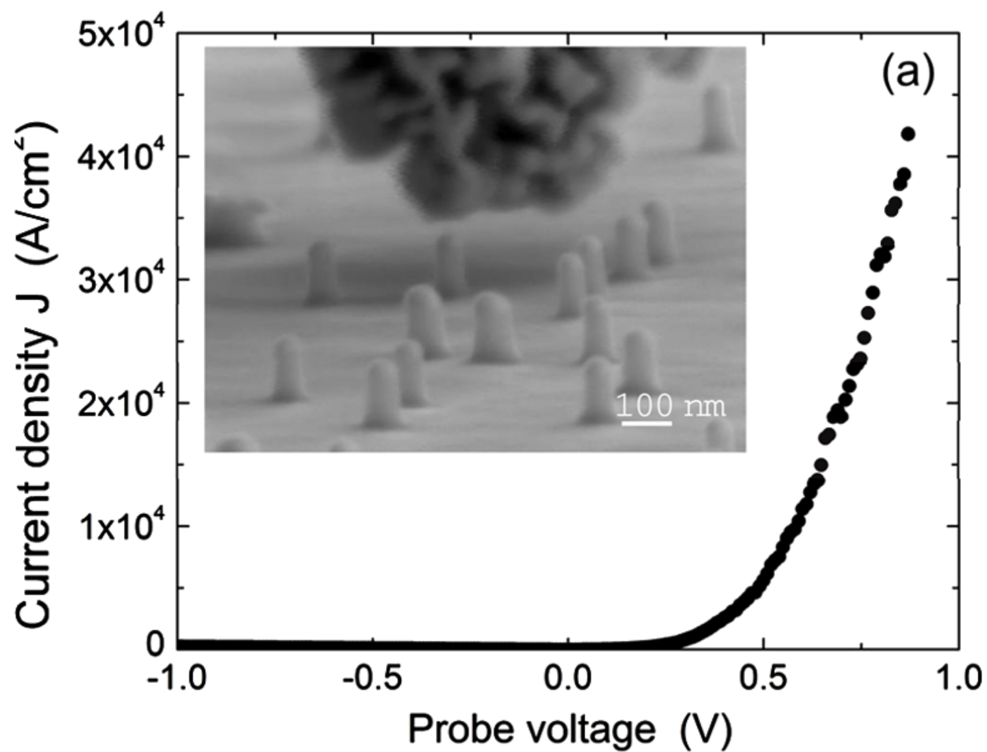
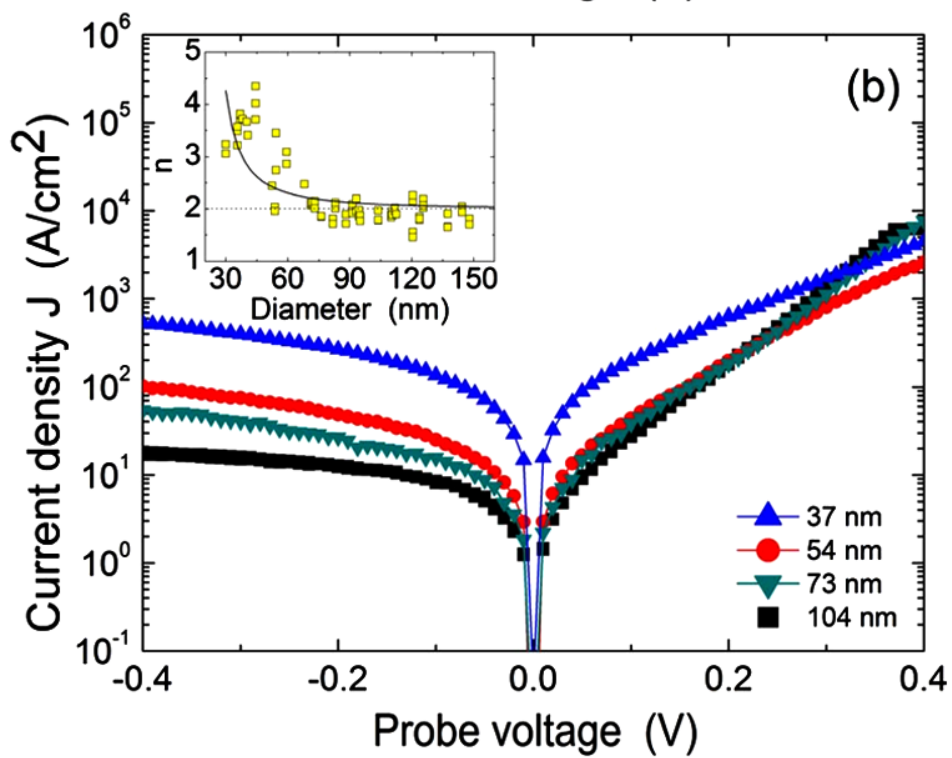
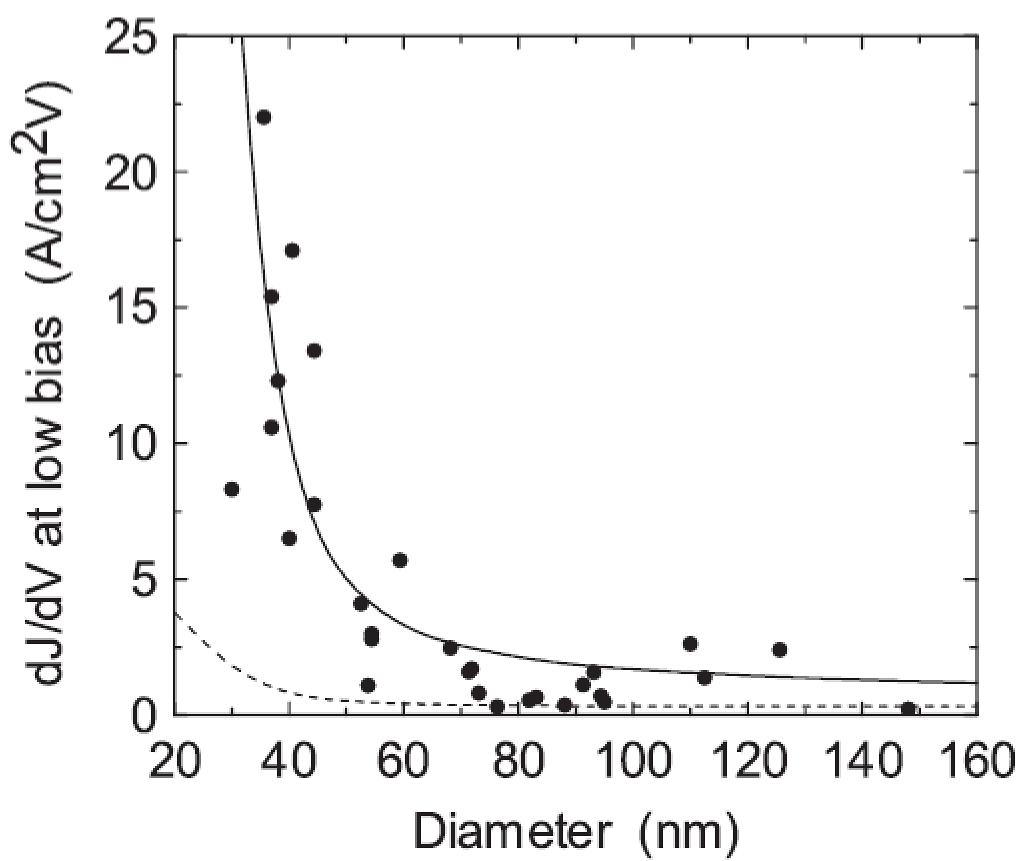




Talin et al., Fig. 7



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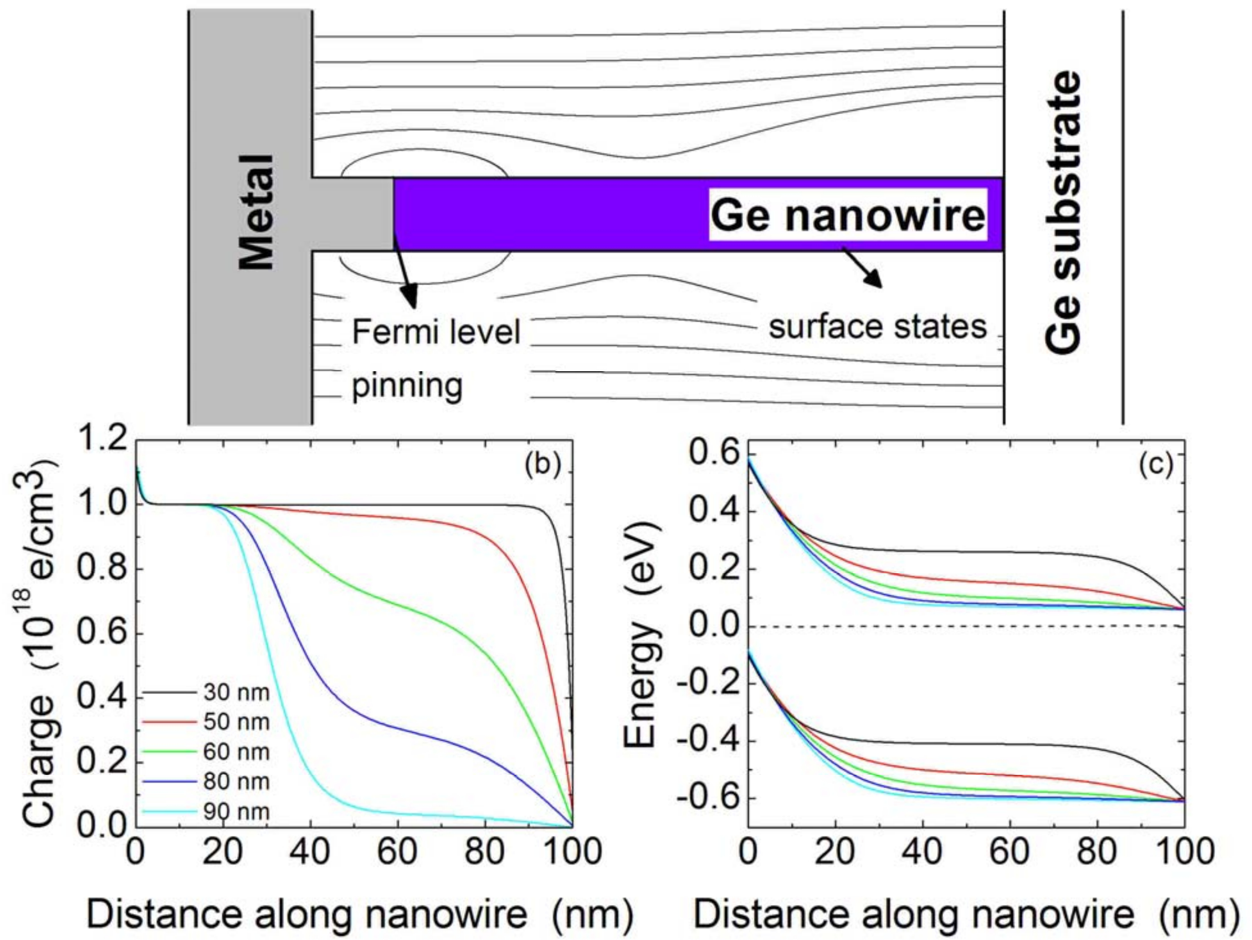

Talin et al., Fig. 9