A Time Synchronization Testbed to Define and Standardize Real-Time Model-Based Control Capabilities in Semiconductor Manufacturing

D. Sharma, D. M. Anand, Y. Li-Baboud and J. Moyne

***Abstract*—Shrinking process tolerances due to decreasing device sizes and increasing chip complexity in semiconductor manufacturing are motivating efforts to improve methods for real-time networked process control. Prior work shows that the lack of precise time synchronization is a critical hindrance to reliable model generation or estimation for process diagnostics and control. This paper first presents an analysis of control data traffic and time synchronization performance over wired and wireless networks to illustrate the need and the challenges in generating high fidelity plant estimates. The paper then discusses a test-bed currently being implemented by the Engineering Research Center for Reconfigurable Manufacturing Systems at the University of Michigan, to explore methods to improve estimator performance using a time-stamped data model.**

Keywords: time synchronization, semiconductor manufacturing, data quality, Equipment Data Acquisition standard, NTP, PTP, time stamping

I. Introduction

Ethernet based networks are widely used for networked control in modern manufacturing plants and are able to provide the quality of service required for close to real time applications. Wireless extensions to Ethernet are also well accepted for control and data acquisition networks where there are no hard, real-time constraints. Typical distribution of delays for wired and wireless ethernet systems are discussed in [6] and [13]. With demands on real-time systems growing, a lot of work is being done to address the non-deterministic delays associated with transmission collision and medium arbitration in the Ethernet technology. One of the more promising strategies is to use a distributed set of controllers embedded in the sensors and actuators. These controllers are able to build a dynamic model of their local environment, by analyzing local sensor data in response to input commands sent to it by the plant level controller. With a good estimate, the controller can interpolate between control inputs, even when messages from the plant level controller are delayed or lost in the network. Model based control at the sensor level opens up a whole new avenue for control design. The cost of embedded software is dropping at a rapid rate allowing additional functions, such as fail safe fault recovery and real-time reconfigurability to be added to the control infrastructure at the lowest level. The quality of model based control though is fundamentally limited by the quality of the 'model'. The model is generated by correlating the local sensor data and remote control data. This requires precise time synchronization between the embedded sensor/actuator node and the remote controller. It is necessary therefore to first quantify time synchronization accuracy for both wired and wireless systems. [6], [13] and [16] discuss jitter in wired and wireless ethernet networks.

Following this introduction, section II discusses time delay distributions in factory control systems showing significant jitter in network traffic in high load conditions. Section III discusses a control testbed being developed at University of Michigan to research precise time synchronization and time stamping methods for real time control. In section IV we discuss the proposed control design techniques for the testbed including Linear-Quadratic-Gaussian (LQG) and Model Predictive Control (MPC) techniques and elaborate on the need for estimation and prediction for precise control. We will also discuss how effects of network jitter on estimation can be minimized by accurate time stamping.

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II. Performance evaluation of networks in semiconductor manufacturing

Evaluation of ethernet networks in factory environments would provide us with an understanding of the network delay distributions in nominal and high load conditions. To develop a measure of the jitter in wired and wireless ethernet networks in factory conditions we developed an equipment data acquisition (EDA) system simulator. Semiconductor manufacturing traffic was implemented using SEMI specifications. SEMI interface 'A' provides a suite of specifications [1], [2], [3], [4] for communication between data sources on the plant floor and data collectors. More details on the EDA architecture used for simulation are provided in [7]. Analysis of the network traffic and network delay distributions discussed below further demonstrated the need for network time synchronization in factory control systems.

A. Network performance evaluation using EDA Simulation

To study the performance of factory scale EDA communication we used the EDA simulator introduced in [12]. The EDA simulator is a C++ and Java native interface implementation of the EDA communication infrastructure [4]. The simulator recreates network traffic expected from a real world, factory scale EDA implementation, including various data types such as event reports, trace reports, and exception reports. Network traffic was monitored in real time using analysis software

TABLE I
COMPARISON OF PERFORMANCE PARAMETERS FOR WIRED VS. WIRELESS DATA ACQUISITION. 1I CORRESPONDS TO 1 INTELLIGENT NODE, SIMILARLY 50D CORRESPONDS TO 50 DUMMY NODES.

Wired parameters	T_{mean}	T_{max}	σ_T
1I	5.4ms	6.2ms	0.4ms
1I+1D	5.6ms	6.3ms	0.3ms
1I+50D	5.6ms	6.4ms	2.5ms
1I+100D	5.6ms	6.4ms	2.4ms
1I+200D	5.7ms	6.3ms	3.2ms

Wireless parameters	T_{mean}	T_{max}	T_{min}	σ_T
1I	9.4ms	12.7ms	7.4ms	1.1ms
1I+1D	8.2ms	12.3ms	7.1ms	1.2ms
1I+20D	9.3ms	39.8ms	7.1ms	5.4ms
1I+30D	10.7ms	43.5ms	7.1ms	7.8ms
1I+50D	18.5ms	82.3ms	7.1ms	18.4ms
1I+100D	27.5ms	85.6ms	7.2ms	23.9ms
1I+200D	46.1ms	402.4ms	7.2ms	121.4ms

developed in-house in conjunction with the commercial network protocol analyzer *Wireshark* [1]. Running an independent protocol parser and delay measurement tool allowed the EDA functions to execute unhindered. EDA simulation was performed over wired ethernet and IEEE 802.11G wireless network. We will use packet delay and jitter to characterize the performance of a network. Jitter is defined as the variation in packet delay and shows the uncertainty in communication delays. A comparison of performance is shown in table I. It clearly shows a marked increase in jitter as network traffic increases. The issue is more severe in wireless than in wired having both greater mean delay (T_{mean}) (close to double) and an order of magnitude higher standard deviation or jitter (σ_T). This increase in jitter shows increased non-determinism in the networks and can lead to decrease in performance and stability of control systems. We believe that network wide time synchronization and time stamping can compensate for jitter in communication channels.

III. REAL-TIME SYNCHRONIZED CONTROL TESTBED

Real-Time Synchronized Control (RTSC) Testbed is a platform developed at the Engineering Research Center, University of Michigan to test networked control strategies using time synchronization. Real time control over sensor networks is a key challenge in the semiconductor industry. RTSC testbed will be used to research techniques to time synchronize sensor and controller clocks over networks to microseconds accuracy using precision time protocol. Ultimately the testbed will be utilized to specify, validate and promote standards for semiconductor manufacturing time synchronization at the device level.

A. Testbed Hardware

RTSC testbed consists of two DC motors each mounted with a metallic disc. Each DC motor is also equipped with an optical encoder and a photo indicator generating one pulse per revolution. The motors are powered using 25 KHz Pulse Width Modulated (PWM) signal generated by a controller board and amplified using an H-bridge. Each DC motor with its sensors is connected to a controller board handling input and output. The real time testbed controller can run on one of the boards connected to the DC motors or can run separately on a different board. Sensors, actuators and controller communicate over the network. This testbed can use wired and wireless ethernet sensor networks to compare time synchronization and control performance. Each controller board is a Freescale device providing a comprehensive IEEE 1588 precision time protocol (PTP) solution. The hardware components include a Coldfire microprocessor and ethernet physical-layer transceiver with PTP support provided by National Semiconductor. It also provides General Purpose Input Outputs, Timers etc required for embedded control applications.

[1]Wireshark is distributed under the GNU general public license. *www.wireshark.org*

B. Control Problem

Our goal is to phase synchronize the two discs over the network. One motor acts as the plant while the second motor provides tracking reference. The input to the plant is voltage and the output is motor shaft position. Phase synchronization in this plant is a DC Motor position control problem. This system has an inherent pole at the origin. The pole will act as an integrator to control inputs adding/increasing the effect of jitter. The control problem will be able to clearly show the improvements in control performance using time synchronization. Our attempt is to synchronize the two discs at high RPMs close to 5000. Network throughput restrictions will limit the amount of sensor feedback data being sent at such high speeds. A state estimator will be implemented to provide full state feedback.

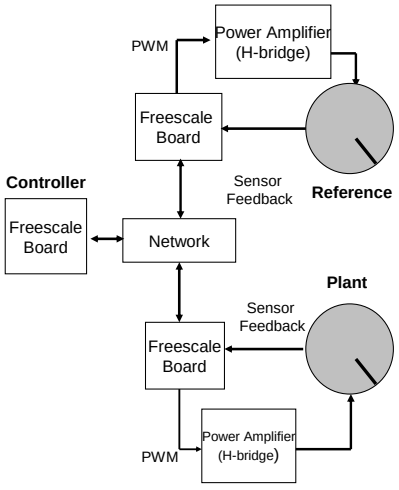

Fig. 1. A schematic of the testbed showing plant, controller boards and network components

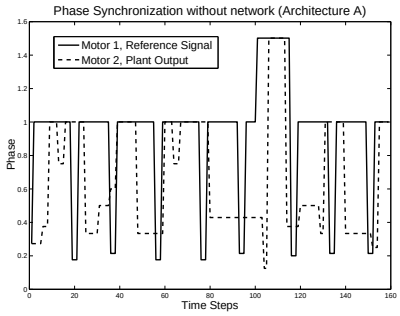

Fig. 2. Tracking control using a preliminary proportional derivative controller on architecture A (sensors and actuator hardwired to controller). Uncertainty in plant dynamics makes it difficult to achieve good tracking

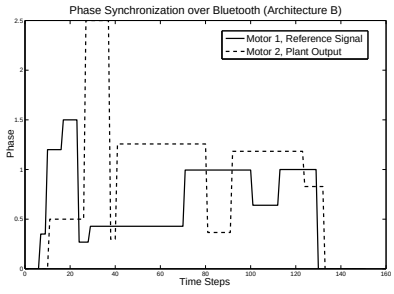

Fig. 3. Tracking control using a preliminary proportional derivative controller on architecture B (sensors and actuator communicating over a wireless Bluetooth channel). Latency and jitter in Bluetooth communication degrades control performance

C. Preliminary Results

A preliminary proportional-derivative (PD) position controller was implemented on the above hardware. Controller performance in networked and non-networked architecture were compared using the preliminary controller. In architecture A, the sensors and plant actuator are hard wired to the controller while in architecture B the sensors and plant actuator are connected to the controller over a Bluetooth (IEEE 802.15.1) network. Figures 2 and 3 show some of the results from the analysis. Figure 3 shows a significant degradation in performance due to latency and jitter in Bluetooth communication. Preliminary analysis showed that significant uncertainty exist in plant dynamics and more advanced control strategies will be needed to achieve precise tracking over a network.

IV. Proposed control design for RTSC testbed

RTSC testbed control design problem can be posed as a Linear-Quadratic-Gaussian (LQG) optimal control problem. An LQG controller is a combination of Linear-Quadratic Regulator (LQR) and Linear-Quadratic Estimator (LQE) or Kalman filter. Quadratic optimization functions are traditionally used to develop feedback control laws for linear systems. The availability of incomplete state information and presence of Gaussian noise in measurements makes a good case for the use of Kalman filters [9]. However for a networked control system (NCS), network delay jitter in communication introduces additional noise in sensor data. Results from [6] and [13] show that network delay distributions under high load may be non-Gaussian and unpredictable. Sensor data being received by the estimator in these network conditions has noise which is difficult to model, making it extremely challenging to design an accurate estimator. Effects of jitter on estimation are discussed in more detail in section IV-A.

Sampling rate of an NCS control loop is restricted by delay in the communication networks. Traditional control networks may force the sampling time to be always more than 4-5 milliseconds. Precise control might require a faster sampling rate due to uncertainty in plant dynamics and disturbance. We propose to use model predictive control techniques to augment the LQG controller [14]. Model predictive control (MPC) techniques are widely used in process control. A model predictive control uses a local model of the plant to predict future controller input sequences. These future controller inputs are sent to the actuator buffer when the communication channel is open. Since communication protocols can handle larger data sizes without significant deterioration in performance [6], [10] and [13] sending multiple control commands does not put any additional traffic load on the network. However reliable model of plant dynamics and accurate output estimation/prediction is essential to MPC. Therefore a key challenge in design of real time NCS controllers and one of our research focus is to ensure accurate estimation over noisy communication channels.

A. Effect of network jitter on estimation

A central part of the Kalman filter and model predictive control is estimation/prediction of output using previous states and inputs. Previous state values are generated from sensor inputs and a key requirement is that the fidelity of sensor data is maintained. One important aspect of this fidelity is the time jitter of the data reported.

Table I shows the change in jitter values as the load on control network increases. Non-determinism in network delays makes controller design difficult. An incorrect choice of design parameters to maximize signal-to-noise ratio will not only introduce bias in state estimation but also can make the estimator unstable [9]. We will work on modifying Kalman filter and using time stamped sensor data to perform estimation [11]. Using IEEE 1588 time synchronization protocol [8] node (sensor, controller) clocks can be synchronized to microsecond accuracy. This will provide us with highly accurate sensor data for estimation even at extremely high sampling rates.

B. Compensating for network jitter using time synchronization

With time stamped data the absolute time at which the data was recorded is conserved despite delays in transmission. Since the controller can reconstruct the exact time at which the data was stamped, it no longer has to rely on the packet's arrival time to estimate the absolute time of data generation. This in itself does not guarantee real time control but will ensure the quality of data required for estimation algorithms discussed in section IV-A. Time synchronization accuracy required for a system will depend on the maximum sampling rate in the system or the minimum time difference between events which need to be monitored. Time synchronization using Network Time Protocol (NTP) was performed on the EDA

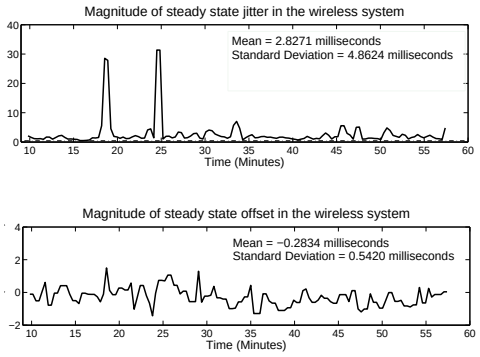

Fig. 4. Time synchronization over IEEE 802.11g wireless link using NTP. Synchronization was performed on 100 EDA nodes from simulation. Results show a mean jitter of 2.8 milliseconds.

simulation experiment discussed in section II-A. Simulation was performed by running 100 server nodes and one client, NTP was implemented on two nodes part of the simulation. Communication delay measurements showed a jitter of 24 milliseconds and large delay outliers. Figure 4 shows steady state magnitude of offset and jitter in the wireless systems. The mean jitter value of 2.8ms in the wireless case is a worst case upper bound on the uncertainty in time accuracy, and is still order of magnitude better than the communication delay jitter. The actual accuracy of synchronization may be better than 2.8ms because of the existence of smoothing and filtering algorithms in NTP [15]. Simulation results show that time synchronization can be used to compensate for delay jitter. If control systems can be designed to take advantage of the time stamped data, precise real-time control can be implemented on noisy communication channels. We will work on developing techniques to perform low level time stamping and precise time synchronization to meet the requirements of semiconductor manufacturing. To achieve high fidelity of sensor data we will work on implementing time stamping and synchronization at the device level using IEEE 1588 [8]. Successful implementation of these techniques can pave the way for the development of smart sensors which can synchronize to a common clock and perform low level time stamping.

V. Conclusion

In this paper we have described a time synchronization testbed that is being developed to characterize, validate and support time synchronized control capabilities at the device level in semiconductor manufacturing. The testbed features an EDA simulator to provide for characterization of network traffic associated with fab APC, and a time synchronization hardware setup that can be utilized to identify time synchronization requirements and capabilities to support APC elements at the device level. Time synchronization has rapidly moved to the forefront as a data quality issue impacting the ability to achieve robust APC, especially as time constraints become more strict. SEMI has addressed this issue at the factory level with a high level time synchronization standard [5]. As we move closer to the device level, timing requirements are more pervasive, and the need for a non-intrusive standardized synchronization solution is very evident. The IEEE 1588 hardware standard offers promise and is being pursued in many other industries. The testbed effort described herein will help the semiconductor manufacturing industry standardize around IEEE 1588 at the device level, thereby ensuring a higher level of data quality and an improved capability for real-time control and diagnostics systems.

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