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The large-scale integration of high-performance silicon nanowire field effect transistors

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Abstract
In this work we present a CMOS-compatible self-aligning process for the large-scale-integration of high-performance nanowire field effect transistors with well-saturated drain currents, steep subthreshold slopes at low drain voltage and a large on/off current ratio ($>10^7$). The subthreshold swing is as small as 45 mV/dec, which is substantially beyond the thermodynamic limit (60 mV/dec) of conventional planar MOSFETs. These excellent device characteristics are achieved by using a clean integration process and a device structure that allows effective gate–channel–source coupling to tune the source/drain Schottky barriers at the nanoscale.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Self-assembled nanowire field effect transistors (NWFETs) have great potential as active building blocks for nanoelectronic applications. Previous studies [1, 2] have demonstrated high-performance nanowire and nanotube field effect transistors with on/off current ratios $\approx 10^5$ and a subthreshold swing (SS) $\approx$100 mV/dec. Based on this research, NW FETs and devices have been developed as a platform to allow different device integrations for various applications, such as optical sensing/emitting devices and chemical/bio-interacting devices. Yet a CMOS-compatible process for the large-scale integration of self-assembled NWFETs with large on/off current ratios and subthreshold slopes at, or ideally below, the room temperature limits of planar MOSFETs has not been reported. There are still concerns that self-assembled nanowire/nanotube devices can have device performances comparable to conventional planar MOSFETs and that the integration of such devices is compatible with traditional CMOS technology. The ultimate device electrical properties, particular the SS, strongly depend on the details of the device structure and the quality of the semiconductor/dielectric interface. The quality of this interface is directly affected by the fabrication processes. Most of the current research on self-assembled nanowire devices involves harvesting nanowires from the preparation substrate and suspending them in liquid to form a nanowire solution. The nanowires are then deposited from the solution onto device substrates either randomly or aligned by using methods such as fluidic alignment [3], dielectrophoresis [4] or nanoscale probe methods [5, 6]. These harvesting/deposition processes are likely to introduce chemical contaminants, particles and other unknown materials surrounding the nanowires that contaminate their surface. The use of electron beam microscopy to examine the nanowire's position during the nanowire alignment is likely a further source of contamination. Additionally, it is challenging to effectively clean the nanowires after positioning them on device substrates. The nanowires, which are held on the surface weakly via electrostatic forces, can easily be lost under aggressive cleaning, particularly under wet processes and sonication. Thus it is highly likely that the nanowire surface will be left contaminated when the device is made. Such a contaminated surface will substantially increase the nanowire

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device interface state density (D_{it}), which will seriously reduce the device performance, as indicated by the transistor subthreshold swing. Therefore, there are issues about whether self-assembled nanowire/nanotube devices can have high performance and how such 'bottom-up' devices fit into the large-scale integration of CMOS technology.

In this work we report the fabrication and characterization of self-assembled Si NWFETs with excellent current–voltage characteristics, large on/off current ratios ($I_{ON}/I_{OFF} > 10^7$) and steep subthreshold slopes. The Si nanowire (SiNW) devices are fabricated on a whole wafer by using a self-aligning technique with standard photolithographic alignment and metal lift-off processes, enabling the large-scale integration of reproducible, high-performance devices with an average SS of 61 mV/dec at room temperature. With the aid of a second bottom gate the SS can be as small as 45 mV/dec, substantially less than the fundamental thermionic limit (≈60 mV/dec) at room temperature for the conventional planar MOSFETs. Our approach clearly shows that the self-assembled NWFETs can have excellent performance and are compatible with CMOS large-scale integration.

The sharpness of the SS is a critical parameter in determining how small a voltage is used to switch the device on and subsequently how much power is dissipated. The need for lower-power circuitry, particularly for portable applications, is driving the search for devices with sharper SS. However, due to thermodynamic properties, there is a fundamental room temperature limit on the SS for conventional MOSFETs. Pioneering studies have shown that nanotube and nanowire FETs with SS < 60 mV/dec can be achieved based on avalanche breakdown or interband tunneling of the channel in the un-gated regions between the gate and source/drain [7–9]. Typically such devices require large drain voltages for the impact ionization or breakdown and may have large series resistance, non-saturated drain current, small on–off current ratios and ambipolar conduction. The NWFETs fabricated in this work exhibit very sharp SSs and large on–off current ratio as well as some of the excellent characteristics of conventional planar MOSFETs: inversion-mode saturated drain current, low series resistance, low voltage operation and unipolar conduction.

2. Experimental details

To fabricate the nanowire devices, we developed a self-aligning process to fabricate top-surrounding-gate NWFETs with a high-k gate dielectric stack, which is an extension of our previous process on the fabrication of nanowire $SiO_2/Si_3N_4/SiO_2/Si$ (SONOS) memory devices [10]. The 'self-alignment' process by which these devices are fabricated is shown in figures 1(a)–(c). The key steps in this fabrication approach are self-assembling and patterning the SiNWs grown from Au catalyst on pre-defined locations. First, a 50 nm thermal SiO_2 was thermally grown on p-type silicon substrates as the insulator of the bottom gate. Then an Au film (∼1 nm) as the SiNW growth catalyst was patterned on the oxide surface by using photolithographic and metal lift-off processes (see figure 1(a)). The SiNWs were grown in a low pressure chemical vapor deposition furnace, at 420 °C, under 500 mTorr

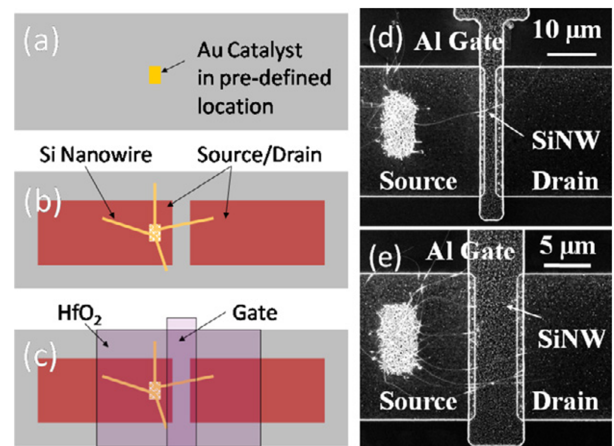

Figure 1. Schematics of self-alignment fabrication processes: (a) Au catalyst is patterned on SiO_2; (b) SiNWs are grown from the Au catalyst and oxidized. Source/drain contacts are aligned and patterned on top of the SiNWs; (c) HfO_2 is deposited and a top gate is patterned on the SiNW. Scanning electron microscope images of typical SiNW FETs with a single-nanowire conduction channel (d) and a multiple-nanowire conduction channel (e).

SiH_4 via a vapor–liquid–solid mechanism [11, 12]. SiNWs of ≈20 μm in length were obtained after growing for 2 h. The diameter of SiNWs is within a range of 5–40 nm, which follows a Gaussian distribution with both the peak and average at ≈20 nm. It is expected that, as the SiNW diameter increases, the whole electrical conduction of SiNW FETs will increase, but the subthreshold slopes and on/off ratios remain the same.

After growth, the SiNWs were then thermally oxidized at 700 °C for 30 min by using dry oxidation. Under these conditions it is expected that a thin layer of oxide (∼3.5 nm) grows on the SiNW surface [13] which improves the interface quality between the SiNW and the subsequently deposited HfO_2 layer. The following compatible fabrication steps were used to pattern the metal contacts (i.e. source, drain and top gate electrodes) on the SiNWs. Lift-off resist (LOR) and photoresist (PR) are applied on the substrate (with nanowires) and defined with photolithographic processes (see figure 1(b)) to form contact patterns for the SiNW FET source and drain. This is followed by a wet etch for 2 min with 2% HF to remove the oxide from the SiNWs and a layer of Al is immediately deposited by thermal evaporation and defined by metal lift-off to form the source and drain electrodes. The Al in the source/drain regions forms Schottky barrier contacts to the SiNWs. A layer of HfO_2 (∼25 nm) is then deposited as the top gate dielectric of the SiNW FET by atomic layer deposition at 250 °C. The formation of the top gate electrode (Al) is similar (minus the HF etch step) to the formation of the source and drain electrodes (see figure 1(c)). Finally, the resulting SiNW FETs were annealed in ambient forming gas (5% H_2 in N_2) at 380 °C for 15 min by using a rapid thermal annealing tool. This step is used to achieve low contact resistance at the electrodes and reduce D_{it} at the gate stack interface [14].

Scanning electron microscope (SEM) images of typical SiNW FETs with a gate-to-source/drain overlap (ΔL) = 1 μm are shown in figures 1(d) and (e) for devices with a single-nanowire and multi-nanowire conduction channel,

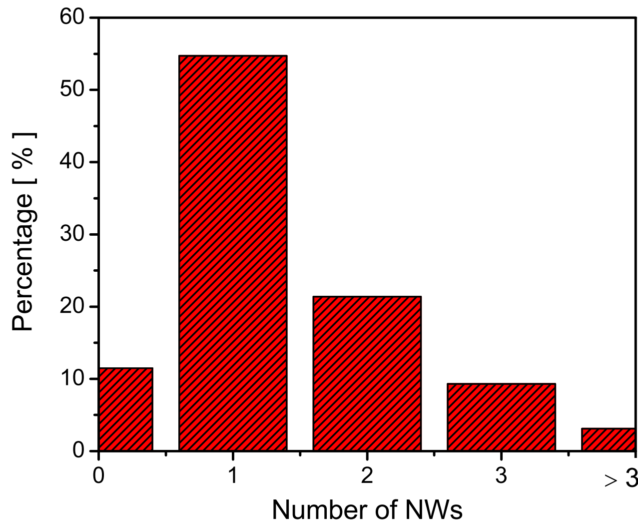

Figure 2. Statistical result: percentage of devices versus the number of Si nanowires connecting the source and drain metal pads. At the *x* axis, '0' means no nanowire connecting. '1' and more means the devices have single-nanowire and multi-nanowire channels, respectively.

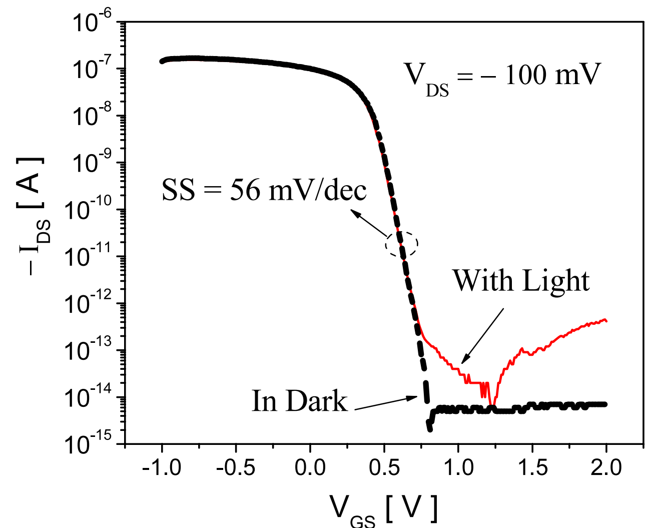

Figure 3. The log-scale transfer characteristics (I_{DS}–V_{GS}) measured in dark and under strong visible light ($V_B = 0$ V).

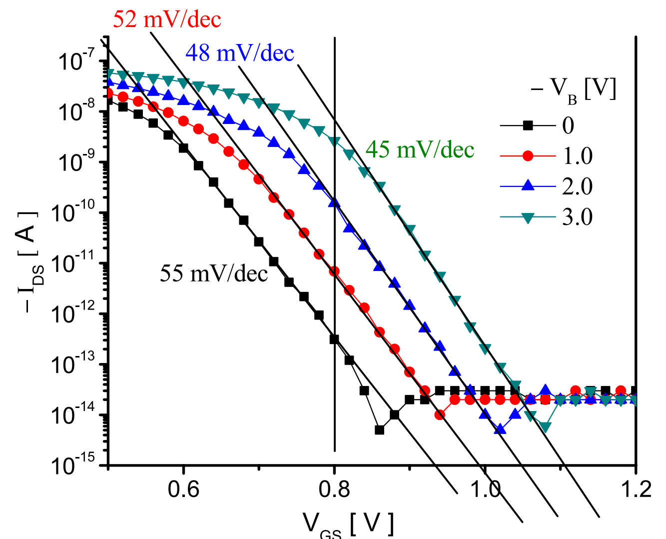

Figure 4. I_{DS}–V_{GS} curves with V_B varying from 0 to −3.0 V at the subthreshold region. The values of subthreshold swing have been directly extracted and shown in the figure.

respectively. In this work, about 90% of the pre-defined locations successfully form the expected SiNW devices with one or more nanowires connected over a whole 4 inch wafer. Statistically, as shown in figure 2, about 60% of the devices have a single-nanowire conduction channel. We believe that the success rate can be further improved and the number of nanowires per device can be modulated by careful optimization of the Au catalyst, device structure and nanowire length. For example, precise control of nanowire density [15] and growth direction [16] to assist nanowire integration has been reported by other scientists.

The SiNW FETs fabricated by using the self-aligning process have a clean gate/channel interface which results in sharp subthreshold slope. As shown in figure 3, the SiNW FET transfer characteristics (I_{DS} versus V_{GS}) are measured in dark and under strong visible light. The light is absorbed by the SiNW channel which generated electron–hole pairs, resulting in higher electron conduction at positive gate voltage compared to the measurement in dark. However the absorbed light does not increase the trapping/detrapping of the interface states with V_{GS} at the subthreshold region. Both measurement (in dark and under light) exhibit similarly sharp SSs (≈56 mV/dec), indicating that the SiNW interface state density is negligible.

3. Results and discussion

Figure 4 shows the transfer characteristics (I_{DS} versus V_{GS}) of the SiNW FET with $V_{DS} = -100$ mV and bottom gate voltage (V_B) varying from 0 to −3.0 V. I_{DS} stays low at about 1–10 fA as V_{GS} extends beyond 1.0 V, indicating that ambipolar behavior is not observed in these Schottky contact devices. The on/off current ratio (i.e. I_{ON}/I_{OFF}) is larger than 10^7 in a 1 V operation voltage window ($V_{GS} = -0.9$–0.1 V, see figure 3). The hole mobility is calculated as 178 cm^2 V^{-1} s^{-1} for the typical SiNW FET (single-nanowire channel with 20 nm in diameter and 5 μm in length), which is less than that of planar MOSFETs. Such mobility degradation is mainly due to the surface recombination (not the remaining Au in the as-grown SiNW) [17]. The mobility is not significantly different for the SiNW FETs with single and multiple nanowires. The subthreshold swing defined by $SS = -[d(\log_{10} I_{DS})/dV_{GS}]^{-1}$ was extracted from the log-scale I_{DS}–V_{GS} curves with V_{GS} at the subthreshold region, which is shown in the figure. The I_{DS}–V_{GS} curves become steeper with decreasing V_B, leading to SSs as low as 45 mV/dec at $V_B = -3.0$ V.

This SS value is well below the thermionic diffusion limit (60 mV/dec) for conventional planar MOSFETs which are governed by carrier thermionic diffusion at the subthreshold region. The thermionic diffusion current is proportional to the minority carrier density gradient along the channel. Unlike

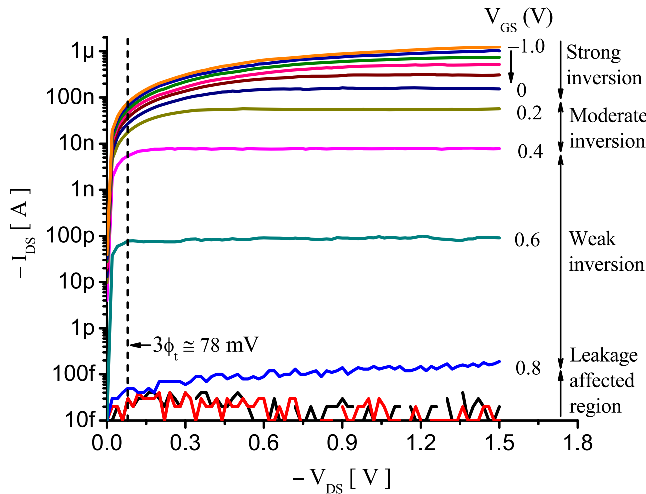

Figure 5. The log-scale output characteristics (I_{DS}–V_{DS}) of a typical SiNW FET fabricated in this work with a single-nanowire conduction channel (see figure 1(d)).

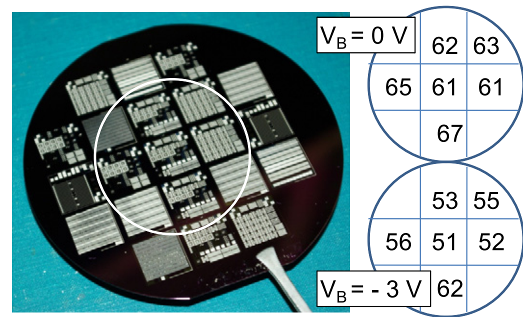

Figure 6. Image of a 4 inch wafer on which a batch of NWFETs have been fabricated. About 80 NWFETs, which are located in one of the five dies inside the white circle, have been measured and summarized to obtain the distribution of SS over the wafer. The averages of the NWFET SS (unit: mV/dec) for each die at (i) $V_B = 0$ and (ii) $V_B = -3$ V are shown in the top-right and bottom-right circles, respectively.

the source/drain (S/D) pn junction diode of conventional MOSFETs, the NWFETs in this work have an additional current 'valve' for the carrier transportation: the Schottky barrier between the S/D and channel. The electric field between the gate and the S/D contacts modulates the Schottky barrier height and width. This gate–channel–source coupling is enhanced by the three-dimensional electrostatics of nanowires and the abrupt S/D Schottky junctions [18]. When a negative V_{GS} is applied, the channel valence band bends upward. Thus, the width of the barrier between the source and the NW channel decreases and the tunneling current increases exponentially. If the Schottky barrier is thin enough, the tunneling component will dominate the channel current. The tunneling rate is not limited by the thermionic emission; thus the SS can be less than 60 mV/dec. Such Schottky barrier tunneling will be substantially enhanced with the effective hole carrier density which increases with more negative V_B.

The output characteristics (I_{DS} versus V_{DS}) of a typical NWFET with a single-nanowire conduction channel (see figure 1(d)) are plotted in figure 5. The bottom gate (V_B) and the source (V_S) are grounded for this measurement. The output characteristics clearly show the strong, moderate and weak inversion regions. These data are similar to those of a conventional long-channel planar MOSFET: (i) in weak inversion, I_{DS} approximately follows the exponential rule (I_{DS} increases exponentially with V_{GS}) and is saturated at $3\Phi_t$ (Φ_t is the thermal potential, $\approx$26 mV at room temperature); and (ii) in strong inversion, I_{DS} approximately follows the square law ($I_{DS} \sim (V_{GS} - V_{TH})^2$) and is saturated at $V_{DS} = V_{GS} - V_{TH}$, where V_{TH} is the threshold voltage of the NWFET. This current saturation is more ideal than that of interband-tunneling FETs which do not exhibit the saturated I_{DS}–V_{DS} characteristics. These output characteristics also show that I_{DS} increases with decreasing V_{GS}; thus this device is a p-channel FET. In addition, the I_{DS}–V_{DS} curves increase sharply in the linear region, indicating negligible series resistance in the source and drain. Such sharp turn-on, well-saturated I_{DS}–V_{DS} characteristics have seldom been reported in the publications on nanowire FETs.

However, if a large number of interface traps are introduced by the fabrication process, these traps will determine the SS, and such steep SSs cannot be achieved. The self-alignment process developed in this work successfully provides a clean dielectric/channel interface for the NWFETs so that S/D injection dominate the SS and excellent device properties are achieved. The small, fully depleted nanowire body (<20 nm in diameter) augments the electrostatic properties of the devices. Since the self-alignment process is effective on the full-wafer scale, the quality of nanowire devices is reproducible and homogeneous across the entire wafer. Figure 6 (left) shows a 4 inch wafer on which a batch of NWFETs has been fabricated. About 80 NWFETs, which are located in one of the five dies inside the white circle, have been measured and analyzed to obtain the distribution of SS over the wafer. The averages of the NWFET SS for each die at (i) $V_B = 0$ and (ii) $V_B = -3$ V are shown in the top-right and bottom-right circles of the figure, respectively. These statistical results show that the values of SS of the NWFETs fabricated in different locations of the wafer are consistent. The overall averages of SS are 63 mV/dec at $V_B = 0$ and 53 mV/dec at $V_B = -3.0$ V. In addition, the performance of NWFETs fabricated in different runs is reproducible. These data illustrate that the large-scale, self-aligning integration process is reproducible and compatible with CMOS technology.

4. Summary

In conclusion, we have developed self-alignment processes to fabricate high-performance SiNW FETs with large I_{ON}/I_{OFF} ratios ($>10^7$), well-saturated I_{DS}–V_{DS} and sharp subthreshold swings as low as 45 mV/dec. The excellent device characteristics stem from the clean fabrication and special Schottky junction source/drain structure which is coupled with the gate. Statistical results show that the performance of nanowire devices is consistent over a whole wafer and

repeatable from run to run, demonstrating integration at the wafer scale. This work also supports that self-assembled nanowire-based devices can have better electrical performance than conventional planar MOSFET and thus can rightfully be viewed as building blocks for future electronics.

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