Advanced Capacitance Metrology for Nanoelectronic Device Characterization

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Abstract. We designed and fabricated a test chip (consisting of an array of metal-oxide-semiconductor (MOS) capacitors and metal-insulator-metal (MIM) capacitors ranging from 0.3 fF to 1.2 pF) for use in evaluating the performance of new measurement approaches for small capacitances. The complete array of capacitances was measured to obtain a "fingerprint" of capacitance values. After correcting these data for pad and other stray capacitances, such data can be used to evaluate the relative accuracy and sensitivity of a capacitance measurement instrument or circuit. This test chip was used to assess the capabilities of two different capacitance measurement approaches: an LCR meter, and a capacitance bridge. A silicon-nanowire based capacitance test structure was fabricated and characterized by using the optimized capacitance measurement methods developed with the MOS/MIM test chip.

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INTRODUCTION

The component capacitance of individual nm-scale nanoelectronic devices for future generations of integrated circuitry defies easy measurement. Emerging nanoelectronic devices such as those fabricated from semiconductor nanowires (NWs) and quantum dots, as well as FinFET type devices (field effect transistors with gates wrapped around a thin Si fin) have capacitances that are much smaller than can be accurately and easily measured by conventional LCR (Inductance (L), Capacitance (C), and Resistance (R)) meters. The intrinsic device capacitances of these deep-submicron devices (such as the gate-drain, source-drain, or gate-channel capacitances) determine the operational characteristics of the structures, and an accurate knowledge of their values is required for accurate device modeling and predictive computer-aided design. The quantum capacitance is a fundamental device attribute associated with the low density of states in low-dimensionality structures such as quantum wires (e.g., carbon nanotubes (CNTs) and semiconductor nanowires). [1,2] This quantum capacitance in nanowire FETs (field effect transistors) can dominate over the gate capacitance, preventing effective conduction control via the gate voltage. Thus, the quantum-capacitance in nanoelectronic devices is currently an area of great fundamental scientific and technical interest. Straightforward methods to experimentally measure the quantum capacitance in nanowire structures can have an important immediate impact.

We are developing methods to combine probe stations with the sophisticated capacitance measurement equipment and expertise associated with maintaining the capacitance standard for the farad to enable measurements of critical capacitances in nanoelectronic devices at the aF-level. As a first step, we have designed and fabricated a capacitance test chip for use in evaluating the performance of new measurement approaches for small capacitances. This test chip contains arrays of metal-oxide-semiconductor (MOS) capacitors and metal-insulator-metal (MIM) capacitors ranging from 0.3 fF to 1.2 pF. By careful analysis of the measurements of the complete array of capacitors, the experimental stray capacitances (such as those arising from contact pads) can be determined and accounted for in measurements of nanoelectronic devices and components. The test chip was used to assess the on-chip measurement capabilities of two

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different capacitance measurement approaches (an LCR meter, and a capacitance bridge). We then applied the optimized capacitance measurement methods to characterize a silicon-nanowire based capacitance test structure.

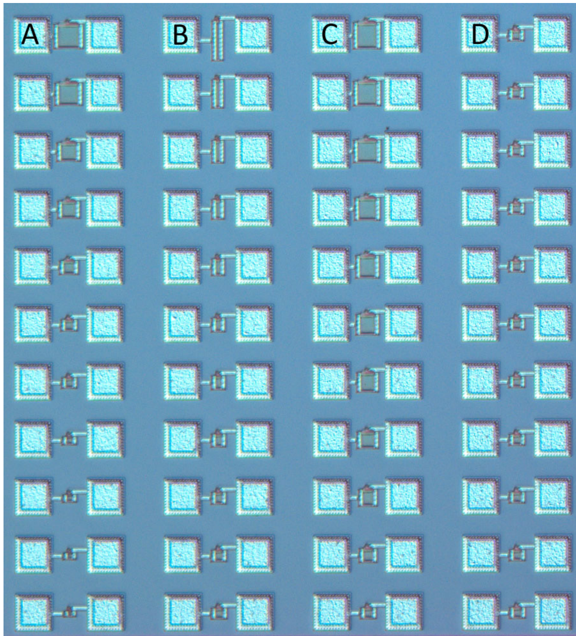

FIGURE 1. Optical micrograph of selected MOS capacitance test structure series. [A] maximum range series 11, 11.3 fF to 1133 fF (designed capacitance); [B] series 12, variation of perimeter to area ratio, 102 fF; [C] series 13, 102 fF steps from 102 fF to 1122 fF; [D] series 14, 102 fF uniformity test.

TEST CHIP LAYOUT AND FABRICATION

The complementary metal-oxide-semiconductor (CMOS) test chips were fabricated in a commercial foundry running a 1.6 µm design rules process. The relatively thick gate dielectrics and inter-metal dielectrics associated with this process (nominally 31 nm and 908 nm, respectively) ensured low dc current leakage in the test capacitors and also reduced the capacitance per unit area of the capacitors relative to more aggressive technologies, enabling the fabrication of robust, small value capacitors. MOS capacitors were chosen for their voltage dependence, and MIM capacitors were chosen for their smaller total capacitance values. Both types of devices were designed with probe pads to each side of the capacitor. A highly doped guard band surrounds the MOS devices to prevent depletion edge spreading.

Sixteen series of MOS devices were designed and fabricated to test various capacitance measurement capabilities such as uniformity and repeatability at a target capacitance, perimeter-to-area ratio variation at a target capacitance, and variation around a target capacitance for a given square geometry. (A full list is given in Table 1.) Each series consisted of 11 individual devices. Figure 1 shows four of these MOS series. The ability to resolve a given capacitance value was tested by producing a range of devices which varied systematically around a target oxide capacitance, C_{ox}, according to the following sequence: 80 %, 90 %, 95 %, 98 %, 99 %, 100 %, 101 %, 102 %, 105 %, 110 %, and 120 % of C_{ox}. Similar MIM devices were fabricated by using the inter-metal dielectric, resulting in correspondingly smaller capacitances. This design yields a total of 176 devices. Two full sets (groups A and B) of MOS and MIM test structures were laid out on each chip.

TABLE 1. Designed oxide capacitance of MOS series.

Series	Min (fF)	Mid (fF)	Max (fF)	Notes
1	11.3	25.5	39.7	Minimum size series
2	77.9	99.2	119.7	Variation around 100 fF
3	159.4	201.9	250.8	Variation around 200 fF
4	405.6	497.3	595.7	Variation around 500 fF
5	794.8	995.9	1190.7	Variation around 1000 fF
6	987.4	997.3	1011.5	Small variation around 1000 fF
7	63.8	102.0	148.8	Variation around 100 fF, squares
8	148.8	204.7	269.2	Variation around 200 fF, squares
9	425.0	516.4	616.3	Variation around 500 fF, squares
10	892.5	1022.8	1161.7	Variation around 1000 fF, squares
11	11.3	119.7	1133.3	Maximum range series
12		101.9		Variation in perimeter-to-area ratio
13	102	612	1122	Equal 102 fF steps
14	102	102	102	Repeatability at 102 fF
15	516.4	516.4	516.4	Repeatability at 516 fF
16	1022.8	1022.8	1022.8	Repeatability at 1022 fF

MEASUREMENT RESULTS

The MOS devices were first measured with a commercial inductance-capacitance-resistance (LCR) meter. Capacitance-voltage (CV) curves were

measured over a range of frequencies and oscillator strengths (V_{osc}) to determine optimum measurement conditions. For this test chip, CV curves measured at 100 kHz, V_{osc} = 50 mV, and dc bias swept from -3 V to +3 V in 50 mV steps were found to have minimal series resistance effects and to produce stable capacitance values from relatively high-speed measurements. An automatic probe station was used to efficiently acquire complete data sets.

Excellent agreement between the designed and experimentally measured MOS oxide capacitances was seen. The extracted C_{ox} was close to the value reported from the foundry process monitor. Figure 2 shows the measured and modeled C_{ox} values for one complete set of all 16 capacitance series. Examples of the difference between the simulated and measured capacitance are shown at the top of Figure 3.

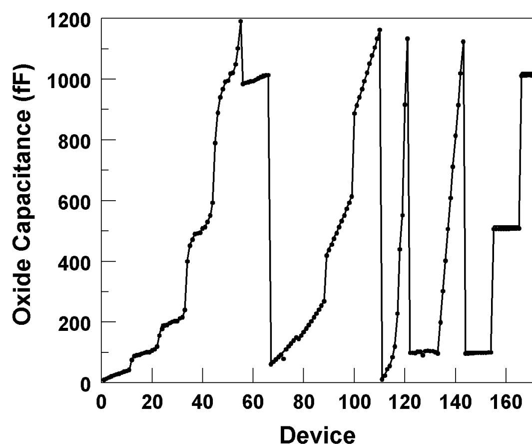

FIGURE 2. Calculated oxide capacitance (solid line) and measured maximum capacitance (points) vs. device index.

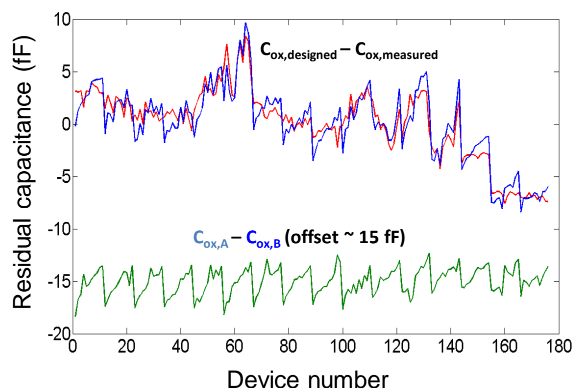

FIGURE 3. Residual capacitances. Top, difference between the measured ($C_{ox,measured}$) and designed ($C_{ox,design}$) MOS capacitance for two full sets of test structures on the same chip (labeled set A – blue line and set B – red line). Bottom, difference between nominally identical devices in set A and set B.

When the voltage is biased in accumulation, the total capacitance of each MOS device is the parallel sum of the pad capacitance, C_{pad}, the perimeter fringe capacitance, C_{fringe}, and the oxide capacitance, C_{ox}. The test structures are designed so that the pad capacitance is MOS geometry independent, the fringe capacitance is proportional to the device perimeter, P, and the oxide capacitance is proportional to the device area, A. The total capacitance, C_{total}, can be expressed as

$$C_{total} = C_{pad} + P \times C_{fringe} + A \times C_{ox} . \quad (1)$$

To simplify analysis, we introduce a parameter S, where the area of the device is $A = S^2$. The perimeter of the device is kS, where and k is defined as the ratio of the perimeter to $A^{½}$. The k-values vary from 4 (for a square device) to 12.3 (for a high aspect ratio rectangle) for our devices, with an average of 4.14. The capacitance per unit area can then be rewritten as:

$$\frac{C_{total}}{A} = \frac{C_{pad}}{S^2} + \frac{kC_{fringe}}{S} + C_{ox} . \quad (2)$$

A plot of 1/S versus the measured capacitance per unit area yields a 2nd order polynomial curve with a y-intercept of C_{ox}, a slope of C_{fringe}, and a curvature of C_{pad}. For this chip we extract C_{ox} = 1.10 fF/µm^2 (compared to 1.12 fF/µm^2 reported by the chip foundry process monitor), C_{fringe} = 11 aF/µm (compared to 34 aF/µm for the monitor), and a C_{pad} of 131.5 fF (compared to our simulated value of 133 fF). This excellent agreement confirms the effectiveness of our test chip as a reliable test vehicle for evaluating the performance of capacitance measurement approaches applied to on-chip test structures.

Chip-to-chip variation was less than ±10 % for C_{ox} and C_{pad}. We have observed a systematic variation between the group A and B MOS devices across all the test chips received. The residual capacitance (the difference in capacitances between identically designed devices in group A and in group B) is shown at the bottom of Figure 3. For each of the 16 series of devices, a similar residual capacitance is extracted that is correlated with the position of the device on the chip. The observed variation may be due to a systematic process variation; however, (as we will mention below) we attribute this trend to a systematic stray capacitance associated with the position of the probe with respect to the physical edge of the chip under test.

MIM capacitance test structure series were also designed and fabricated. Because the inter-metal dielectric is significantly thicker than the gate oxide in the MOS structures, the MIM devices have correspondingly smaller capacitances. Their design capacitances range from 240 fF down to 0.38 fF. These devices were measured with both the

commercial LCR meter and a commercial ultra-precision capacitance bridge. In order to optimize the measurement performance of both instruments, these devices were measured at 1 kHz, V_{osc} = 1 V. A substantially longer averaging time (5 min) was required to resolve the MIM capacitance compared to the MOS CV responses. Because there is no change in the capacitance as a function of voltage in the MIM structures for moderate voltages, a relatively larger oscillator voltage is allowed. Good agreement is obtained when the results of the two measurement approaches are compared to the calculated values for the 77 devices in the MIM series as shown in Figure 4.

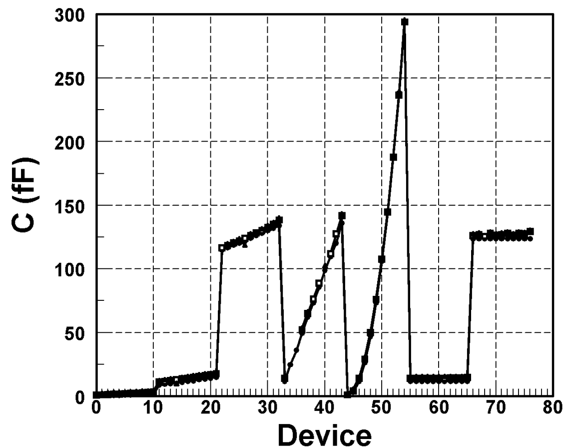

FIGURE 4. MIM Calculated and measured capacitances: Theoretical data -- including stray capacitance (solid circles and line) and measured capacitance for the two instruments (solid squares and open circles).

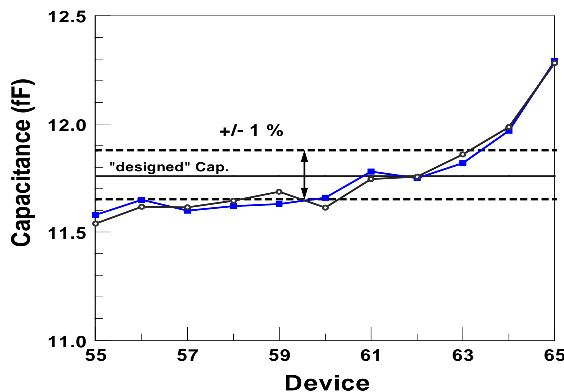

FIGURE 5. The adjusted capacitance as extracted from capacitance bridge measurements and LCR meter measurements of 11 nominally 11.75 fF MIM capacitors.

By plotting the measured capacitances versus the design capacitance, a 15 fF stray probe and cable capacitance was obtained. In addition, we could account for a difference in the thickness of the actual inter-metal dielectric compared to the value initially used in simulations. For the range of devices measured, the capacitances measured by the two instruments differed by ≈1.2 fF. After taking this constant offset into account, the two instruments agreed to within an average of 30 aF. The excellent agreement for relative changes in capacitance is shown in Figure 5 for 11 nominally identical devices with a ≈11.75 fF capacitance. As illustrated in Figure 5 (and in the residuals in Figure 3-top), an upward trend is observed within a given set of devices. This feature is due to the stray capacitance that arises from the coupling between the probe tip and the chip-substrate. At the boundaries of the chip, this capacitance varies systematically with the position of the probe with respect to the edge of the chip. This upward trend should not be measured if full wafers were probed (instead of individual chips).

SILICON NANOWIRE CAPACITANCE

The capacitance associated with a single semiconductor nanowire structure is experimentally difficult to determine accurately. [3] For example, the capacitance per unit length of a single nanowire device with a geometry similar to that in our SiNW test structures described below (a 20 nm diameter SiNW wrapped by a high-κ gate stack with a Ω-shaped metal top-gate) is ≈180 aF/μm (as simulated by using commercial modeling software). More aggressively scaled nanowire devices have been modeled with CV curves with a maximum capacitance of ≈ 4 aF (10^{-18} F) and a minimum capacitance of ≈1 aF. [4] In typical nanowire structures formed on an oxidized Si-substrate, the stray capacitance between the contact pads and the substrate is significantly larger than that of the nanowires themselves. In addition, this stray metal-oxide-semiconductor capacitance varies with applied voltage, making it challenging to account for it. As a first step towards measuring the capacitances of individual semiconductor NW devices, we designed and fabricated a capacitance test structure consisting of many SiNWs in parallel.

These test structures (schematically shown in Figure 6) were fabricated by using a "self-aligning" process [5,6] that has been successfully used to fabricate a variety of devices such as steep-subthreshold, Schottky tunneling FETs, [7] and charge trapping memory cells. [5, 8]. The essential steps are as follows. First a layer of thermal SiO_2 was grown by dry oxidation on a silicon wafer. SiNWs (~ 20 nm diameter) were then grown from Au catalysts in pre-defined locations by the vapor-liquid-solid process. The growth was immediately followed by dry thermal oxidation to form a thin SiO_2 interface layer (~3.5 nm) around the SiNWs. By optimizing the catalyst position and thickness, a relatively dense layer of SiNWs is grown to form the semiconducting electrode of a MOS

capacitor. Al Schottky contacts to the SiNWs were patterned by lithography after the SiO_2 was removed in the contact regions. HfO_2 was deposited by ALD (atomic layer deposition) as a high-κ layer to complete the gate dielectric. Finally, an Al top gate electrode was defined and deposited.

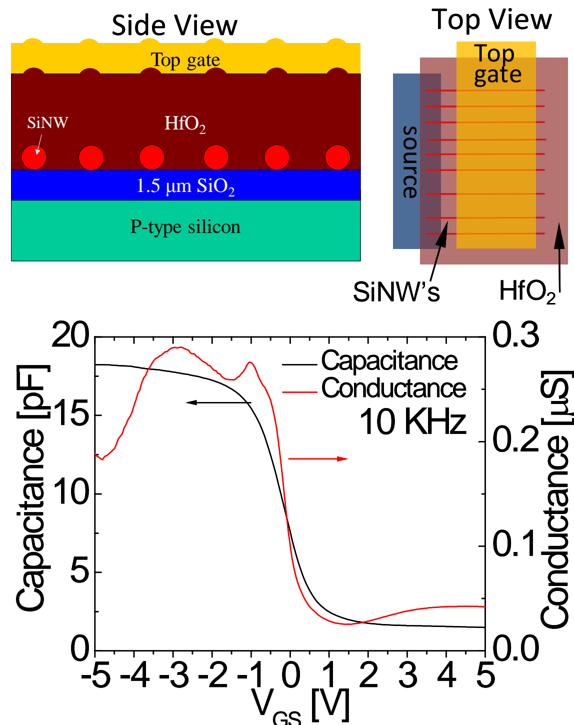

FIGURE 6. SiNW capacitance test structure. Top, schematic diagrams (not to scale) of the device structure. Note that the SiNWs in the actual structures have a random spacing. Bottom, capacitance-voltage and conductance-voltage measurements taken at room temperature and 10 KHz.

Typical CV and conductance-voltage data for a multi-SiNW test structure are shown in Figure 6. These data were obtained by using the methods optimized in characterizing the MOS/MIM test structures. Such data demonstrate that SiNW test structures can be fabricated and the capacitance of these devices effectively measured. Even though the exact number of SiNWs is unknown in these structures, the CV data are effective for characterizing critical device properties such as nanowire/dielectric interface traps and active nanowire doping levels. We are actively designing and fabricating new test structures to enable CV measurements on single SiNW structures.

SUMMARY

In summary, we have used a capacitance test chip to assess the ability of two commercially available capacitance measurement systems to measure the on-chip capacitance of MIM and MOS capacitors with small capacitance values within a probe station. With this equipment, we demonstrated that we can measure relative changes in capacitance on the order of 10's of aF. This resolution is sufficient to measure many nanoelectronic devices and materials; however, further improvements are needed to fully characterize deep-submicron CMOS devices and other emerging nanoelectronic structures.

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