Prototype Thermal Design for a 256 Pixel Transition Edge Sensor Bolometer Array with Additional on-chip Cooling[1]

Galen C. O'Neil, Peter Lowell and Joel Ullom

National Institute of Standards and Technology, 325 Broadway, Boulder, CO 80303, USA

Abstract. Normal-metal/insulator/superconductor (NIS) tunnel junctions can be integrated with transition edge sensor (TES) bolometers to provide additional cooling to the sensor. For example, a TES array cooled to 300 mK by a He^3 refrigerator could be enhanced with additional on-chip NIS cooling that decreases the effective bath temperature of each TES to 100 mK. The noise of the array with on-chip cooling would be $\sim$40% lower than a similar array without on-chip cooling. Additionally, the lower bath temperature allows a more physically robust design with the same saturation power per pixel. However, on-chip NIS cooling does not come for free. While the NIS coolers reduce the bath temperature seen by each pixel, they also dissipate about 100 times as much power as the pixel alone and increase the fabrication complexity. We describe a potential thermal design of a 256 pixel TES bolometer array with on-chip cooling. We show that such an array is feasible despite the increase in thermal power dissipation.

Keywords: Millimeter receiver, TES bolometer, Green Bank Telescope, Microrefrigerator, Normal-insulator-superconductor tunnel junction
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INTRODUCTION

The Multiplexed Squid TES Array at Ninety GHz (MUSTANG) is an instrument currently installed on the Green Bank Telescope (GBT) in West Virginia[1] which is a 64 pixel TES Bolometer array with a bath temperature of 300 mK provided by a He^3 refrigerator. MUSTANG is an ideal candidate for an upgrade to NIS-cooled TES bolometers because it would benefit from a lower effective bath temperature and the He^3 refrigerator installed on the telescope is not able to be replaced with something with a lower bath temperature in a cost effective manner. Integrated NIS coolers can lower the Noise Equivalent Power (NEP) by providing a lower effective bath temperature by replacing the array itself rather than the He^3 refrigerator. The current array is not operating at theoretical limits, however we will compare improvements assuming that that theoretical limits are achieved in both a next generation array without NIS coolers and a future array with NIS coolers. Figure 1 shows a prototype of a 100 pixel array that may soon replace the 64 pixel array and should perform closer to theoretical limits. While the addition of NIS cooling decreases the effective bath temperature seen by the bolometers, it also increases the total power dissipation of the array. This increase will translate directly into larger thermal gradients in the Si substrate of the array. We present a thermal model to predict temperature gradients across the array and a thermal design that will minimize those temperature gradients.

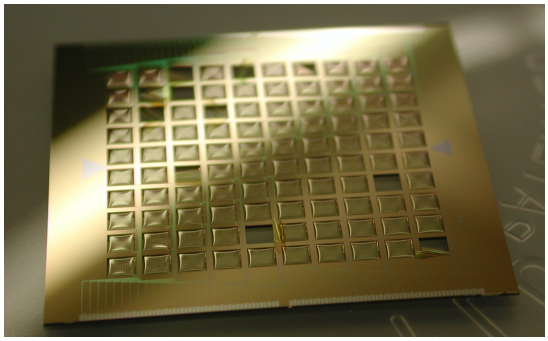

FIGURE 1. Prototype of a 100 pixel MUSTANG array. This array is very similar to the array that we are modeling. The substrate is a 275 μm thick Si wafer with 500 nm thick SiN membranes. Each pixel is 2 mm by 2 mm and the pixel to pixel pitch is 2.5 mm. The pixels have MoCu bilayer TES thermometers with Nb wiring and a PdAu mesh to absorb 90 GHz radiation. This prototype does not include NIS coolers, heatsinking bond pads or underside Au.

DESIGN CONSIDERATIONS

Pixels in the MUSTANG instrument require a saturation power, P_{sat}, of 8-9 pW. To account for margins in the fabrication process, we will assume a saturation power of 12 pW for our calculations. The saturation power is give by,

$$P_{sat} = K(T_c^n - T_{Bath}^n), \quad (1)$$

where K is the thermal conductivity of the SiN legs suspending the TES bolometer, n is an exponent we have measured to be $\sim$3, T_{Bath} is the effective bath temperature

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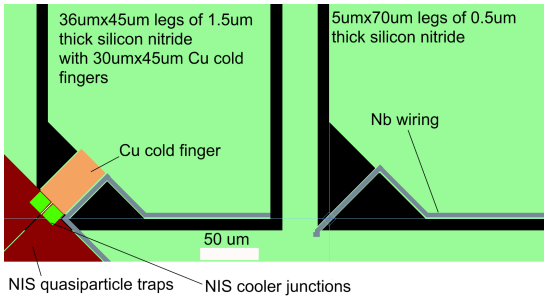

FIGURE 2. The right side shows the current leg design where the bath temperature is provided by the Si substrate and the thermal isolation is provided by long skinny legs of SiN. The left side shows a potential leg design incorporating NIS coolers. The Cu cold fingers provide the effective bath temperature and the thermal isolation is provided by the SiN. The NIS coolers consist of two 12 μm by 12 μm tunnel junctions per leg and quasiparticle traps with dimensions on order 200 μm.

and T_c is the membrane temperature which is equal to the TES transition temperature during operation. The NEP can be calculated as,

$$NEP = \sqrt{2k_b(G(T_c)T_c^2 + G(T_b)T_b^2)}, \qquad (2)$$

where $G(T) = \frac{dP_{sat}}{dT_c}|_T$[2]. Combining Equations 1 and 2, we can calculate that for the current bath temperature of 300 mK, the optimal NEP is $2.66{\cdot}10^{-17}$ $\frac{\mathrm{W}}{\sqrt{\mathrm{Hz}}}$ with K=94.7 pW/K^n and T_c of 536 mK. With NIS coolers that reduce the effective bath temperature to 100 mK the NEP would be improved to $1.54{\cdot}10^{-17}$ $\frac{\mathrm{W}}{\sqrt{\mathrm{Hz}}}$ with K=2560 pW/K^n and T_c of 179 mK. The NEP can be improved by $\sim$40% by integrating NIS coolers into the MUSTANG array. Another feature of NIS coolers is that the lower temperatures make thermal isolation easier. We see that K, which is roughly inversely proportional in the number of squares of SiN used for thermal isolation and roughly proportional to the thickness of the SiN, can be much larger in the NIS-cooled pixels. Larger K translates into thicker and shorter SiN legs, which should improve the physical strength of the pixel and increase yield.

NIS DESIGN CONSIDERATIONS

NIS coolers remove power directly from the electron system in the normal metal electrode. By suspending the normal-metal on a membrane to isolate the phonon system, both the electrons and phonons can be cooled[3, 4]. The extended normal metal can be used to provide an effective bath temperature, $T_{NIS-Bath}$, to a bolometer. Figure 2 shows how the legs of the current MUSTANG bolometers would be modified to work with NIS coolers.

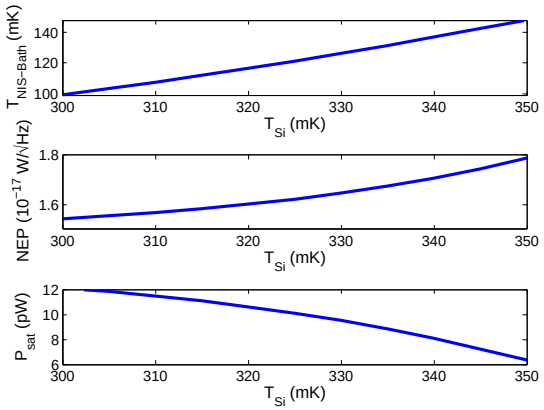

FIGURE 3. The effects of temperature variation across the array. Modeling of 2 series 12μm by 12μm NIS junctions with resistance area product of 1000 $\Omega\mu$m^2 and quasiparticle return parameter of β=.005 shows how the effective bath temperature, $T_{NIS-Bath}$, for the bolometers varies with the silicon substrate temperature. The NIS thermal model used here is described by Clark et al. [5]. Using calculated values of $T_{NIS-Bath}$, we also show calculated values of NEP and saturation power vs silicon substrate temperature using equations 1 and 2.

The Cu cold fingers provide the effective thermal bath and the thermal resistance comes from the SiN membrane, rather than the legs.

In the non-NIS-cooled case, the total power deposited in the Si substrate per pixel is equal to the saturation power. In the NIS-cooled case, the saturation power is a power load on the NIS thermal bath and the total power deposited in the Si substrate is equal to the saturation power plus the joule power of the NIS coolers. The total power deposited by the NIS coolers is given by $M_{NIS}P_{sat}$ where M_{NIS} is called the NIS power multiplier. This multiplier will vary along with $T_{NIS-Bath}$ depending on the ratio of the area of the NIS cooler junctions to P_{sat}. Typical values for M_{NIS} range from 40-500 and we will design around a value of 100.

The large increase in power deposited into the Si substrate with NIS coolers has the potential to lead to large temperature gradients across the bolometer array. Temperature gradients in the Si substrate will affect $T_{NIS-Bath}$ as well as P_{sat} and the NEP of the detectors. These effects are shown in Figure 3. Another danger is that it will become harder to bias many detectors at the same time.

THERMAL MODEL

We want to create a thermal model for an NIS-cooled TES bolometer array with realistic parameters and have chosen to simulate a potential future version of MUSTANG with 256 pixels. Each pixel will have a saturation power of 12 pW so each pixel will deposit 1.2 nW in-

TABLE 1. Parameters and values used in the thermal model.

Variable	Value	Description
κ_{Si}	0.0157 W/(K m)	Thermal conductivity of Si, value evaluated at 300 mK
κ_U	6.65 W/(K m)	Thermal conductivity of underside Au, value evaluated at 300 mK
ρ_{Au}	0.11 $\mu\Omega cm$	4 K resistivity of Au assuming a RRR*of 20
T_b	300 mK	Copper sample box temperature
T_{HS}	300.8 mK	Electron temperature of Cu Heatsink Pads
M_{NIS}	100	NIS power multiplier
P_{sat}	12 pW	Saturation power of a single pixel
Σ_U	1 nW/(m^3K^5)	Electron-Phonon coupling of underside Au
Σ_{HS}	1 nW/(m^3K^5)	Electron-Phonon coupling of Cu heatsink Pads[6]
t_U	5 μm	Thickness of underside Au†
t_{HS}	0.5 μm	Thickness of Cu heatsink pads**
t_{Si}	275 μm	Thickness of Si substrate
l_{array}	40 mm	Length (and width) of the array on the chip
s_{HS}	0.1875	Fraction of the length of the array taken up by optional center heatsinking pad

* RRR is the ratio of room temperature resistivity to 4 K resistivity
† Chosen to be easy with e-beam deposition, could increase to 50 μm+ with electroplating
** Chosen to be deposited in the same step as the normal metal banks on the TES, could increase to 5 μm with a separate deposition

FIGURE 4. Schematic of the thermal model.

cluding the NIS-cooler contribution, with a total power of 307 nW deposited on the chip. We will add a layer of Au to the underside of the array to increase thermal conductivity and add Cu heatsinking pads to the edges of the chip which are attached to the copper sample box with Au wire bonds. There is an optional heatsinking pad in the middle of the chip and a hole in the chip which would allow wire bonds directly to the copper sample box.

A schematic of the thermal model is shown in Figure 4. The phonons in the Si substrate couple directly to both the electrons in the underside Au and the Cu heatsinking pads. All the power from the NIS junctions is deposited in the red region in the Si substrate. The heatsinking pads couple to the copper sample box through the Wiedemann-Franz thermal conductivity of the Au wire bonds. We treat T_{HS} as constant to simplify the model. We assume no direct coupling between the underside Au and the copper sample box. Table 1 provides a description of the variables used and many of their values.

We solve for the position dependence of two temperatures, T_{Si} and T_U, in one dimension. The one dimensional model should have higher temperature gradients than a two dimensional model by approximately $\sqrt{2}$. Both temperatures are described by diffusion equations

$$0 = \kappa_{Si} S_{Si}(x) \frac{d^2}{dx^2} T_{Si}(x) + P_{Array}(x) + P_{HS}(x) + P_U(x), \tag{3}$$

$$0 = \kappa_U S_{Si}(x) \frac{d^2}{dx^2} T_U - P_U(x) \frac{t_{Si}}{t_U}. \tag{4}$$

Where most of the variables are described in Table 1. $S_{Si}(x)$ is a geometry function that is equal to one for x outside the array and equal to 1/5 for x inside the array to account for the removed material behind the membranes. All of the power terms are scaled to have the proper power per unit volume in the Si substrate, therefore the P_U term in Equation 4 requires additional scaling.

The phonon thermal conductivity of Si, κ_{Si} is calculated by $C_{Si} c_{Si} l_{Si}/3$ where the speed of sound, c_{Si}, is 7800 m/s and the heat capacity, C_{Si}, is $0.575 \cdot T_{Si}^3$ J/(K m^3)[7]. The mean free path, l_{Si}, should be limited by the thickness of the Si substrate, which is 275 μm. We multiply that width by $\sqrt{2}$ to calculate l_{Si}. The thermal conductivity of the underside Au, κ_U, is calculated from the Wiedemann-Franz law along with the properties of Au shown in Table 1. Both κ_{Si} and κ_U are based on the local temperature at each point in the array.

The power terms are given by

$$P_{Array}(x) = S_{array}(x) \frac{P_{total}}{t_{Si} l_{array}^2}, \tag{5}$$

$$P_{HS}(x) = \frac{t_{HS}}{t_{Si}} \Sigma_{HS} (T_{Si}(x)^5 - T_{HS}^5) S_{HS}(x), \tag{6}$$

$$P_U(x) = \frac{t_U}{t_{Si}} \Sigma_U (T_{Si}(x)^5 - T_U(x)^5) S_{Si}(x). \qquad (7)$$

Where $S_{array}(x)$ is one for x inside the array and zero for x outside the array. $S_{HS}(x)$ is one for x inside of the heatsink pads and zero for x outside of the heatsink pads. In the case with the optional center heatsinking pad, $S_{HS}(x)$ is set to a value, s_{HS}, for x inside the central heatsink pad. This value is less than one to represent the fraction of the length of the array taken up by the central heat sink. We have allocated 3 pixels worth of area, 2.5 mm by 7.5mm, to the central heatsink pad and one pixel worth of area to a hole to allow bonding directly to the copper sample box. We calculate the resistance of each Au wire bond to be 1.1 mΩ for a length of 500 μm and a diameter of 25 μm. That translates into a Weidemann-Franz thermal conductivity of 6.6 μW/K per wire bond at 300 mK. If we assume that one half the total dissipate power leaves through 30 wire bonds, we have a temperature drop of 0.8 mK across those wire bonds. As a result of this calculation we set T_{HS} to 300.8 mK.

We solve the coupled diffusion equations in MATLAB with the function *bvp4c*. This function will solve sets of linear differential equations, so we linearize the diffusion equations. It is important to linearize the equations such that the internal boundary conditions maintain constant power flux, $\kappa \frac{dT}{dx}$, rather than constant derivative of temperature, $\frac{dT}{dx}$. To achieve this we define the elements of the input vector y to be $[T_{Si}, \kappa_{Si} \frac{dT_{Si}}{dx}, T_U, \kappa_U \frac{dT_U}{dx}]$. The elements of the derivative y' are defined as $[y(2)/\kappa_{Si}, \kappa_{Si} \frac{d^2 T_{Si}}{dx^2}, y(4)/\kappa_U, \kappa_U \frac{d^2 T_U}{dx^2}]$. Where $y(2)$ and $y(4)$ are the 2nd and 4th elements of y.

RESULTS AND DISCUSSION

Results from the thermal model evaluated with parameters from Table 1 are shown in Figure 5. Based on Figure 3 the saturation power (NEP) would vary from 11.7 pW ($1.56 \cdot 10^{-17} \frac{\mathrm{W}}{\sqrt{\mathrm{Hz}}}$) to 8.4 pW ($1.70 \cdot 10^{-17} \frac{\mathrm{W}}{\sqrt{\mathrm{Hz}}}$) across the array with no underside Au and no central heatsinking. With the combination of both underside Au and central heatsinking, the saturation power (NEP) is 12.1 pW ($1.55 \cdot 10^{-17} \frac{\mathrm{W}}{\sqrt{\mathrm{Hz}}}$) to within 0.5% (0.14%) across the entire array. The small deviation between T_U and T_{Si} suggests that at 300 mK, it would be an acceptable simplification to add the thermal conductivities of the Au and Si and solve only one diffusion equation.

CONCLUSIONS

We have provided a thermal model for a 256 pixel NIS-cooled bolometer array. Despite the large additional heat load due to the addition of NIS coolers, our thermal design will limit temperature gradients across the array to less than 3 mK and variation in saturation power (NEP) to less than 0.5% (0.14%).

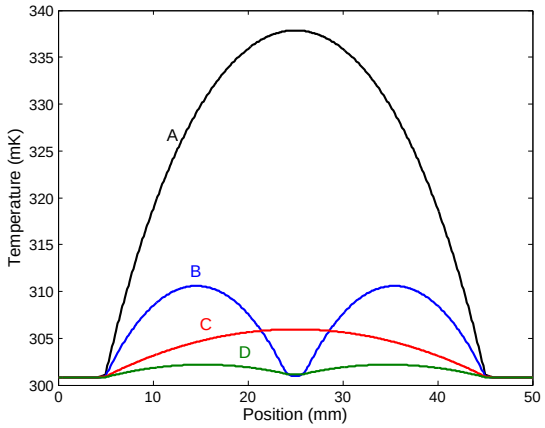

FIGURE 5. Results of the thermal model. Trace A shows the temperature of the Si substrate phonons, T_{Si}, with no underside Au and no central heatsinking. Trace B show no underside Au and a central heatsink that is 2.5mm by 7.5mm in area. Trace C shows 5 μm of underside Au with no central heat sink. Trace D combines the heatsink from B and the underside Au from C. The maximum deviation between T_U and T_{Si} is $\sim$0.15 mK and occurs at the center of the array in trace B.

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