

# Electronics for a Next-Generation SQUID-Based Time-Domain Multiplexing System

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**Abstract.** A decade has elapsed since the design, development and realization of a SQUID-based time-division multiplexer at NIST. During this time the system has been used extensively for low-temperature-detector-array measurements. Concurrently, there have been substantial advancements both in detector array and commercial electronic component technology. The relevance and applicability of the technology has blossomed as well, often accompanied by more demanding measurement requirements. These factors have motivated a complete redesign of the NIST room-temperature read-out electronics. The redesign has leveraged advancements in component technology to achieve new capabilities better suited to the SQUID multiplexers and detector arrays being realized today. As examples of specific performance enhancements, the overall system bandwidth has been increased by a factor of four (a row switching rate of 6.24 MHz), the compactness has been increased by over a factor of two (a higher number of detector columns and rows per circuit board), and there are two high speed outputs per column (allowing fast switching of SQUID offsets in addition to digital feedback). The system architecture, design implementations, and performance advantages of the new system will be discussed. As an application example, the science chain flight electronics for the Micro-X High Resolution Microcalorimeter X-ray Imaging Rocket will be described as both a motivation for, and a direct implementation of the new system.

**Keywords:** SQUID, multiplexing, instrumentation, transition edge sensor.

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## INTRODUCTION

A complete redesign of the time-division SQUID multiplexer (TDM) room temperature electronics is underway at NIST. The legacy system [1], developed around the turn of the millennium, has proved instrumental in the implementation and advancement of SQUID based TDM for transition edge sensor (TES) detector array readout. The system has found wide acceptance through worldwide deployment and has been proven for a wide range of applications [2-4]. The system has also served as the template for the development of the multichannel electronics (MCE) at the University of British Columbia [5]. The MCE are currently in use on, or undergoing qualification for, several major astronomical instruments including SCUBA2, ACT, SPIDER, BICEP and CCAT.

The motivation for the system redesign is a result of both advancements in electronic component

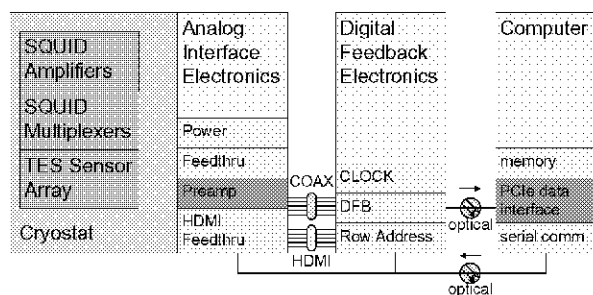
technology, which enables higher performance in the room temperature electronics, and recent developments in TES detector array and SQUID read-out technology, which will leverage these improvements to achieve unprecedented system performance.

## SYSTEM ARCHITECTURE

The architecture of the new system is similar to that of the legacy system. A block diagram of the system is shown in figure 1. The main changes in the architecture reflect increases in the functional density on the new circuit boards. While the 3U crate standard has remained the template for the board designs, advancements in component technology have allowed increases in the number of channels (rows and columns) instrumented per board. For the new digital feedback card design (DFBx2) a single board has

circuitry to control two columns. And for the new row address driver card design (RA16) the number of row drivers has been doubled from eight to sixteen per board.

As seen in Fig. 1 there are two major system components still under development. To handle the increased data rate from the new system when driving larger arrays at fast multiplexing rates, redevelopment of the data interface to the host computer is necessary. A prototype data interface utilizing the peripheral component interconnect express (PCIe) computer expansion card standard is under development. And to achieve the higher open loop bandwidth required for faster multiplexing, redevelopment of the analog conditioning circuitry is underway.



**FIGURE 1.** A functional block diagram for the next generation TDM system. Items in green are fully designed and verified, items in red are under development, items in yellow are legacy components.

## SYSTEM DESIGN

The system redesign was focused on achieving the following goals; faster multiplexing capability, enhanced functional capability, increased functional density, and upgrading of components (to avert obsolescence).

The main redesign efforts have been focused on the DFBx2 and RA16 cards. Both cards have substantial hardware and firmware modifications as described below. Considerable effort was expended to assure complete reverse compatibility with the legacy system. Currently, there is no immediate need or plan to redesign the legacy CLOCK card for the new laboratory system. We may however opt to migrate an alternate improved design implementation to the 3U form factor to function as the system clock card. This new design, developed by NASA GSFC specifically for the Micro-X program, has the beneficial feature of a USB interface for commanding and limited data streaming. As another option, we also have the capability to configure a DFBx2 card (with an enabled on board oscillator) as the system timing card.

**TABLE 1.** Component specification comparison for the legacy and next generation designs.

Component/Spec	Legacy	DFBx2/RA16
<b>ADC</b>		
device	AD6640	AD9230
bits	12	12
sample rate [MSPS]	65	170-250
<b>DAC</b>		
device	AD9754	AD9744
bits	14	14
update rate [MSPS]	125	210
<b>FPGA</b>		
device	Altera	Altera
	APEX	Cyclone III
	1:P20K100	1:P3C25
logic elements	4160	24624
memory [Kbits]	53	594
I/O [pins]	159	215

## Digital Feedback Card

The redesign of the analog front end to the DFBx2 card was required to accomplish the target improvement in multiplexing speed of a factor of four. This represents an increase from a row switching rate of 1.56 MHz in the legacy system (a row dwell period of 640 ns) to 6.25 MHz in the redesigned system ( a row dwell period of 160 ns). This 4X speed improvement is derived from a combination of an increase in the system master clock rate by a factor of two (from 50 MHz to 100 MHz) and an increase in feedback algorithm efficiency and commensurate data piping rate by a factor of two (reducing the row dwell time from 32 to 16 master clock cycles). The utilization of the AD9230 analog-to-digital converter (ADC) allows sampling at 100 MHz with plenty of headroom (refer to Table 1 for component specifications). And the low voltage differential signaling (LVDS) output mode assures high data transmission fidelity to the FPGA.

The replacement of the legacy digital-to-analog converters with the AD9744 device enables the complete front end to run at speeds up to 200 MHz. The new design has added a second DAC for each feedback column. This 2<sup>nd</sup> DAC can be used as a high speed programmable feedback offset to the multiplexer 2<sup>nd</sup> stage SQUID. This effectively widens the tolerance to physical parameter variation (critical current, normal state resistance) in the 1<sup>st</sup> stage multiplexer SQUIDs. More explicitly, the bias chain operating point can be fine tuned on a row by row basis to realize more uniform gain.

Substantial improvements in field programmable gate array technology (FPGA) have been leveraged by upgrading to a component from the Cyclone III family of devices by Altera. The resources of the EP3C25

allow the parallel and independent implementation of two channels of digital feedback in a single device. The high I/O count in the 324 pin ball grid array package allows physical realization of the interfaces to [2] ADC's and [4] DAC's per FPGA. This FPGA also benefits from dedicated phase locked loop circuitry (PLL) for stabilizing, multiplying, and distributing the master system clock, and embedded multipliers to optimize and accelerate the feedback computation algorithm.

Another major design change involves the inclusion of a 2<sup>nd</sup> identical FPGA in the data path for real-time processing of signals from the digital feedback FPGA. There are a multitude of potential tasks for this 2<sup>nd</sup> FPGA. Possible data management tasks include stream formatting, configurable interfacing to various data transmitters, and double data rate (DDR) streaming for high data rate applications. Potential signal processing tasks include digital filtering, pulse detection and triggering, and feedback and error signal mixing.

In an effort to provide more agility in terms of the data interface, the data transmitter hardware has been migrated to a daughter card. Presently, a 125 MBd dual channel (one per column) optical transmitter daughter card is used to send data over plastic fibers to the legacy PCI card. Alternative transmitter implementations will be required at higher data rates.

Redevelopment of the firmware and hardware for this card has led to some new system capability. Most notably, the inclusion of the 2<sup>nd</sup> DAC and the capability to close the feedback loop on this output simplifies system characterization. Acquiring both feedback signals with one locked and the other providing a swept excitation allows direct measurement of SQUID and detector response curves. These can include  $V(\Phi)$ ,  $V(I)$ , and  $I(V)$  dependent on configuration. The new firmware implements multiple data modes that allow bundling of various combinations of feedback (DAC output level) and error signals (ADC input level) on the two channels. These new characterization capabilities will simplify development of tuning algorithms in the future.

### Row Address Card

The major change in the row address driver board design is the expansion to sixteen driver circuits on a single 3U card (a doubling in functional density). The DAC circuitry is identical to that for the DFBx2 design. The FPGA is identical as well.

For future system implementations, the RA16 will be used to source dc bias signals, both for the SQUID amplifiers as well as elements in the focal plane including heaters and detectors. This will replace the

functionality of the legacy BIAS tower cards (see [1] for a full description of the legacy system). Passive filters on the RA16 outputs can be configured to limit the noise bandwidth of the bias signals.

Expansion to sixteen channels per card has also mandated a change in interconnection strategy. In place of individual SMB connectors for each drive circuit the RA16 front panel presents four HDMI (high-definition multimedia interface) connectors. Each HDMI cable has four individual shielded twisted pairs rated for 340 MHz of bandwidth. Each cable carries four bias pairs from the row driver circuitry and it takes four cables to instrument the full sixteen rows.

The most substantive functional changes in the RA16 derive from modifications to the firmware. The firmware has been structured to act as an arbitrary state sequencer. Time division multiplexing is simply one mode of the sequencer. This modification allows any sequence of any combination of the sixteen channel states (signal level, enable). This mode has been implemented in anticipation of developments in multiplexing strategies other than TDM. This feature will be utilized for the code division multiplexing (CDM) scheme currently under development at NIST.

The firmware also allows individual control of the channels such that sequencing, dc level, or function generator emulation (triangle/sine/square) may be selected independent of the other channels on the card. And progress has been made towards sourcing low distortion sine wave signals at frequencies up to 100 kHz for complex impedance measurements of TES detectors.

### Data Interface Card

The legacy system utilizes a sixteen channel fiber optic receiver card mounted in the host computer with a PCI 1.0 interface. The PCI 1.0 standard has a maximum data transfer rate of 133 MB/s. This data rate is insufficient for many current and most future applications under consideration or development.

In conventional TDM the maximum data rate (DR) per column can be calculated as follows for the two systems:

$$DR_{legacy} = \frac{bits}{\tau_{dwell}} = \frac{32}{32 \times 20ns} = 6.25MB/s \quad (1)$$

$$DR_{DFBx2} = \frac{bits}{\tau_{dwell}} = \frac{32}{16 \times 10ns} = 25.0MB/s \quad (2)$$

$\tau_{dwell}$  is the row dwell time. For a 32 column array these data rates scale to 200 MB/s and 800 MB/s respectively.

To manage these large data rates we are developing a receiver card with a PCIe interface. This newer bus standard boasts much higher data rates than its predecessor: 250 MB/s for version 1, 500 MB/s for version 2, and 1 GB/s for version 3 (future). These rates are per lane and the bus architecture allows for up to 32 lanes in a physical PCIe expansion slot.

Our concept is being implemented on an Altera Arria GX development board. The Altera Arria device family is an FPGA product line specifically targeted at transceiver applications. These devices currently are available with an embedded soft core (license required) that implements the physical PCIe interface. In the near future a lower cost version of the device with a hard core (no license required) will become available.

The development board is based on four lane architecture with a corresponding 1 GB/s total data rate (PCIe v1.x). Tests on the embedded development board have validated sustained DMA transfer rates of 850 MB/s. Our prototype receiver will be built on a daughter card. We will employ four receivers, one per lane. Each receiver will stream data from a single DFBx2 card. This implies two columns of data per lane (eight columns per card) with a total data rate of 200 MB/s, well within both the specification and bench validation limits.

## SYSTEM PERFORMANCE

All components required for TDM are operating as intended. The system has been demonstrated to operate at a master clock rate of 100 MHz. Advantages resulting from the new functionality (i.e. 2<sup>nd</sup> stage SQUID feedback switching) are still under investigation.

In terms of noise performance, the analog front end circuitry performs comparably to the legacy system. With the input shorted, we typically measure a bit noise of 1-2 bits dependent on the system configuration. When referred to the input of the first stage SQUID this noise level does not contribute significantly to the system NEP.

We have measured the bit noise of the feedback signal to the 1<sup>st</sup> stage SQUID of a linear multiplexer at 4K under closed loop operation. Referring this noise to the 1<sup>st</sup> stage SQUID input we measure  $\sim 1 \mu\Phi_0 / \sqrt{\text{Hz}}$ , a value consistent with the noise expected from the SQUID at 4K.

We have also used the DFBx2 to measure the energy resolution of x-ray pulses from a <sup>55</sup>Fe source and achieved a FWHM of  $3.10 \pm 0.1$  eV at 5.9 keV without optimization. A direct comparison with the legacy system showed comparable results under identical measurement conditions.

## SYSTEM APPLICATION: MICRO-X

The initiative to undertake the system redesign was largely derived from the successful proposal to develop the payload for the Micro-X High Energy Resolution Microcalorimeter X-ray Imaging Rocket [6-8]. This sounding rocket will fly with a 121 pixel x-ray imaging TES array read-out with SQUID multiplexers. The science chain electronics are based in part on the designs presented in this paper.

The array will be instrumented as two independent 4 X 16 element sub-arrays to allow for redundancy should one side of the array fail during flight. Our collaborators at NASA GSFC have developed a master controller board which assumes all functionality for control and command, timing and synchronization, data management, and telemetry interface. The University of Florida, Gainesville, has developed the power supply. NIST will provide the cryostat interface electronics.

The circuit designs have been prototyped and are undergoing qualification. The designs will be migrated to the flight board format by the end of 2009. The system integration will occur at MIT during 2010. The first flight is scheduled for January of 2011 with Puppis A as the astronomical target. Successive flights are scheduled for mid-2012 and early 2014.

## REFERENCES

1. C. D. Reintsema, J. Beyer, Nam S. W., S. Deiker, G. C. Hilton, K. Irwin, J. Martinis, J. Ullom, L. R. Vale, and M. MacIntosh, *Rev. Sci. Instrum.* **74**, 4500-4508 (2003).
2. W. B. Doriese, J. N. Ullom, J. A. Beall, W. D. Duncan, L. Ferreira, G. C. Hilton, R. D. Horansky, K. D. Irwin, J. A. B. Mates, C. D. Reintsema, L. R. Vale, Y. Xu, B. L. Zink, *Appl. Phys. Lett.* **90**, 193508 (2007).
3. Kilbourne, C.A.; Doriese, W.B.; Bandler, S.R.; Brekosky, R.P.; Brown, A.-D.; Chervenak, J.A.; Eckart, M.E.; Finkbeiner, F.M.; Hilton, G.C.; Irwin, K.D.; Iyomoto, N.; Kelley, R.L.; Porter, F.S.; Reintsema, C.D.; Smith, S.J.; Ullom, J.N., *Proc. SPIE*, **7011**, 701104 (2008).
4. Niemack, M.D., *Proc. SPIE*, **6275**, 62750C (2006).
5. E. S. Battistelli, M. Amiri, B. Burger, M. Halpern, S. Knotek, M. Ellis, X. Gao, D. Kelly, M. MacIntosh, K. Irwin, C. D. Reintsema, *J. Low Temp. Phys.*, **151**, 908-914 (2008).
6. Figueroa-Feliciano, E. et al., *Proc. SPIE*, **7011**, 70113U (2008).
7. Wikus, P. et. al., *these proceedings* (2009).
8. Figueroa-Feliciano, E. et al., *these proceedings* (2009).