High-Voltage Capacitance Measurement System for SiC Power MOSFETs †

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***Abstract* -- Adequate modeling of a power MOSFET is dependent on accurate characterization of the inter-electrode capacitances. With the advent of high-voltage silicon carbide (SiC) power MOSFETs, it has become important to develop a measurement system that can perform and record high-voltage capacitance versus voltage measurements on these devices. This paper describes a measurement apparatus that safely and accurately allows high voltage capacitance-voltage (CV) measurements to be performed. The measurements are based on conventional LCR meter CV techniques but with added circuitry to interface the LCR meter to high voltage bias sources. The effects of the added circuitry are studied theoretically, and the CV measurement accuracy is verified with experimentation. High voltage capacitance voltage measurements are presented for both silicon and SiC power MOSFETs.**

***Index Terms*— Capacitance, CoolMOS™, CV measurement, high-voltage, LCR meter, power MOSFET, silicon carbide.** ‡

I. INTRODUCTION

It is well known that power MOSFETs have superior switching characteristics compared to other three terminal power switches. Because the power MOSFET is a majority carrier type device, there is no minority carrier charge to be removed when the device is switched. Under ideal conditions, the switching speed of a MOSFET is primarily determined by the charging and discharging of the device capacitances. The lack of minority-carrier charge results in a fast switching speed, but it also results in a higher on-state resistance. Scaling up the voltage rating of power MOSFET increases its on-state resistance to a point where conductivity modulated devices become the more efficient option. Advanced super-junction power MOSFET structures, such as CoolMOS™, help to reduce the on-state resistance of majority carrier devices at high voltage, but are difficult to manufacture for voltage ratings exceeding 1 kV [1].

Advances in silicon carbide (SiC) device fabrication have overcome the limitations of silicon power MOSFETS. The properties of SiC make it more suitable for high-power operation compared to silicon. In particular, SiC's breakdown electric field is nearly an order of magnitude larger than that of silicon. Research and development of SiC devices has yielded power MOSFETs that have superior resistance for given voltage and current ratings [2, 3]. SiC power MOSFETS can operate at high voltage (10 kV) and switch in less than 100 ns, permitting 20 kHz operation. This is nearly 100 times faster than the switching speed of conductivity modulated silicon devices with comparable voltage ratings. With these significant advances, it is essential to produce adequate models that fully describe the response of a SiC MOSFET under a wide range of conditions [2].

In order to model the switching waveforms of any power MOSFET, the MOSFET's inter-electrode capacitances must be known for a wide range of applied voltages [4]. Since there are few commercially available silicon power MOSFETs with blocking voltages exceeding 1 kV, there has not been a strong need for an accurate high-voltage CV measurement system. Therefore, typical CV measurement systems rarely exceed several hundred volts. Since SiC power MOSFETs are being developed with voltage ratings of 10 kV, it is desired to have a CV system that can apply a drain voltage of up to 5 kV in order to fully characterize the SiC MOSFET inter-electrode capacitances.

The purpose of this paper is to introduce a high-voltage, capacitance versus voltage (HV CV) measurement system which safely isolates applied DC voltages from the impedance meter that records the MOSFET's capacitance. The accuracy of this measurement system is analyzed and verified. For safety and ease of use, the process of taking these measurements is fully automated. Some examples of HV CV measurements are presented for 10 kV SiC MOSFETs and CoolMOS™ devices. Additionally, the safety system utilized to protect all users of the measurement system is briefly discussed.

II. MEASUREMENT CIRCUIT

A. C-V measurement circuit layout

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‡ Certain commercial products are identified in this paper to adequately describe the performed experimental procedures or results, and this identification does not necessarily imply any recommendation or endorsement by NIST.

The complexity of this HV CV circuit arises because a typical LCR meter is voltage sensitive and cannot withstand applied DC voltages on the order of 1 kV or more [5]. The goal of the new system is to enable CV measurements with applied voltages of up to 5 kV across the drain-source terminals of a SiC power MOSFET. To accomplish this, a protection circuit must be added to isolate these high voltages from the LCR meter. Implementing this protection circuit in a way that maintains accuracy and safety is a challenge in developing the new system.

The circuit layout for the HV CV apparatus is shown in Fig. 1. Fig. 1(a) shows the main CV system, which attaches to the circuit shown in Fig. 1(b) at terminals CM1 and CM2. The main CV system consists of six connection terminals (CM2', DUT1, SG, VdRef, Drain, and DUT2) that are used to generate the three capacitance measurement configurations; gate-drain capacitance (C_{GD}), drain-source capacitance (C_{DS}), and gate-source capacitance (C_{GS}). The **Gate Bias Supply** and **Low Voltage or High Voltage Drain Supply** are used to control the gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}). The **Gate Volt Meter** and **Drain Volt Meter** are used to measure V_{GS} and V_{DS}, as current leakage through the MOSFET terminals will cause supplied and measured voltage values to deviate. Resistors are placed in series with the voltage meters to suppress any noise and parasitic capacitances that the voltage meters generate.

Capacitors, C_{CD} and C_{CG}, block the high DC voltage from the terminals of the LCR meter. If the device should suddenly fail during a high-voltage capacitance measurement, a large transient can be coupled into the LCR meter causing it to be destroyed. The resistors, R_{CD} and R_{CG}, shown in Fig. 1 control the magnitude of this current during such a failure and allow the diode bridge to safely clamp the voltage in order to protect the LCR meter. The **AC adaptor** and associated bipolar rectifier components are present to ensure that the diode bridge is always in reverse bias during normal circuit operation, and therefore, this bridge's impedance is always very high. This minimizes the bridge's effects on the CV measurement.

Fig. 2 shows the three capacitance measurement configurations, including (a) C_{GD}, (b) C_{DS}, and (c) C_{GS}. These three configurations enable the flexibility to accurately measure three different forms of capacitance in three terminal devices with a high impedance switch input.

B. Safety considerations

The measurement circuit is contained in a plastic safety box with safety interlock switches that prevent high voltage from being applied to any user-accessible terminals when the lid is open. In addition, a three-color tower-light indicates the status of the system: off condition, standby condition, and energized condition. Fig. 3 shows the high- voltage CV

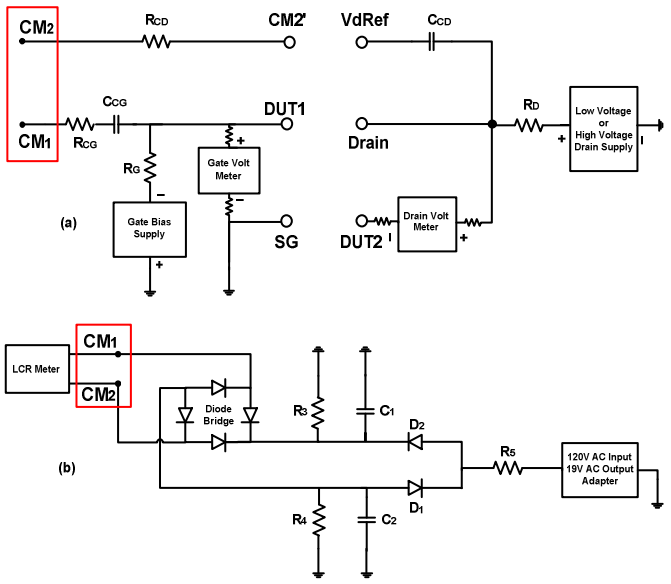


Fig.1. High voltage capacitance-voltage circuitry; (a) main circuitry showing terminal points, voltage supply, voltage meter, and DC blocking capacitors; (b) hookups to LCR meter and bridge rectifier.

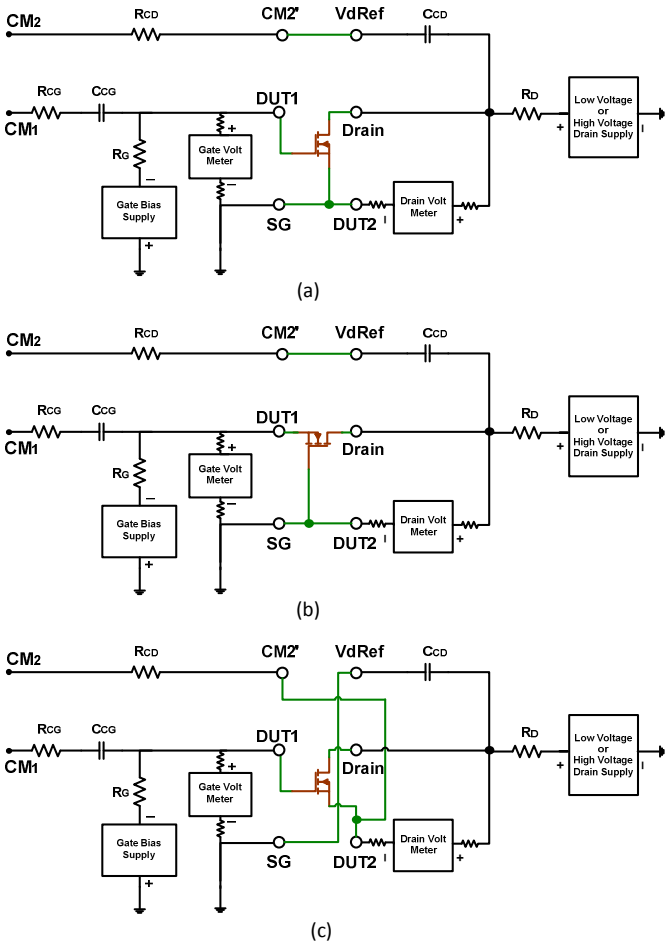


Fig. 2. The three capacitance measurement configurations (a) C_{GD}, (b) C_{DS}, and (c) C_{GS}.

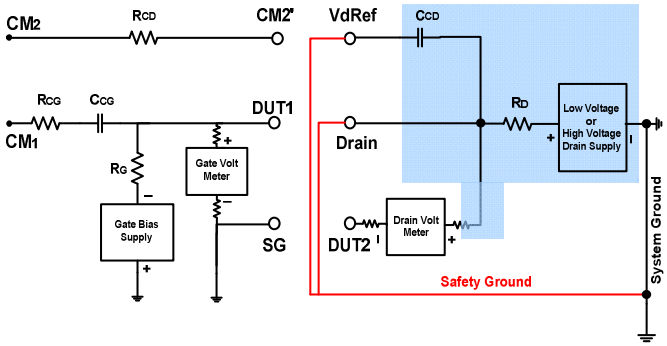


Fig. 3. High-voltage CV circuitry indicating the system ground, the safety ground, and the high-voltage section (the blue shaded area) is isolated from the rest of the circuit components for safety.

circuitry indicating that the high-voltage section (the blue shaded area) is isolated from the rest of the circuit components providing double insulation for additional safety. The system ground is the LCR meter ground, and this point is connected to the building ground. The indicated red safety grounds are a pair of ground clips that the user must attach to the terminals indicated in Fig. 3 to be assured that the indicated terminals contain no hazardous voltages. This is a back-up feature as, once the safety box is opened, power is shut down. However, it is possible that the high-voltage coupling capacitors in the system could contain residual charge, and the ground clips serve to remove this charge.

III. Analysis of Capacitance Voltage Measurement System

After developing the HV CV circuit, it is necessary to verify that the additional passive and active components of this circuit do not cause inaccuracies in the capacitance data taken by the LCR meter. This section examines the LCR meter measurement method, and the total impedance of the measurement system, and it presents equations to describe the system's accuracy.

The LCR meter is an auto balancing bridge LCR meter. It has two input terminals, high and low. Fig. 4(a) shows a crude diagram of how the LCR meter measures impedance [6]. The virtual ground causes the impedances Z_H and Z_L to have no effect on the measurement of voltage and current at the high and low terminals, respectively.

Fig. 4(b) shows an equivalent circuit of a C_{GD} measurement, derived from component impedances that are grouped together and shown in Fig. 4(c). In Fig. 4(c), impedances R_{GSMSR} and C_{GSMSR}, represent the equivalent impedance of the **Gate Volt Meter** and impedances, R_{DSMSR} and C_{GSMSR}, represent the equivalent impedances of the **Drain Volt Meter**. The presence of the coupling capacitors and series resistors, represented with Z_{CCD} and Z_{CCG}, in series with the high and low terminal points of the LCR meter cause the measurement of C_{GD} to be inexact. The inaccuracy of this impedance measurement is dependent on the magnitude of Z_{CCD} and Z_{CCG} relative to the MOSFET's impedance.

AC current flowing through the drain coupling impedance, Z_{CCD}, will cause a voltage drop between Z_{GD} and the virtual ground. Therefore, the parallel Z_{DS} branch will have an equal voltage, and some of the current, I_{GD}, will be diverted from reaching the LCR's internal am meter. The ratio of current that is diverted from the LCR's terminals is described with a current divider,

$$\frac{I_{MSR}}{I_{GD}} = \frac{Z_{DS}}{Z_{DS} + Z_{CCD}}. \tag{1}$$

The voltage drop across Z_{CCD} must also be taken into consideration,

$$\frac{V_{GD}}{V_{MSR}} = \frac{Z_{GD}}{Z_{GD} + \dfrac{Z_{CCD} Z_{DS}}{Z_{CCD} + Z_{DS}}}. \tag{2}$$

Equations (1) and (2) show that the smaller Z_{CCD} is compared to Z_{GD} and Z_{DS}, the less is the voltage across Z_{CCD} and the current diverted from the LCR meter. Therefore more accurate impedance measurements result.

In order to reduce the voltage across Z_{CCG}, the equivalent impedance of Z_{GD} in parallel with Z_{GS} must be much larger than Z_{CCG}. Solving the voltage divider in terms of V_{GD} and V_{MSR} gives the transfer function

$$\frac{V_{GD}}{V_{MSR}} = \frac{1}{1 + Z_{CCG}\left(\dfrac{Z_{GD} + Z_{GS}}{Z_{GD} Z_{GS}}\right)}. \tag{3}$$

All the effects of Z_{CCD} and Z_{CCG} cause the LCR meter to inflate the true value of the MOSFET's impedances. These capacitance measurements will then be smaller than the true MOSFET inter-electrode capacitances.

The total accuracy of an LCR measurement taken with this circuitry is derived using the product of Eqs. (1), (2), and (3);

$$\%\,Accuracy = \left(\frac{Z_{DS}}{Z_{DS} + Z_{CCD}}\right)\left(\frac{1}{1 + Z_{CCG}\left(\dfrac{Z_{GD} + Z_{GS}}{Z_{GD} Z_{GS}}\right)}\right)\left(\frac{Z_{GD}}{Z_{GD} + \dfrac{Z_{CCD} Z_{DS}}{Z_{CCD} + Z_{DS}}}\right). \tag{4}$$

Equation (4) is verified by conducting a controlled measurement with a network of three capacitors all connected with one another. This emulates the inter-electrode capacitance within a MOSFET in a static way to determine whether or not the predicted accuracy is on target with the measured accuracy of MOSFET capacitance.

The exact value of each of the capacitors is measured directly with the LCR meter, not using the HV CV circuitry. Then, using the HV CV circuitry, another measurement is

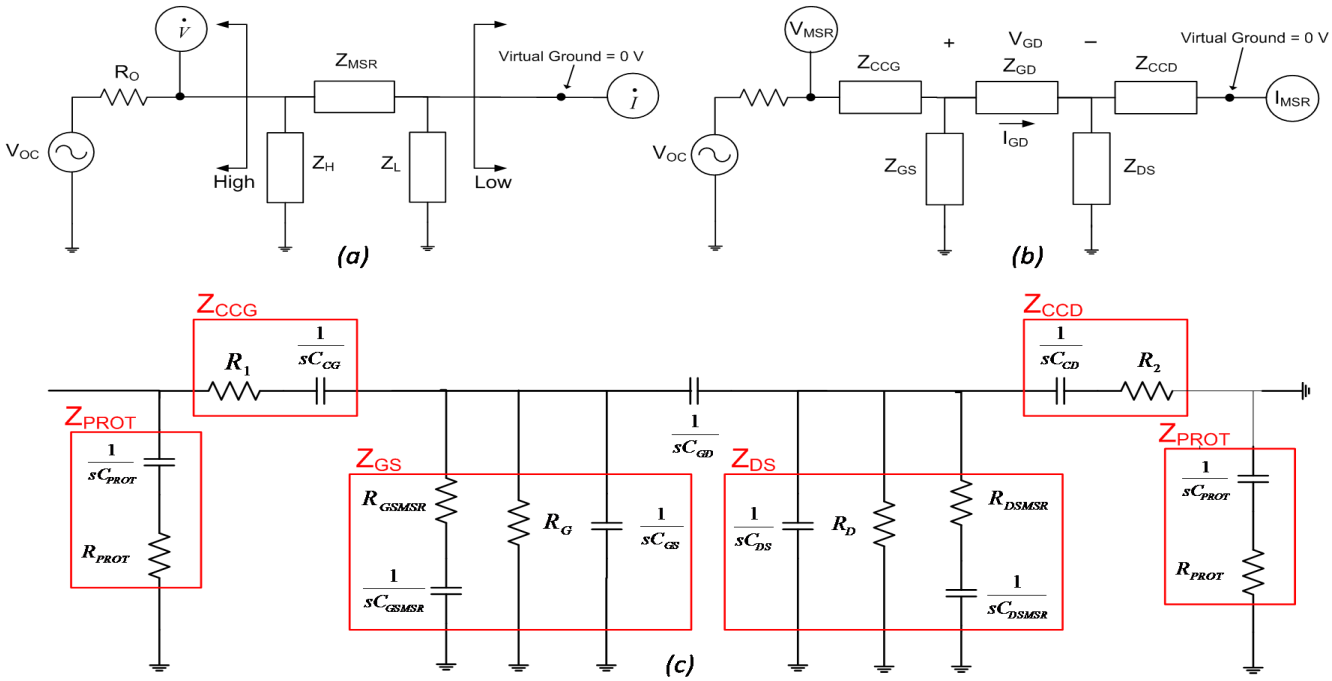


Fig. 4. (a) Basic sketch of LCR measurement method, (b) sketch of the LCR meter with the HC CV circuitry applied, and (c) an expanded version of the HC CV circuitry showing the equivalent impedances of all HV CV components.

taken of the capacitor network. The accuracy of the HV CV measurement is compared with the predicted accuracy, using (4) and the component values that make up the HV CV circuit.

Table 1 shows the results of this verification experiment. The calculated and measured accuracies are all within 1 % of each other. With a maximum offset between measured and calculated accuracy of only 1 %, it is reasonable to assume that the equation developed to predict the accuracy of this high-voltage CV circuit is correct.

The larger the MOSFET's capacitance, the larger the coupling capacitors must be in order to achieve precise measurements. In order to maximize the safety of this measurement system, it is important to understand the approximate maximum value of each inter-electrode MOSFET capacitance and insert coupling capacitors that guarantee acceptable accuracy. Using coupling capacitors that are exceedingly larger than maximum MOSFET capacitance will attain much higher accuracy than necessary and will also store a needless amount of energy during high-voltage measurements. This stored energy can pose as a hazard to the measurement apparatus and the user if there is a failure.

TABLE I
MEASURED AND CALCULATED CAPACITANCE VALUES USING A HV CV CIRCUIT WITH COUPLING CAPACITORS VALUES OF 0.1 µF

Capacitance	Real Capacitance	Measured Capacitance	Accuracy of Measurement	Calculated Accuracy
C_{GD}	3.037 nF	2.726 nF	89.76 %	89.86 %
C_{DS}	1.000 nF	0.9219 nF	92.19 %	91.60 %
C_{GS}	3.929 nF	3.698 nF	94.12 %	93.56 %

IV. SOFTWARE INTERFACE AND OPERATION

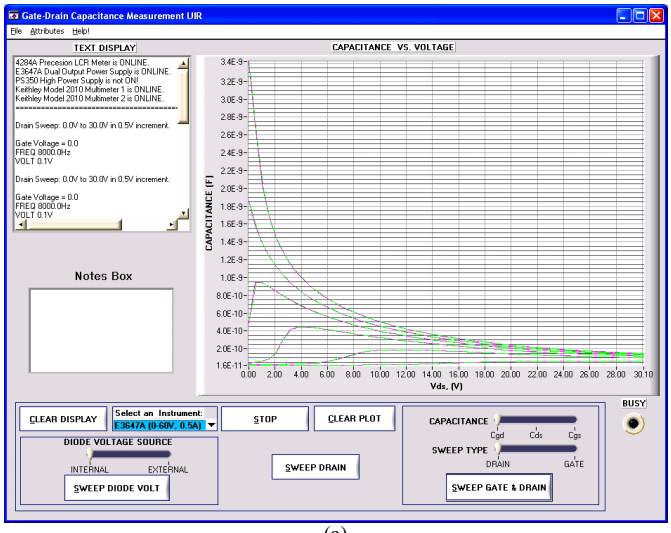
The software that is utilized to perform this HV CV measurement is part of a larger parameter extraction program, IGBT Model Parameter extrACtion Tools (IMPACT) [7]. This program was previously extended to include HV drain depletion capacitance measurements for SiC power MOSFETs [8]. In this paper, the software is further extended to include three capacitance measurement configurations; gate-drain capacitance (C_{GD}), drain-source capacitance (C_{DS}), and gate-source capacitance (C_{GS}). The **Sweep Gate & Drain** button in Fig. 5(a) is expanded to allow the various combinations of both capacitance type (e.g., C_{GD}, C_{DS}, or C_{GS}) and sweep voltage type (e.g., gate or drain) measurements to be made. From the HV capacitance measurement front-panel shown in Fig. 5(a), the operator can specify which capacitance is being measured; which voltage parameter, gate, or drain, is placed on the X-axis; and which voltage source is used. The text display at the top left corner of the screen displays the most current action the program is performing.

The coupling capacitors and current limiting resistors that are used to isolate the LCR meter from destructive voltages affect the accuracy of the measurement as described in section II. In order to get a check on accuracy, the sweeps are done both with an increasing voltage ramp and also a retracing decreasing voltage ramp. Both tracings are plotted as shown in Fig. 5. In Fig. 5(a), these traces lie on top of each

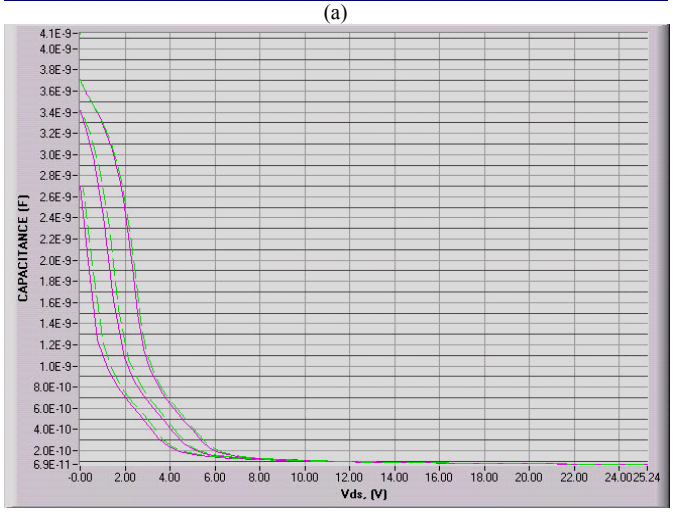
other, while in Fig. 5(b) hysteresis indicating error is visible. To reduce this hysteresis error, larger coupling capacitors or a higher measurement frequency may be needed.

To perform the HV capacitance measurements, the user first needs to set up the attributes by selecting the "Attributes" option on the menu bar of Fig. 5(a), which opens the sub-panel shown in Fig. 6. From this sub-panel, the user can set up the LCR small signal parameters and the gate step and/or drain voltage sweep values. For Drain Setup, either a low-voltage power supply or a separate high-voltage supply is used, and there is a separate box for each. The Sweep Diode Bias box is for two-terminal CV measurements. Additional delay parameters are included to enable the coupling capacitors to be charged after changing the bias voltages [8].

In the **Measurement Error** box in Fig. 6, the user enters the *Relative Error* to be allowed. This is the maximum difference between the applied input voltage and the actual voltage on the MOSFET terminal as measured with either of the dc voltmeters shown in Fig. 1(a). If the MOSFET is leaky, there will be a difference between these two values.



(a)



(b)

Fig. 5. HV capacitance measurement front-panel: (a) no hysteresis effect and (b) hysteresis effect.

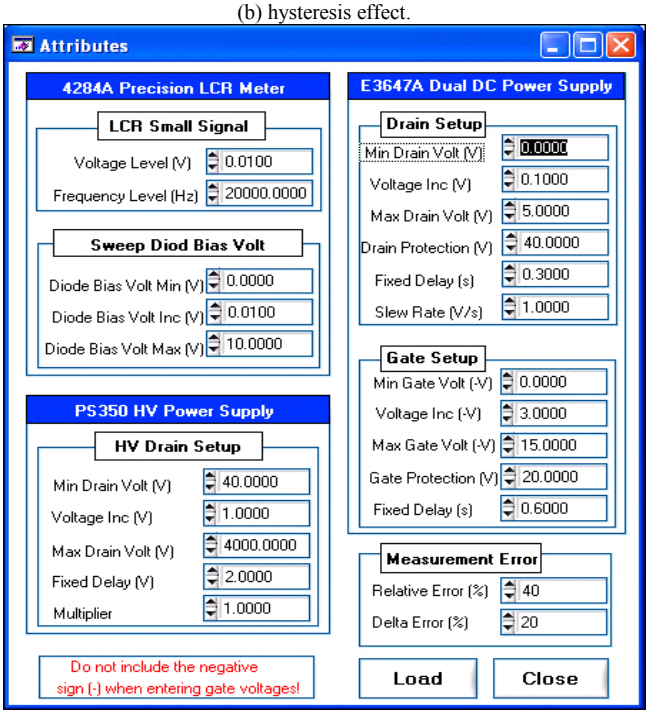


Fig. 6. HV capacitance measurement sub-panel.

To perform a measurement over the full desired voltage range, the relative error value may have to be increased or the MOSFET swapped out for a less leaky device. The *Delta Error* is the maximum allowable difference, for each voltage sweep, that a stepped voltage value is allowed to deviate from its starting value.

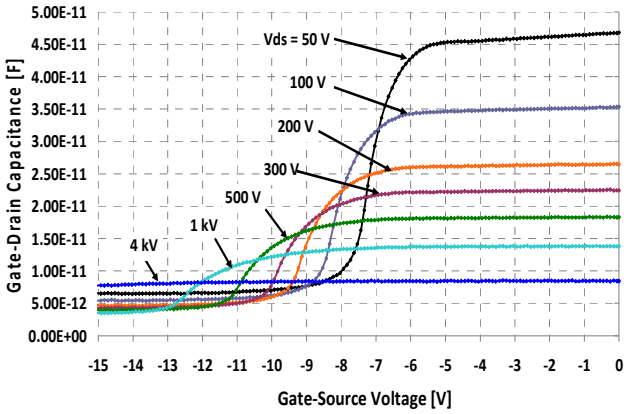
V. High-Voltage Capacitance Voltage Measurement Results

Fig. 7 shows the measured C_{GD} versus V_{GS} for both (a) a 10 kV, 5 A SiC MOSFET and (b) a 650 V, 60 A Si CoolMOS^{TM} at a frequency of 20 kHz. For more negative gate voltages, the gate drain capacitance becomes shielded by an inversion layer under the gate-drain overlap. This shielding effect is apparent by the sudden drop in capacitance value as V_{GS} becomes more negative. At higher drain voltages, C_{GD} is lower due to the wide depletion region under the gate-drain overlap [9]. Fig. 8 again shows the measured C_{GD} results, with V_{DS} on the horizontal axis and with V_{GS} as a parameter. Note that for the Si CoolMOS^{TM} device, the C_{GD} goes through a minimum around 70 V V_{DS} shown in Fig. 8(b), and this is reflected in Fig. 7(b).

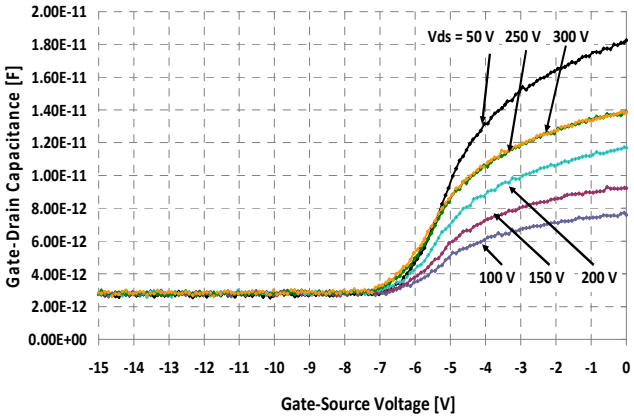
Fig. 9 shows the measured C_{DS} versus V_{DS} for (a) a 10 kV, 5 A SiC MOSFET and (b) a 650 V, 60 A Si CoolMOS^{TM} at a frequency of 20 kHz. The C_{DS} decreases with V_{DS} due to the increasing drain-source depletion width for both the SiC and Si devices.

Figs. 10 and 11 show the C_{GS} versus V_{GS} and C_{GS} versus V_{DS} for (a) a 10 kV, 5 A SiC MOSFET and (b) a 650 V, 60 A

Si CoolMOS™ at a frequency of 20 kHz, respectively. For more negative V_{GS}, the gate-drain overlap becomes inverted,

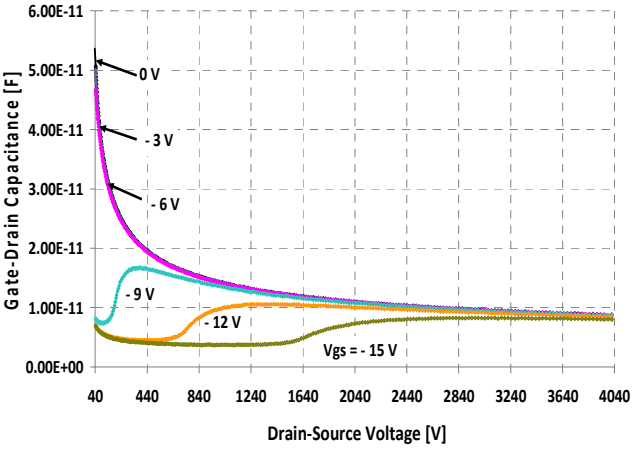


(a)



(b)

Fig. 7. Measured gate-drain capacitance versus gate-source voltage for (a) a 10 kV, 5 A SiC MOSFET and (b) a IPW60R045CP 650 V, 60 A Si CoolMOS™ at frequency of 20 kHz.



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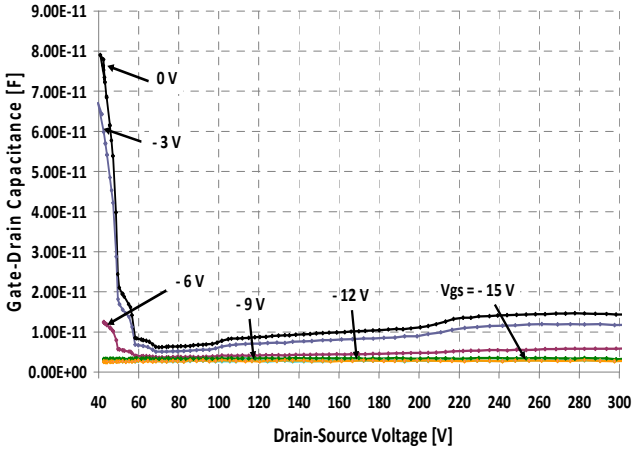
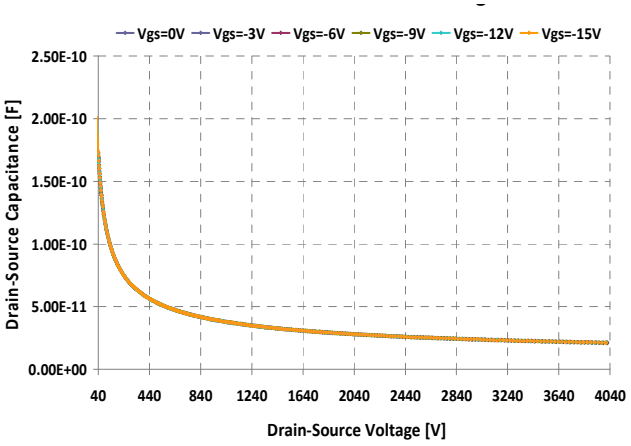


(b)

Fig. 8. Measured drain-source capacitance versus gate-drain voltage for (a) a 10 kV, 5 A SiC MOSFET and (b) a IPW60R045CP 650 V, 60 A Si CoolMOS™ at frequency of 20 kHz.



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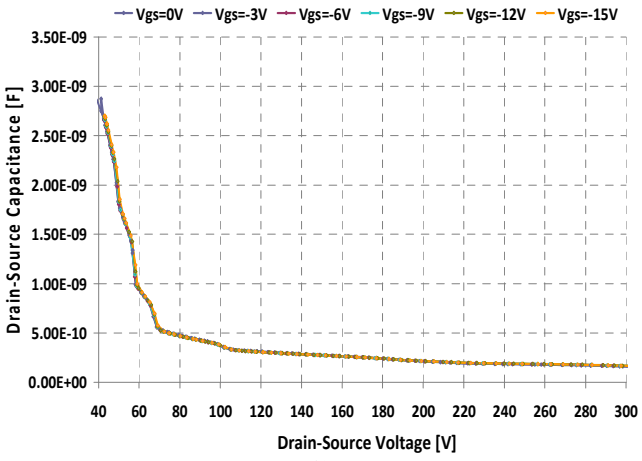
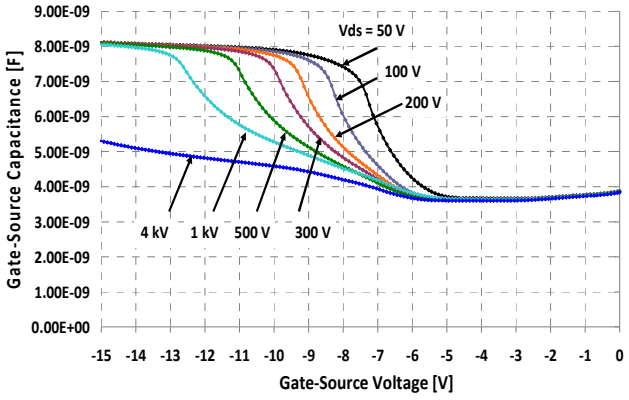


(b)

Fig. 9. Measured drain-source capacitance versus drain-source voltage for (a) a 10 kV, 5 A SiC MOSFET and (b) a IPW60R045CP 650 V, 60 A Si CoolMOS™ at frequency of 20 kHz.



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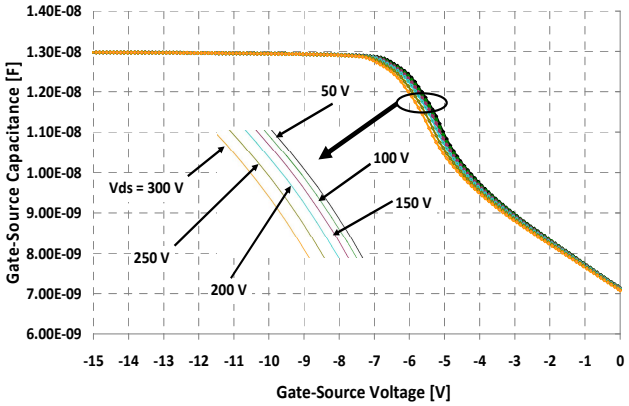
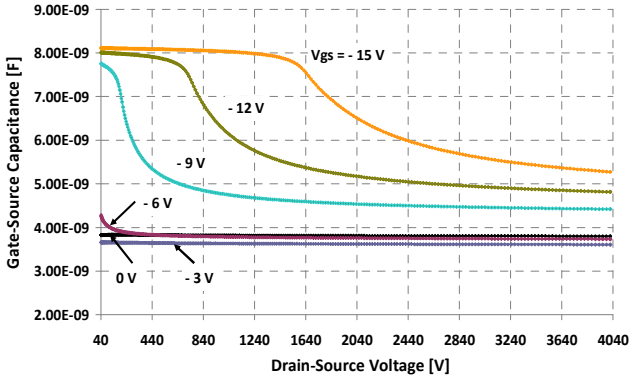
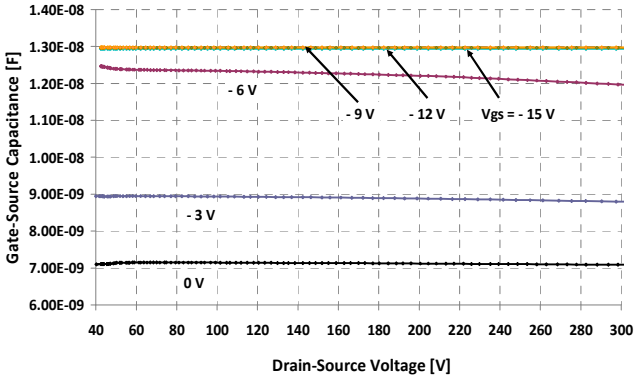


(b)

Fig. 10. Measured gate-source capacitance versus gate-source voltage for (a) a 10 kV, 5 A SiC MOSFET and (b) a IPW60R045CP 650 V, 60 A Si CoolMOS™ at frequency of 20 kHz.



(a)



(b)

Fig. 11. Measured gate-source capacitance versus drain-source voltage for (a) a 10 kV, 5 A SiC MOSFET and (b) a IPW60R045CP 650 V, 60 A Si CoolMOS™ at frequency of 20 kHz.

and the gate to gate-drain overlap inversion layer capacitance is shunted to the source contact through the body region, increasing the total gate-source capacitance. For higher V_{DS}, the back gate bias effect reduces the inversion layer width and decreases the gate-source capacitance. Note that for the SiC MOSFET device, the C_{GS} varies with V_{DS} while the Si CoolMOS™ device does not.

VI. Conclusions

In this paper, a measurement system is described that safely and accurately allows up to 5 kV CV measurements to be performed on high-voltage SiC and Si devices. The measurements are based on conventional LCR meter CV techniques but with added circuitry to interface the LCR meter to high-voltage bias sources. The effects of the added circuitry are studied theoretically, and the CV measurement accuracy is verified with experimentation. The IMPACT software package has been extended to include three capacitance measurement configurations; gate-drain capacitance, drain-source capacitance, and gate-source capacitance. High voltage capacitance voltage measurement results for both Si CoolMOS™ and SiC power MOSFETs are demonstrated.

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