Micrometer-width damascene copper conductors at ≥10 MA/cm^2*

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***Abstract*—We have applied high amplitude (~10 MA/cm^2) alternating current (AC) at 100 Hz and direct current (DC) to copper interconnect lines with widths in the few-micrometer range covered with a thick layer of SiO_2. Under our test conditions of Joule heating, the lines typically fail with lifetimes from 100 to 100,000 s, with a well-defined correlation between cyclic temperature range and the logarithm of lifetime. Post-test scanning electron microscopy (SEM) examination reveals substantial voiding and grain growth, particularly in AC tests at the higher cyclic temperature ranges. Lines without the full SiO_2 constraint fail much sooner than the constrained lines for similar cyclic temperature ranges. The less-constrained lines also had surface contours that were not present on the fully constrained lines. Optical observations during the tests indicate that the void generation behavior appears different during the AC and DC tests, with a saturation behavior occurring in the AC tests, sometimes long before failure. The distributed void density in our AC tests was at least as great as that in the DC tests.**

Keywords--alternating current; fatigue; grain; void;

I. INTRODUCTION

This paper presents observations on the behavior of damascene copper lines under high current density of the order of 10 MA/cm^2, both alternating current (AC) and direct current (DC). Our interest arises from two threads in engineering and technology: (1) reliability of electronic interconnects; and (2) use of electrical stressing as a probe of material properties. The reliability of micrometer- and nanometer-scale conductors in electronic interconnect structures is a perennial issue for electrical and electronic devices, as it is now with regard to the copper damascene structure. The International Technology Roadmap for Semiconductors indicates that design current densities for "intermediate wires at 105 °C" crossed the 1 MA/cm^2 threshold in the year 2008 [1]. The Roadmap foresees requirements exceeding existing capability for current density in the year 2013, at a density of 2.25 MA/cm^2. The reliability of these conductors is clearly a thermomechanical issue, because it involves stress and temperature. Very high mechanical stresses have been found to exist in copper damascene interconnect structures [2]. The controlling material factors have been considered to be interfaces, such as grain boundaries within the metallic conductor and adhesive bonds between the conductor and its surrounding dielectric. The present status of opinion within the microelectronics industry is that voids are key elements in important failure mechanisms in interconnects. Investigators have extensively studied two types of voids: electromigration voiding [3], where mass flow caused by electrical current has a predominant role; and stress-induced voiding [4], where the relaxation of process-induced stresses plays the key role. Mechanisms involved in the generation and behavior of voids are clearly central to the reliability of electrical conductors under high current, but it is difficult to evaluate them. Thermal cycling by Joule heating is a useful method of imposing local thermal and thermomechanical cycling as a means of studying these failure mechanisms [5]. Temperature cycling using a furnace at very low frequencies is a classical "stressing" method for testing the integrity and reliability of electronic structures and devices [6]. High-amplitude DC is well known to cause electromigration voiding, which is a critical reliability issue for microelectronic interconnects. Specific tests for characterizing electromigration resistance are widely documented [3].

Several research groups, including ours, have been exploring the use of electrical testing to obtain information about the mechanical behavior of thin films [5, 7-8]. Electrical testing can impose two key stress quantities in addition to the current, mechanical stresses and temperature, but not independently. What differentiates this approach from the widely practiced accelerated stress testing of various types [5] is the effort to link the performance in the electrical tests to values of specific conventional mechanical properties such as fatigue lifetime and yield and ultimate tensile strengths, rather than focusing solely on predicting service lifetime. High-amplitude alternating current (AC) has been used for most of the research on electrical testing for mechanical properties, denoted as AC fatigue [5]. A series of reports on aluminum lines has shown that electrical testing can produce thermomechanically induced mechanical fatigue [9]. This approach to fatigue testing, although without precedent in the macro world, offers significant advantages for thin films and nanostructures. In particular, the electrical

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approach offers applicability to buried and otherwise inaccessible structures and to very small structures. However it is also reasonable to expect that electrical testing may be a way to probe, test, and characterize the material properties involved in physical mechanisms that are more clearly and closely related to failure of electrical conductors. Since many nanostructures are physically buried and inaccessible for mechanical testing, electrical testing, which is conveniently implemented, offers the possibility of use for inspection or quality control.

This paper describes the techniques and specimens used and experimental results on damascene copper conductors typical of commercial microelectronics. The observations are on few-micrometer-wide lines; the advantage to using wide lines is that information can be obtained from optical observations during testing, which is impossible in the narrower lines. The focus here is on the phenomenological results of applying AC and DC current densities of the order of 10 MA/cm^2. These results include the generation of voids with dimensions up to a micrometer, grain growth and related microstructural changes, and electrical failure. It is expected that such results will provide new insight into the physical understanding of DC electromigration, and also offer a powerful means for investigating the effects of temperature, electrical current, and mechanical stress on void formation.

II. Experiment

The specimens used here were damascene copper conductors manufactured by use of typical commercial practices of the microelectronics industry. The electrodeposition and related processes leave residual hydrostatic tension in the lines [10]. The lines tested had widths of approximately 3 or 5 μm and were electroplated into trenches in SiO_2 dielectric. The constrained lines had an optically transparent overlayer of SiO_2 about 700 nm thick, as measured by imaging a cross section in the SEM (scanning electron microscope). Lines designated as 'thin constraint' had a SiN coating, discovered by serendipity, produced by thermal annealing of the damascene structure at temperatures of 300 °C and above for a few hours. This SiN coating was typically less than 100 nm thick, as estimated from energy-dispersive x-ray measurements in the SEM. The test structures included contact pads that were used for the test probes. All tests were run under voltage control [11]. The constrained lines were tested in air in a probe station, while the unconstrained lines were mounted in chip carriers, wire-bonded, and tested in vacuum.

Temperatures were obtained from electrical resistance measurements [12]. The proportionality factor between temperature change and resistance change was measured statically by use of a hot stage. The peak resistance during the 100 Hz tests was found by acquiring digital current and voltage waveforms, fitting the waveforms separately with a discrete Fourier transform, and using the fitted voltage and current values at the peak [11]. The temperature range is the difference between the minimum and maximum temperature in the cycle, measured at the beginning of the tests. Measurements later in the tests showed that this range did not change significantly through practically all of the lifetime. For the lines tested under DC, the temperature range is the temperature increase above ambient produced by the current. Contrary to the usual practice in electromigration testing, in which substrate heating is used [3], the specimens were heated only by Joule heating. The lifetime is the interval between the time when full voltage was applied and the time of electrical failure.

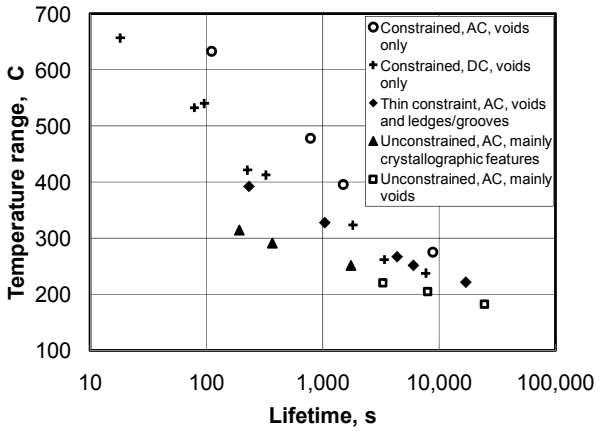

Figure 1. Lifetimes to electrical failure of various copper lines tested under high amplitude AC, with a set of DC data for comparison. The unconstrained lines are 5 μm wide; the others are 3 μm wide. The current density in all these lines is in the 10 to 15 MA/cm^2 range. SEM examination after failure showed voids in all the constrained lines and in the longest-lived unconstrained lines. The shorter-lived, unconstrained lines showed clearly crystallographic features that are believed to have resulted from dislocation slip processes.

In constrained lines, the SiO_2 dielectric was removed by etching in hydrofluoric acid to permit post-test examination in the SEM. The grain structure of the lines was imaged by use of orientation mapping by electron backscatter diffraction (EBSD) [13, 14].

The process of void formation in the constrained 3 μm wide lines was observed by acquisition of a series of optical images at intervals of 10 s to 30 s. The images were all processed to enhance the contrast between the voids and the copper line. Because the formation of the voids in the AC tests reached a clear saturation point, these images allowed an approximate measurement of the time interval to saturation.

In the thin constraint lines, the SiO_2 dielectric was removed prior to testing, leaving the SiN layer. After testing, the SiN was removed by reactive ion etching to allow SEM observation and EBSD analysis.

III. Results

Fig. 1 shows a plot of peak temperature against lifetime for the main specimen and test type variations that illustrates the typical behaviors. All specimen types show an approximately linear decrease of the logarithm of lifetime with temperature range. Constrained lines tested by AC have higher lifetimes than unconstrained lines, with the thin constraint lines having intermediate lifetimes. Constrained lines tested with DC have also intermediate lifetimes. The

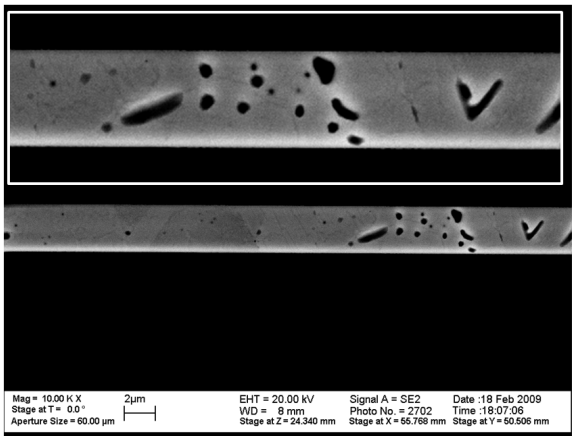

Figure 2. SEM micrograph of a constrained copper line after electrical testing under sinusoidal excitation and removal of the dielectric covering the specimen. This specimen was tested under sinusoidal AC at a peak current density of approximately 14 MA/cm^2; it self-heated to a temperature of 396 °C and had a lifetime of 1497 s. Note the round and elongated void types. Inset: Expanded display of the right-hand portion of the image.

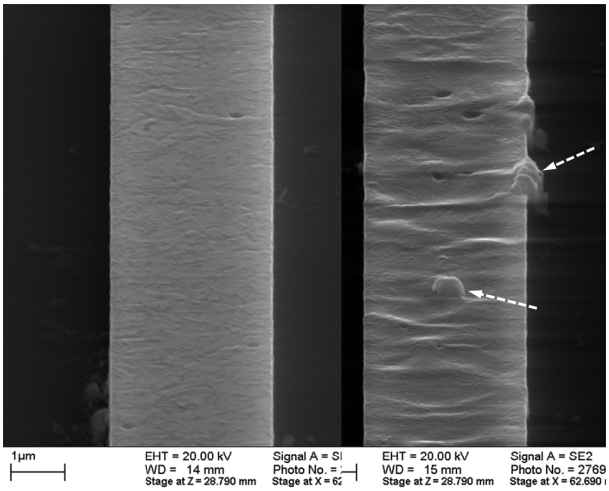

Figure 3. SEM micrograph of copper lines with thin constraint. Left: untested. Right: tested at a peak AC current density of 13 MA/cm^2. The cyclic temperature range was 262 °C and the lifetime was 2645 s. The prominences near the lower center and upper right in the tested line (arrows) are copper oxide. The bright horizontal contours indicate topographic features (ridges or grooves). Note the voids.

unconstrained lines stressed by AC excitation developed characteristic topologies, depending on the temperature range. The lines cycled with temperature ranges below about 250 °C had copious voids, as shown by SEM examination after the tests. Lines of the same type, tested under higher temperature ranges, showed few voids, but pronounced extrusions and intrusions associated with crystallographic features similar to those reported previously for unconstrained copper [5]. All the constrained lines showed voids, and none showed the crystallographic features.

Fig. 2 shows a SEM image of a constrained specimen tested under sinusoidal AC at a peak current density of approximately 14 MA/cm^2; it self-heated to a temperature of 396 °C and had a lifetime of 1497 s. Note the abundant

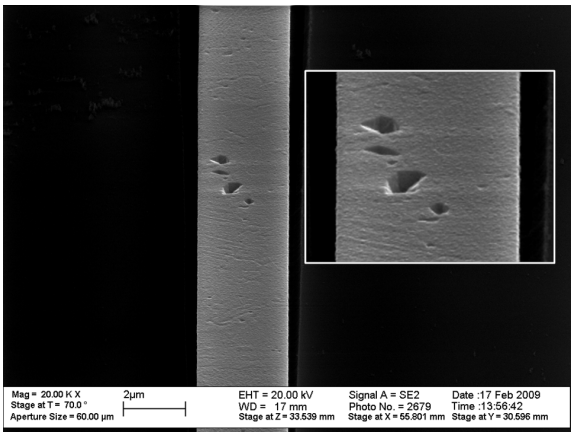

Figure 4. SEM micrograph of a constrained copper line, after electrical testing under DC and removal of the dielectric covering the specimen. It was tested under DC at a current density of approximately 15 MA/cm^2; it self-heated to a temperature of 413 °C above ambient and had a lifetime of 326 s. Inset: region of specimen with voids. Note the faceted void shapes.

voids. The specimen lines did have a very low density of tiny voids before testing, but at the magnification of the main image in Fig. 2, very few voids would have been seen before testing. The inset in this figure shows more detail of the voids. In observations made after the tests, voids were often associated with grain boundaries, but were seen in the middle of grains as well.

Fig. 3 shows images of two specimens with the thin constraint layer, one untested and one after testing at a peak AC current density of 13 MA/cm^2. The cyclic temperature range was 262 °C and the lifetime was 2645 s. Note the bright contours on the surface that indicate topographic features, ridges or grooves. The EBSD observations showed that these contours usually lie along grain boundaries.

Fig. 4 shows an SEM image of a constrained specimen tested under DC conditions at a current density of approximately 15 MA/cm^2; it self-heated to a temperature of 413 °C above ambient and had a lifetime of 326 s. Voids were seen in all the specimens tested under DC, but at lower density than in the AC tests. The inset in this figure is a magnified image of the region of the voids, showing their faceted shape. Faceting was more pronounced in the DC test than in the AC.

Fig. 5 shows orientation maps of five specimens: (a) as received; (b) after a 30 h anneal at 300 °C; (c) tested under DC (shown in Fig. 4); (d) annealed at 420 °C for 1 h; and (e) tested under AC (shown in Fig. 2).

Fig. 6 shows a time series of optical images acquired during an AC test of a single line that was fully constrained with SiO_2. The interval between images was 10 s. The images were processed to enhance contrast. The 10 images shown, extracted from the full sequence, show that the visible void content stabilizes at about 95 s after the start of the AC current. The lifetime of this line was 14294 s. The appearance of this line remained as shown in the last image in Fig. 6 for the vast majority of its lifetime.

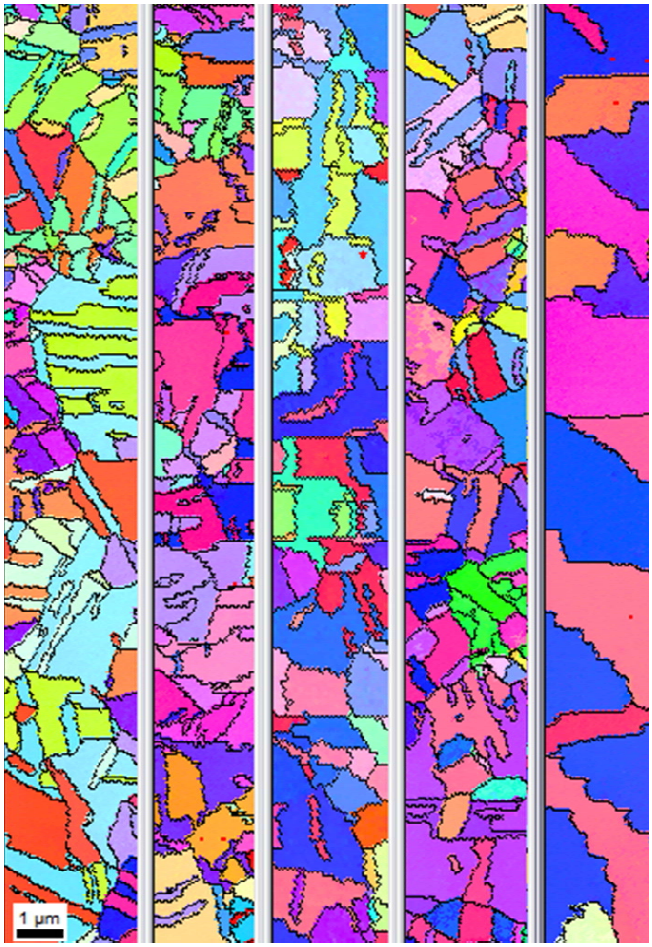

Figure 5. Orientation maps of portions of five damascene copper lines showing the effect of annealing and electrical testing on the grain structure. (a) Grain structure of an as received line. (b) Effect of a 30 h aneal in a vacuum furnace at 300 °C. (c) Orientation map of part of the line shown in Fig. 4 (DC test). (d) Orientation map of a line that received a treatment of 1 h in a vacuum furnace at 420 °C. (e) Orientation map of part of the line shown in Fig. 2 (AC test).

IV. Discussion

All lines in electronic interconnect structures are constrained by dielectric; therefore, the case of constrained lines is important. Fig. 1 shows that fully constrained lines can withstand higher temperature ranges, and therefore higher AC currents, than less constrained lines. The behavior under DC is shown for comparison. Voids are involved in the electrical failures of all types of copper lines studied here. Figs. 2 and 4 show the appearance of voids in constrained lines after failure, but not at the actual failure locations. The failure locations are always too severely damaged for post-test SEM analysis.

The unconstrained lines with shorter lifetimes that occur at the lower left of Fig. 1 show crystallographic features that have been associated with a competing failure mechanism, namely, AC fatigue involving dislocation motion [5]. The lines with thin constraint show both voids and surface contours that indicate grooves and ridges, Fig. 3. These surface features are less regular and less distinctive than those reported in connection with AC fatigue in copper and aluminum, but they could also be a result of dislocation motion. The lifetimes plotted in Fig. 1 for the lines with thin constraint may have been reduced by local failures of the coating that allowed some oxidation of the copper, as shown in Fig. 3.

Grain growth in aluminum resulting from cyclic heating with AC has been discussed in the literature [15]. Fig. 5 compares the as-received structure, Fig. 5a, to the structure after selected anneals and tests. This series of orientation maps shows that neither a 300 °C anneal for 30 h alone (Fig. 5b) nor testing under DC at about 413 °C above ambient (Fig. 5c) produced rapid grain growth in the present copper lines. A 420 °C temperature exposure for 1 h (Fig. 5d) produced slight grain growth. However, testing with AC for about 0.4 hr at a peak cyclic temperature of ambient plus 396 °C (Fig. 5e) produced noticeable grain growth. Grain growth was typical for the specimens tested under AC. The peak cyclic temperature reached in this specimen, about 420 °C, corresponds to a homologous temperature of 0.49.

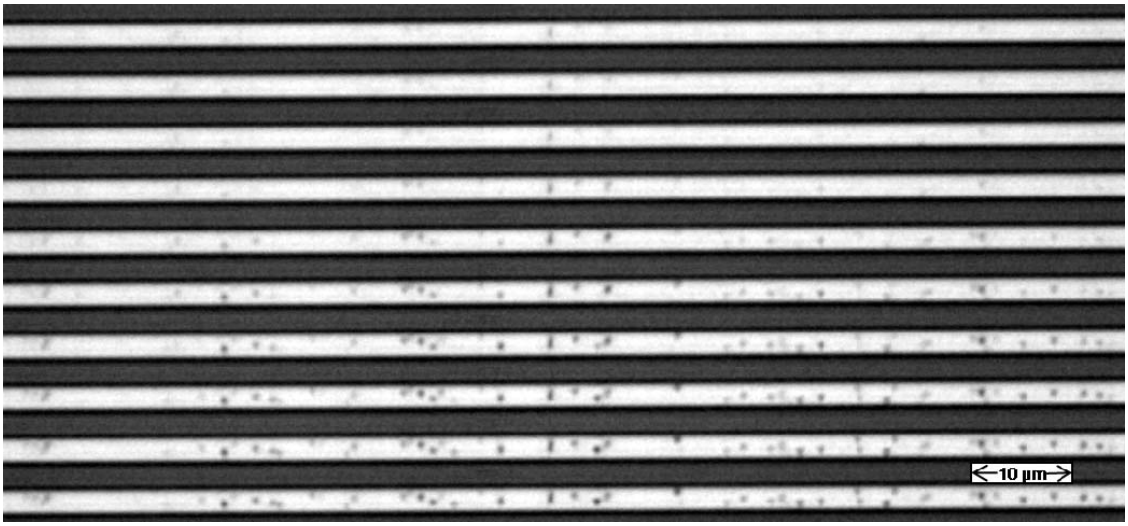

Figure 6. Montage of 10 images during an AC test at 100 Hz of a line fully constrained with SiO_2. The time series runs from top to bottom. The top image was acquired at 30 s into the test, and the acquisition interval was 10 s. The abrupt change from unvoided to voided is clearly shown.

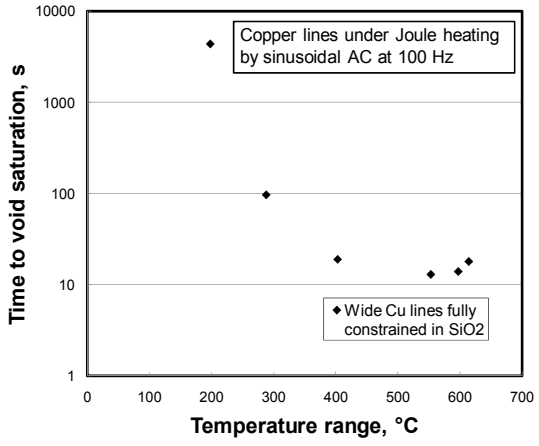

Figure 7. Time interval to void saturation for a series of AC tests of fully constrained wide copper lines tested at 100 Hz, plotted against the cyclic temperature range.

This is at the lower end of the range of annealing temperatures where grain growth would be expected.

The behavior of voids in copper conductors has been widely discussed in the literature for electromigration voiding [3] and stress-induced voiding [16]. Although the fundamental cause of the voids is the triaxial tension built into the structure [2], the factors that control void generation rates, sizes, size distributions, spatial distributions, mobility, and agglomeration are not well known. As part of the present series of tests, optical observations of the generation of voids by high amplitude AC were made. Fig. 6 shows images from such a test. Since the acquisition times of these images are separated by 10 s, the time to void saturation can be defined to within about ± 5 s for this and similar tests. Fig. 7 plots void generation times determined in this manner against cyclic temperature range for a series of tests at 100 Hz.

The data presented here have both practical and scientific implications. The practical implication is that accelerated tests of the current-carrying capacity of electrodeposited copper lines must account for the current type (AC or DC) and also for the line geometry (constrained or unconstrained). These tests show that current densities must be controlled well below 10 MA/cm^2 in actual structures, especially for devices within the severe (150 °C) environment of an engine. The critical failure mechanism for such lines under both DC and AC loads involves voids, so methods of predicting and controlling the generation of voids, and of stabilizing them to prevent them from growing too large, are of interest. The scientific implications of these data relate to the causes of void generation and of grain growth. The cyclic nature of the AC tests seems to accelerate both of these processes. A possible mechanism for the acceleration of both grain growth and void generation may be dislocation motion. The cyclic stresses and strains in these lines are believed to be sufficient to cause dislocation motion [17], and plastic deformation by dislocations was related to grain growth in aluminum lines tested under high amplitude AC [15]. The generation of vacancies and "cavitation" in metals by dislocation motion was studied decades ago, in observations of voids at grain boundaries [18], electrical resistance changes [19], and flow stress changes [20] in different pure metals.

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