Niobium silicide junction technology for superconducting digital electronics*

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***Abstract*—Digital superconducting electronics (SCE), which allows for very low power consumption and fast switching speeds, are a promising technology to deliver ultra-high performance computation. Currently, the preferred technology for junctions in SCE consists of Nb/AlOx/Nb tunnel junctions. Important developments have been achieved using this technology. Further improvements rely on increased speed and circuit density by means of fabricating higher critical current density (J_c) junctions and reducing circuit dimensions. As an alternative to these tunnel junctions, we propose a technology based on Nb/Nb$_x$Si$_{1-x}$/Nb junctions, with barriers near the metal-insulator transition. Tuning both the composition and thickness of the barrier allows for a large range of junction properties, this control of the barrier has demonstrated good targeting of properties and good reproducibility.**

I. INTRODUCTION

SUPERCONDUCTING digital electronics continues its development towards delivering ultra-fast and ultra-low power computing. Some of the most impressive achievements in this field include a T-flip–flop circuit operating up to 770 GHz [1] and a 4 kbit memory operated at 580 ps and 6.7 mW [2].

The earliest SCE circuits used junctions with lead and lead alloys, but these suffered from poor stability and their properties deteriorated after repeated thermal cycling. Presently, the preferred technology for high-speed superconductive digital circuits is based on Nb/AlO$_x$/Nb junctions with barriers on the order of 1 nm thick, developed in the early 1980's [3]. These junctions have proved to be stable, reproducible, and able to yield uniform devices.

Other attempts have been made to obtain suitable junctions for SCE, including SINIS (S=superconductor, I=insulator, N=normal metal), AlN replacing AlOx, high-resistivity SNS using TiNx, NbN$_x$ or TaN$_x$, HTS, etc. The only technology that has been partially competitive with Nb/AlOx/Nb, has been some NbN devices that replace Nb as the superconductor and allow operation near 10 K [4].

Recent efforts have attempted to make faster AlO$_x$–barrier tunnel junctions by increasing the current density J_c. The only way to achieve this is to reduce the barrier thickness to just a few monolayers of oxide and reduce the junction dimensions into the sub-micron regime. For such thin barriers, the transport mechanism begins to change, and appears to be dominated by metallic-like conduction, and J_c uniformity from junction to junction is much more difficult to achieve.

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We propose an alternative technology for SCE based on Nb/Nb$_x$Si$_{1-x}$/Nb junctions. By choosing x ≤ 0.05, the Nb-Si barriers can be reproducibly tuned between metallic and insulating behavior. A junction with a several-nanometer thick Nb-Si barrier would produce comparable electrical performance to that of high-Jc tunnel junctions, but has the potential for better reproducibility and uniformity.

For voltage standards it has been straightforward to change the characteristic frequency of junctions from 20 GHz to 70 GHz by choosing the appropriate composition and thickness. Excellent uniformity was demonstrated with large circuits of ~70000 nearly identical junctions [5]. Similarly, much faster junctions with characteristic frequencies above 500 GHz have been fabricated [6].

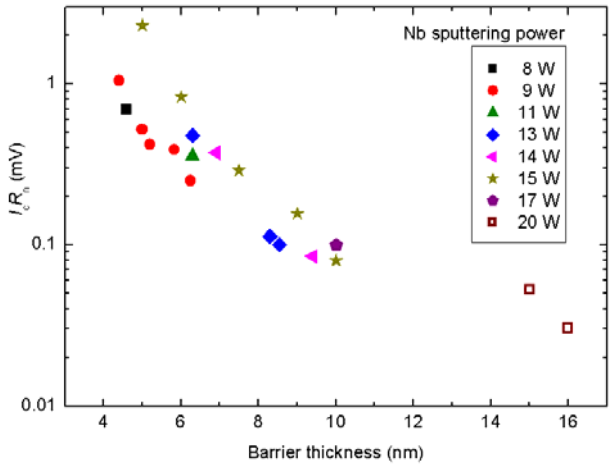

Fig. 1. I_cR_n vs barrier thickness for Nb/Nb$_x$Si$_{1-x}$/Nb junctions with different Nb content in the barrier determined by the power of the Nb sputtering gun. The Si sputtering gun power was set at 200 W for all junctions in the figure.

II. AMORPHOUS NB-SI-BARRIER JUNCTIONS

NIST has been developing Nb/Nb$_x$Si$_{1-x}$/Nb junctions to replace previously successful junction technologies for voltage standards, namely PdAu and MoSi$_2$ SNS junctions. Typically, these junctions have a low normal resistance R_n and, as a consequence, low values of I_cR_n (if I_c, the critical current, is to be kept within practical limits). This makes them unsuitable for high-speed electronics. However, one of the advantages of our co-sputtering deposition system is the ability to control both the composition of the barrier along with its thickness [7]. The relative power of the Nb and Si sputtering guns determines composition, and the deposition period determines thickness. This allows a continuous spectrum of barrier properties from low resistance, Nb-rich barriers, to insulating barriers of pure silicon. A wide range of junction parameters, such as J_c, capacitance (C), and R_n can be reliably selected. Of particular

interest are junctions with more insulating and thinner barriers, which have I_cR_n products greater than 1 mV and J_c greater than 60 kA/cm^2. Fig. 1 shows a variety of I_cR_n values for junctions with different barrier deposition conditions.

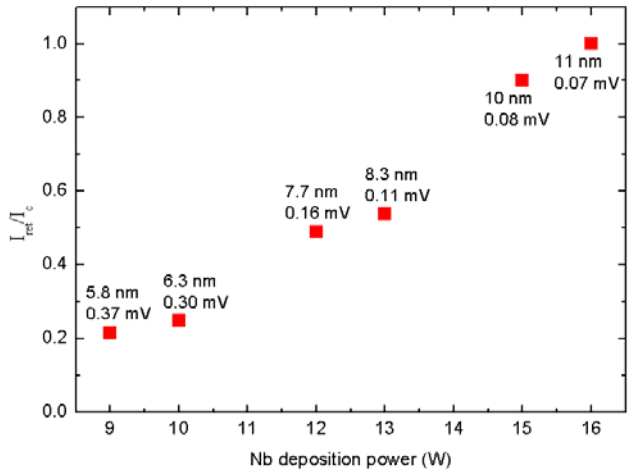

Fig. 2. Hysteresis (I_{ret}/I_c, where I_{ret} is the return current) vs barrier Nb content as determined by deposition power. All junctions have a targeted J_c between 4 and 5 kA/cm^2. Barrier thickness and I_cR_n product are indicated for each point.

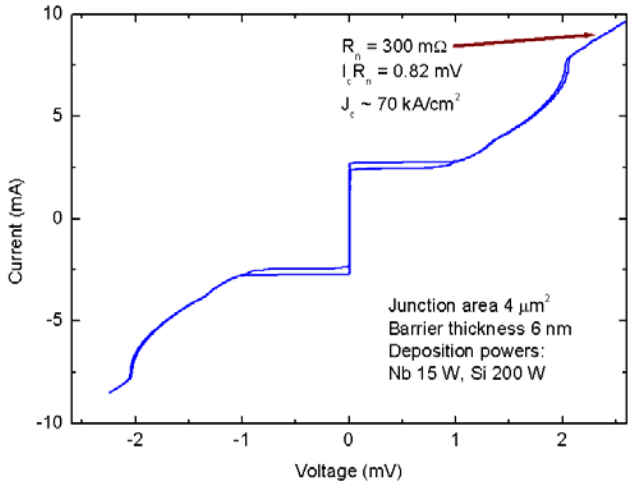

Fig. 3. Slightly hysteretic current-voltage characteristic of a high J_c junction.

A valuable characteristic of our junctions is their robustness and ability to withstand fabrication processing: SINIS junctions that have dual AlO_x insulating layers are detrimentally affected by plasma processing, dramatically lowering device yield, which is not a problem for Nb/Nb_xSi_{1-x}/Nb junctions under comparable process conditions [5]. These junctions are more robust partially because of the thicker barriers.

Another important feature is the good reproducibility of junction properties. For our junctions this can be seen in the dependence of J_c on barrier composition and thickness, as demonstrated in [8]. For a fixed barrier composition, J_c has a nearly exponential dependence on the barrier thickness.

Independent control of composition and thickness allows simultaneous targeting of J_c and resistance, which determines the damping. As an example, Fig. 2 shows a set of junctions with the same targeted J_c, between 4 kA/cm^2 and 5 kA/cm^2, but with different hysteresis, and I_cR_n values. As the concentration of Nb decreases, the junctions become more resistive and also more hysteretic, for a fixed J_c.

High values of I_cR_n can be achieved with a variety of thickness and composition combinations. More metallic barriers produce large values of J_c, which require smaller lateral fabrication dimensions to maintain practical I_c values. These junctions are ideally suited for SCE logic, because they are intrinsically critically damped, as shown in Fig. 2. Without the need for shunt resistors, they avoid the parasitic inductances arising from shunts and can achieve much higher circuit density. More resistive barriers will allow larger lateral junction dimensions, but the reduced damping will increase their hysteresis. More hysteretic junctions are suitable for latching logic and input/output circuits, such as Suzuki stacks [9]. Electrical properties of junction are shown in Fig. 4. Another feature in this case is the potential for higher-density vertical stacks of junctions, which have already been demonstrated [10].

Notice in Fig. 4 that the sub-gap R (above I_c) and the corresponding I_cR is larger than R_n and I_cR_n. We think the sub-gap R better represents the junction dynamics, because it is nearer the operating point in a digital circuit. It also suggests faster operation than that given by the I_cR_n value [11].

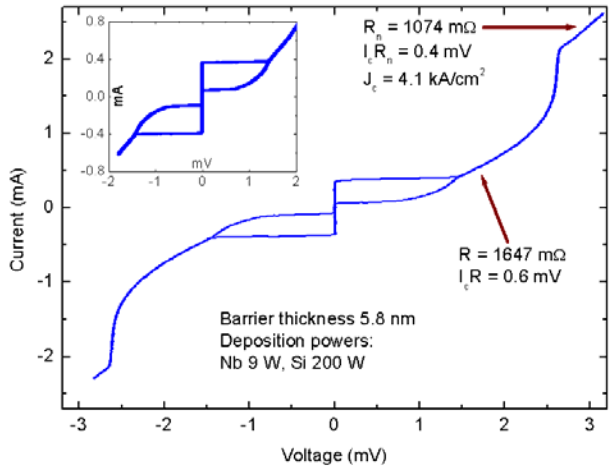

Fig. 4. Current-voltage characteristic of two junctions in parallel. The more resistive barriers produce larger hysteresis compared to the junction in Fig. 2.

III. Conclusion

Nb/Nb_xSi_{1-x}/Nb junctions are a potential alternative to the prevalent Nb/AlOx/Nb junctions for digital SCE applications. A fabrication process exists that has demonstrated reproducible and uniform junctions with a great variety of properties. Junctions with I_cR_n values greater than a millivolt and with little hysteresis are promising for applications in SCE logic, while more hysteretic junctions could be applied in latching logic and outputs circuits. Near-future plans to fabricate digital circuits with these junctions will test their potential.

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