Versatile co-sputtered $Nb/Nb_xSi_{1-x}/Nb$ Josephson junctions for Josephson voltage standards and high-speed superconducting digital electronics*

David Olaya, Paul D. Dresselhaus, and Samuel P. Benz

Abstract—**Josephson junctions that use co-sputtered amorphous Nb-Si barriers can be made with a wide variety of electrical properties. Critical current density (J_c), capacitance (C), and normal resistance (R_n) can be reliably selected within wide ranges by choosing both the barrier thickness and its Nb concentration. Metallic barriers near the metal-insulator transition are ideal for Josephson voltage standards, as they have relatively high I_cR_n products (where I_c is the critical current) and are non hysteretic and highly reproducible. More insulating junctions, with thinner barriers, have I_cR_n products greater than 1 mV, and J_c values up to ~60 kA/cm^2 may be useful for superconductive digital electronics. Recent improvements to our deposition system have allowed us to obtain higher values of J_c and better uniformity across the wafer.**

I. INTRODUCTION

JOSEPHSON junctions made with co-sputtered Nb-Si barriers have already been shown to have excellent uniformity and reproducibility in Josephson voltage systems in which tens of thousands of junctions all have sufficiently similar properties to each other as to allow 10 V to be obtained from the addition of their first constant voltage step under microwave bias. These junctions are more robust than SINIS (S=superconductor, I=insulator, N=normal metal) junctions that have AlO_x for the insulator and which have also been used in voltage standard applications. SINIS junctions also seem to be affected by plasma processing, giving a low yield of working devices [1]. Junctions with Nb-Si barriers, on the other hand, are more robust due, in part, to the increased thickness of the barriers, which is of the order of several nanometers.

High-J_c Nb/AlOx/Nb junctions, with barriers only a few monolayers thick, are presently the preferred technology for high-speed superconductive digital circuits. In comparison with these junctions, the relatively thicker barriers of Nb-Si junctions have the potential for better reproducibility and uniformity.

II. JUNCTION ELECTRICAL PROPERTIES

The Nb-Si-barrier junctions are fabricated in a multi-gun sputter system capable of co-sputtering; details of the fabrication process can be found in [2]. The relative power of the Nb and Si guns determines the composition, and the deposition time determines the thickness. Together, these deposition parameters determine the junction electrical characteristics, such as I_c, R_n, and C.

The two controllable barrier parameters, composition and thickness, enable a wide range of electrical properties. The proven reproducibility of these properties can be seen in the dependence of J_c on barrier composition and thickness, as shown in [3]. For a given barrier composition, the value of J_c has a nearly exponential dependence on the barrier thickness.

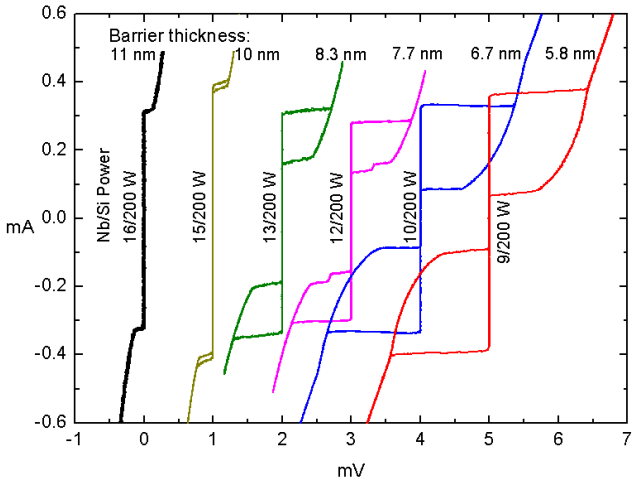

Fig. 1. Current-voltage characteristic for six pairs of junctions designed to have similar J_c but different composition and thickness. Curves are displaced on the voltage axis for clarity. Thinner barriers with lower Nb content display higher characteristic voltage I_cR_n and more hysteresis.

The simultaneous but independent control of these parameters allows us to obtain junctions with a chosen J_c but with different resistance and capacitance, so that they have different characteristic frequencies and a different amount of damping, which produces different magnitudes of hysteresis in the current-voltage curves (*IVC*). Fig. 1 shows a set of six *IVC* for pairs of parallel junctions with dimensions of 2.5 μm x 2.5 μm. The junction pairs have different composition and thicknesses, but are all designed to have the same value of J_c. As the concentration of Nb decreases, the junctions become more resistive and also more hysteretic, because the less metallic barriers become more resistive. The preferred properties for a specific application can be obtained through the correct choice of thickness and composition. For high-speed

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D. Olaya, P. D. Dresselhaus, and S. P. Benz are with the National Institute of Standards and Technology, Boulder, CO 80305 USA (e-mail: david.olaya@nist.gov).

digital electronics, for example, high values of I_cR_n can be achieved with a variety of combinations of thickness and composition. More metallic barriers will produce large values of J_c, which require smaller lateral fabrication dimensions to maintain I_c values within practical limits. More resistive barriers will allow junctions to have larger lateral dimensions, but the reduced damping will increase *IVC* hysteresis.

TABLE I GROWTH CONDITIONS AND PROPERTIES OF NB/NB-SI/NB JUNCTIONS

Power Nb/Si (W)	Thickness (nm)	J_c (kA/cm^2)	C (pF)	I_c/I_{ret}	ε
16/200	11	3.9	2.1	1.00	658
15/200	10	4.1	2.1	1.11	593
14/200	9.4	2.9	1.0	1.13	275
13/200	8.3	3.0	1.3	1.86	309
13/200	8.5	2	0.9	1.52	215
12/200	7.7	3.7	1.0	2.04	213
10/200	6.7	2.6	0.6	4.07	121
10/200	6.3	3.9	0.6	4.02	108
9/200	6.3	1.6	0.5	4.45	85
9/200	5.8	3.5	0.6	4.39	91
9/200	5.8	4.1	0.7	4.64	114
9/200	5.8	5.1	0.7	3.75	117
9/200	5.8	6.4	0.6	3.32	100
9/200	5.8	7.4	0.7	2.28	110

It has been found that junctions of low Nb content are more susceptible to residual impurity gases in the chamber during deposition. Voltage standard circuits operating at 75 GHz were found to have large J_c non uniformity across the wafer [4]. The origin of the non uniformity was found to be outgassing from the cooling graphite foil (used to heat-sink the wafer during deposition) and possibly also the platen in back of the wafer. The effect was more pronounced in circuits nearest to the flat of the wafer, where there was a small opening in the wafer holder. A new holder plate with no gap improved the uniformity. Experiments on thicker films made of only the barrier material showed considerable improvement in resistivity uniformity after a new holder plate with no gap around the wafer flat was installed. Before this change, a film deposited with 8/200 W (Nb/Si power) had a mean resistivity of 7.4 mΩ•cm with a standard deviation of 5.6 mΩ•cm. After removing the gap and reducing the residual gases, a similar wafer had a lower average resistivity of 3 mΩ•cm with a smaller standard deviation of 0.4 mΩ•cm. A further increase in J_c and decrease of barrier resistivity was obtained by replacing the graphite foil with a solid Al metal disc for wafer cooling. It is not clear what residual gas is responsible for the depressed value of J_c. Preliminary studies show that it is also possible that residual water vapor may be responsible for suppression of the critical current density.

Table I shows the growth conditions and measured properties, J_c, C, amount of hysteresis (I_c divided by the return current, I_{ret}), and dielectric constant (ε) of the barrier for different wafers. Capacitances were inferred by measuring voltage resonance steps in the *IVC* of SQUIDs in which flux was coupled by adjusting the current in a directly coupled wire, as described in [5]. The values of C and ε decrease as the Nb content of the barrier decreases. Fig. 2 shows these trends for the same group of wafers with similar J_c shown in Fig. 1.

As expected, the value of J_c increases as the Nb content increases or the barrier thickness decreases. J_c also increases when the impurities affecting the barrier are reduced. The last five entries of Table I show samples with the same composition and thickness; they all have similar values of C and ε, but those near the bottom, corresponding to improvements in wafer mounting in the deposition chamber, have higher J_c and, at the same time, less hysteresis. Future work will demonstrate the reproducibility of these deposition conditions.

III. CONCLUSION

The ability to control the thickness and composition of the barrier allows us to make Nb/Nb$_x$Si$_{1-x}$/Nb junctions with properties suitable for applications from voltage standards to superconducting electronics. Improvements in the fabrication process added to their ease of fabrication, reproducibility and stability and suggest that these junctions are promising for application in high-speed digital electronics.

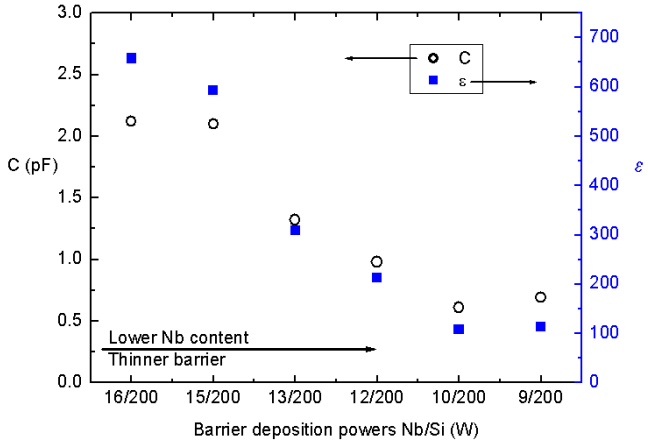

Fig. 2. Capacitance, C and dielectric constant, ε of the barrier in Nb/Nb$_x$Si$_{1-x}$/Nb junctions. Note that the barrier thickness is decreased together with Nb concentration to maintain J_c constant. This group of junctions is identical to those plotted in Fig. 1.

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