

# Arrays with Double-stacked $\text{Nb}_x\text{Si}_{1-x}$ -Barrier Junctions for Use in Programmable Josephson Voltage Standards driven at 70 GHz\*

F. Mueller, R. Behr, R. Wendisch, J. Kohlmann, D. Olaya, P. D. Dresselhaus, and S. P. Benz, *Senior Member, IEEE*

**Abstract**—Double-stacked Nb junctions with  $\text{Nb}_x\text{Si}_{1-x}$  barriers were inserted into previously successfully tested 1 V and 10 V designs for Programmable Josephson voltage standards (PJVSs) with bias frequency near 70 GHz. Despite non-optimum targeting of the junction electrical parameters, comparison of the two circuits allows evaluation and optimization of the 10 V circuit design.

## I. INTRODUCTION

TODAY the most advanced AC voltage metrology for the low frequency region ( $f < 1$  kHz) is based on the Programmable Josephson Voltage Standard (PJVS) [1]. According to the fundamental equation for Josephson voltage metrology, the array output voltage is

$$U(t) = nN(t)f/K_{J-90}. \quad (1)$$

The PJVS systems exploit this equation by rapidly programming the voltage  $U(t)$  by changing the junction number  $N$  through biasing different sub-arrays with different numbers of junctions.  $K_{J-90}$  is the Josephson constant ( $K_{J-90} = 483\,597.9$  GHz/V),  $n$  denotes the order of Shapiro steps (typically using the three voltage states  $n=0$ , and  $\pm 1$ ) and  $f$  the microwave frequency.

For nearly a decade PTB has used the SINIS junction technology (S=superconductor, I=insulator, N=normal metal) to realize large arrays ( $N$  up to nearly 70 000) for PJVS systems [2]. As the  $I_cR_n$  product of this junction type can easily be tuned, the PJVSs can be driven at 70 GHz, a frequency commonly used by the voltage-metrology community. However, due mainly to plasma-induced damage during the complex SINIS fabrication process, the yield is quite low (about 5 %) and only a few 10 V circuits are available [3].

In contrast, the SNS junction technology is much simpler and more robust, because only the thickness of a given N-layer

determines both  $I_cR_n$  and the current density. This technology's limitation for low-speed applications, due to the low  $I_cR_n$  of classical SNS junctions, has been overcome by recent progress with silicide-materials near the metal-insulator transition. NIST has demonstrated that Nb junctions with amorphous  $\text{Nb}_x\text{Si}_{1-x}$  barriers are a potential technology for high-speed superconductive electronics [4]. By changing the Nb content of the barrier the  $I_cR_n$  can be tuned from 10  $\mu\text{V}$  ( $x \sim 0.12$ ) to nearly 1 mV ( $x \sim 0.05$ ). Based on these junctions and an existing 70 GHz microwave design, PTB and NIST, in close cooperation, have successfully realized a 10 V PJVS circuit with about 70 000 Josephson junctions [3]. These arrays are suitable for metrological AC applications and can be used as drop-in replacements for SINIS arrays in existing 1 V and 10 V systems operated at 70 GHz. 10 V PJVS circuits with silicide-barrier junctions have better yield and larger current margins compared to circuits with SINIS junctions.

In this paper, we describe our efforts to implement vertically stacked silicide-barrier junctions in the same 70 GHz circuit designs that were already demonstrated with non-stacked junctions. The use of stacked junctions provides a practical way to increase the output voltage and enables optimization of the 10 V design.

## II. FABRICATION PROCESS

The Nb-( $\text{Nb}_x\text{Si}_{1-x}$ -Nb)<sub>2</sub> pentalayers with two barriers were grown on oxidized Si wafers at NIST. The NbSi is deposited by co-sputtering from a Nb and a Si sputter target. The middle Nb electrode is 50 nm thick. Other fabrication details are described in [3]. The patterning of the pentalayers was performed at PTB by means of e-beam lithography for all relevant circuit levels [3]. To ensure anisotropic etching of the two vertically stacked junctions, ICP-etching (Inductive Coupled Plasma) with  $\text{SF}_6$  was used.

## III. RESULTS AND DISCUSSION

The presented results are preliminary and obtained from a pentalayer whose junctions have an  $I_cR_n$  product 12 % higher than the desired target characteristic voltage of 145  $\mu\text{V}$ . Nevertheless, results of the fabricated circuits allow a number of conclusions. Fig. 1 shows a typical current-voltage curve (IVC) for the largest array segment (half 10 V array) with 34 816 double-stacked junctions of a 10 V circuit. The IVC with microwaves (black line) demonstrates current margins for

Manuscript received May 8, 2009. The research within this EURAMET joint research project leading to these results has received in part funding from the European Community's Seventh Framework Programme, ERANET Plus, under Grant Agreement No. 217257

F. Mueller, R. Behr, R. Wendisch, and J. Kohlmann are with the Physikalisch-Technische Bundesanstalt (PTB), 38116 Braunschweig, Germany (e-mail: [franz.mueller@ptb.de](mailto:franz.mueller@ptb.de))

D. Olaya, P. D. Dresselhaus, and S. P. Benz are with the National Institute of Standard and Technology (NIST), Boulder, CO 80305 USA. (e-mail: [samuel.benz@nist.gov](mailto:samuel.benz@nist.gov))

\*US Government work not subject to U.S. copyright.

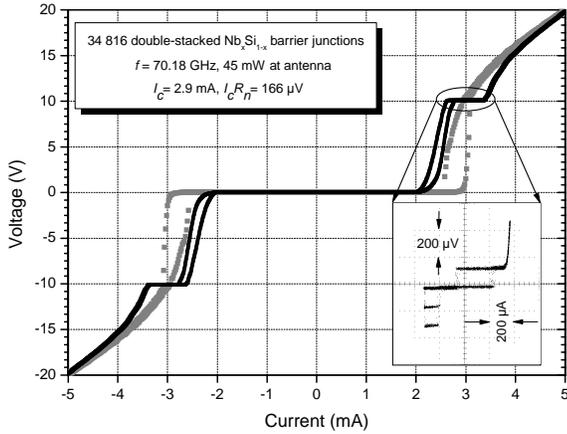


Fig. 1 IVC of the largest segment of a 10 V circuit design with 34 816 double-stacked silicide-barrier junctions arranged in 64 striplines, grey points: without microwaves, black line: with microwaves. The inset shows the 10 V steps with high resolution.

the 10 V step of approximately 0.5 mA. Probably due to the non-optimum  $I_c R_n$ , the large hysteresis seen in the IVC without microwaves (grey points) decreases the useful current range of the step at 10 V, because multiple metastable steps overlap the same current range (inset picture). However, previous experiments with non-stacked silicide-barrier junctions demonstrated that the hysteresis can be suppressed by applying sufficiently large microwave power. Circuits of the same design, but using 69 632 non-stacked junctions having similar electrical parameters, exhibit perfect 10 V steps with current margins larger than 1 mA if they are driven by approximately the same microwave power [3]. Therefore, we hypothesize that the double-stacked 10 V circuits with 139 264 junctions arranged in 128 microstriplines suffer from excessive microwave attenuation that prevents uniform microwave power from being applied to all the junctions within the stripline. The number of junctions embedded in each of the 64 striplines forming the largest array segment (Fig. 1) varies between 1 156 and 1 164. This number seems to exceed the admissible limit based on a compromise between damping of a passive stripline ( $I_{dc} = 0$ ) and self-oscillation coupling effects occurring in active striplines ( $I_{dc} > I_c$ ) [5], [6].

From the same pentalaer wafer, we also fabricated 1 V circuits with double-stacked junctions. In contrast to the 10 V arrays, the design of the 1 V chips is very homogenous, because each of the 64 parallel striplines contains only 128 double-stacked junctions. All of these 1 V circuit designs worked perfectly and produced twice the output voltage (2 V). Under microwave irradiation they displayed a doubled maximum voltage of approximately 2.37 V at 70 GHz, and the current margins were larger than 1.2 mA. In contrast to the 10 V circuits, the maximum available microwave power (approximately 45 mW at the antenna) is just able to suppress the hysteresis, so that overlapping metastable Shapiro steps were not observed. However, while separately investigating each array segment (bit), we detected a specific design difficulty of our circuits based on “low-impedance” striplines with embedded double-stacked junctions. Fig. 2 presents the IVCs of all segments under microwave irradiation at 70 GHz.

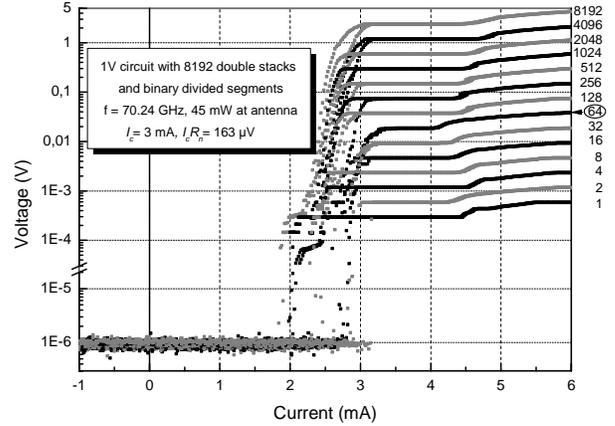


Fig. 2 IVCs of a complete 1 V circuit design and of all segments under microwave irradiation. The number of double stacks is indicated to the right of the corresponding curve and increases from bottom to top in a binary sequence.

The flat portion of the first Shapiro steps exceeds current margins of more than 1 mA except the segment with 64 stacks displaying a flat portion of only 0.5 mA. The reason for this is the undesirable microwave attenuation by the 128 unbiased junctions lying in front of this sub-array. This effect is observed in one of the outer striplines (a concern also for the 10 V circuits), and is also well known from SINIS arrays [2], [6].

#### IV. CONCLUSIONS

We have successfully demonstrated double-stacked silicide-barrier junctions for the use in PJVS circuits. The present 70 GHz designs for 1 V and 10 V circuits had previously proven their usefulness when fabricated with non-stacked junctions. In this paper, we describe how these designs were tested with double-stacked junctions that could be useful for higher voltage applications. The results showed that microwave power reaching the smallest array segments (bits 0 to 6) depended on the microwave attenuation of the unbiased segments in front of them. With the present 10 V design, we are optimistic about realizing the goal of 20 V with more microwave power and with optimized junction parameters.

#### REFERENCES

- [1] C. A. Hamilton, C.J. Burroughs, and R. L. Kautz, “Josephson D/A Converter with Fundamental Accuracy,” *IEEE Trans. Instrum. Meas.*, vol. 44, pp. 223-225, Apr. 1995.
- [2] F. Mueller, R. Behr, L. Palafox, J. Kohlmann, R. Wendisch, and I. Krasnopolin, “Improved 10 V SINIS Series Arrays for Applications in AC Voltage Metrology,” *IEEE Trans. Appl. Supercond.*, vol. 17, pp. 649-652, June 2007.
- [3] F. Mueller, R. Behr, T. Weimann, L. Palafox, D. Olaya, P. D. Dresselhaus, and S. P. Benz, “1V and 10V SNS Programmable Voltage Standards for 70 GHz,” to appear in *IEEE Trans. Appl. Supercond.*, 2009.
- [4] B. Baek, P. D. Dresselhaus, and S. P. Benz, “Co-Sputtered Amorphous Nb<sub>2</sub>Si<sub>1-x</sub> Barriers for Josephson-Junction Circuits,” *IEEE Trans. Appl. Supercond.*, vol. 16, pp. 1966-1970, Dec. 2006.
- [5] R. L. Kautz, “Design and operation of series array Josephson voltage standards,” *Metrologie at the frontier of Physics and Technology*, edited by L. Crovini and T. J. Quinn, (North-Holland, Amsterdam), pp. 259-296, 1992.
- [6] R. Behr, H. Schulze, F. Müller, J. Kohlmann, I. Krasnopolin, and J. Niemeyer, “Microwave coupling of SINIS Junctions in a Programmable Josephson Voltage Standard,” *Proc. ISEC’99, Ext. Abstr.*, pp. 128-130, June 1999.