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Atomic layer deposition enabled interconnect technology for vertical nanowire arrays

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ABSTRACT

We have demonstrated an atomic layer deposition (ALD) enabled interconnect technology for vertical, *c*-axis oriented gallium nitride (GaN) nanowire (NW, 5–10 μm in length, 80–200 nm in diameter) arrays encapsulated by benzocyclobutene (BCB). The nano-scaled ALD multilayer is essential to provide conformal co-axial dielectric (ALD-alumina)/conductor (ALD-tungsten) coverage and precise thickness control for nanowire metallization. Furthermore, we have successfully developed a fabrication process to locally remove and connect tungsten (W) interconnect on NWs. Cross-sectional image taken in a focused ion beam (FIB) tool confirms the conformality of ALD interconnects. Photoluminescence (PL) wavelengths of the nanowires array can be tuned dynamically by changing the input current supplied to ALD-tungsten interconnect which heats nanowires. Such an experiment also demonstrated the quality of interconnect. This interconnect technology can be applied to various vertical nanowire-based devices, such as nanowire light emitting diodes, nanowire-based field effect transistors, resonators, batteries or biomedical applications.

1. Introduction

Low dimensional materials such as nanowires (NWs) have attracted considerable research attention and interest due to their unique electrical, optical, magnetic properties [1]. They are promising material candidates as fundamental building blocks for future electronic [2,3], optoelectronic [4,5], energy [6], sensor [7] and biomedical [8] applications. Usually NW-based devices are constructed as horizontal configurations. NWs are taken from as-grown substrate, and then assembled, interconnected and tested [9,10]. Vertical nanowire array devices, compared to horizontal NW configurations, are of great importance for achieving ultrahigh integration density at a device level without the need of additional assembly and rearrangement processes. For example, vertical nanowire arrays are the best configuration for solid state supercapacitors [11,12], lithium ion batteries [13] and NW light emitting diodes (LEDs) [14]. These applications require large surface-to-volume ratio of vertical NWs for enhanced performance and potentially higher efficiency.

Studies have been made on interconnect and integration of vertical NWs. Electrical interconnect to the top of NWs has been demonstrated by using electrostatic attachment of gold nanoparticles onto the tips of NWs [15]. Interconnect is formed from the bottom electrode through NWs to the top gold nanoparticle film. Vertical integration of NWs has been developed by using a sequence of fabrication process from material filling, mechanical polishing to the formation of top and bottom electrical interconnects [16]. Usually, nanowires are parts of interconnects, and electrodes are formed on top and bottom of NWs. For vertical NW-based LEDs, field effect transistors (FETs) or batteries, device performance could be significantly enhanced through the utilization of the large surface-to-volume ratio of vertical NWs while coated with high-quality electrical and dielectric interconnects. However, it is always a challenge to interconnect these vertical/as-grown nanowires because of their small diameters, extremely high aspect ratios, and random distributions on the substrate. In addition, for certain applications, to locally remove and connect interconnects on vertical NWs is another challenge.

Our study presents a new interconnect technology for vertical NW arrays with a novel nano-scaled conductor/dielectric

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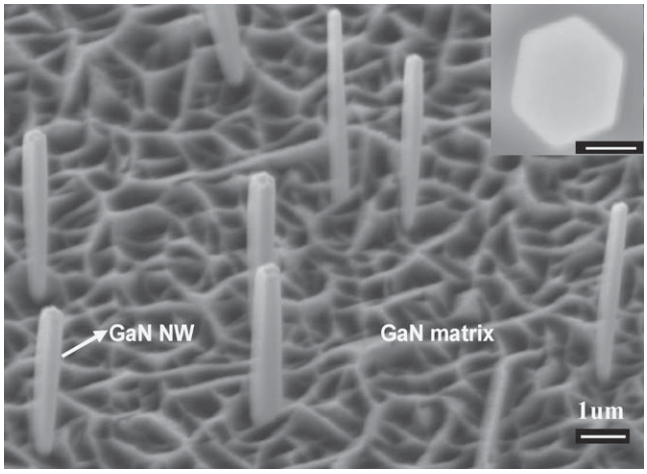

Fig. 1. Field-emission scanning microscopy (FESEM) image of *c*-axis oriented GaN nanowires. Nanowires, ranging from 5 to 10 μm in length and 80–200 nm in diameter, were grown on silicon (1 1 1) by nitrogen plasma enhanced MBE [17,18]. The faceted GaN matrix is visible in the image. (Inset) Top view of single NW (scale bar: 100 nm).

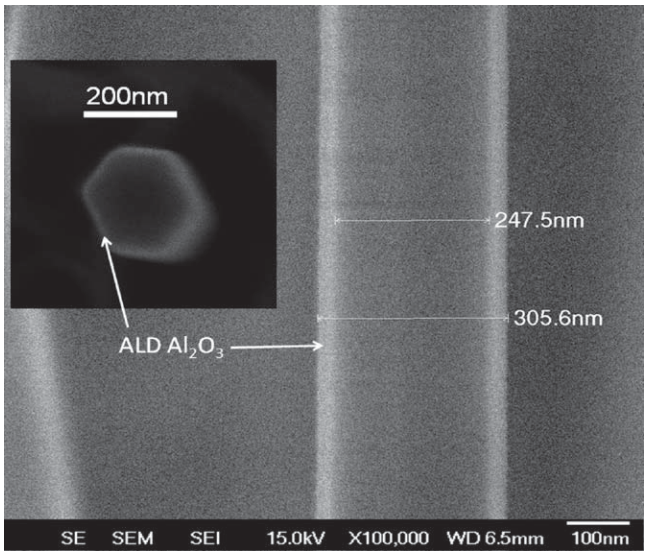

Fig. 2. Cross-sectional and top view (inset) SEM images of ALD-Al_2O_3 layer (30 nm, shell) on GaN NW (core). Conformal Al_2O_3 (30 nm) was deposited on the surface of NWs as a dielectric layer using atomic layer deposition. Scale bar: 100 nm.

multilayer fabricated using atomic layer deposition (ALD). Benzocyclobutene (BCB) is employed as filling material to encapsulate NWs. We have also developed a fabrication process to locally remove and connect tungsten interconnect on NWs. Using local interconnect process, we can dynamically tune the wavelength of GaN NWs by heating the NWs via input current supplied to ALD-tungsten interconnect and verify the connection of interconnect.

2. Nanowires interconnected with tips covered

Fig. 1 shows the *c*-axis oriented GaN NWs that were grown on Si (1 1 1) in an entirely catalyst free fashion using nitrogen plasma enhanced molecular beam epitaxy (MBE). The detailed synthesis technique could be found in references [17,18]. These wires are defect-free with a typical diameter of 150 nm. The nanowires used in this study were roughly 8 μm in length.

We then employed ALD processes to interconnect GaN NWs. ALD is a low temperature (for example, 120 °C for Al_2O_3 and W film growth) thin film growth technique allowing atomic-scale thickness control. ALD utilizes a binary reaction sequence of self-limiting chemical reactions between gas phase precursor molecules and a solid surface [19,20]. Films deposited by ALD are extremely smooth, pinhole-free and conformal to the underlying substrate surface. This conformality enables successful uniform coating of the entire nanowire device. Furthermore, ALD is a low temperature process enabling deposition on thermally sensitive materials.

ALD-Al_2O_3 (30 nm) and ALD-W (40 nm) were sequentially deposited on the surface of NWs which serves as a dielectric layer and an electrical connection layer, respectively. The conformality of ALD-Al_2O_3 coating was verified by field emission scanning electron microscopy (FESEM) as shown in Fig. 2, from side view and top view (inset). Fig. 3 shows the FESEM images of tungsten layers (deposited by ALD and sputtering) and placed on top of the ALD-Al_2O_3 layer. Apparently, ALD deposition provides a more conformal tungsten coating (Fig. 3a) compared to sputtered W (Fig. 3b). A polymer encapsulation process for the interconnected vertical NW devices has also been developed. This encapsulation processing was needed to finalize the interconnection of the devices coated with the ALD conductor/dielectric multilayer and also provide a robust mechanical support. In this study, we selected BCB as the filling material to encapsulate vertical NWs. BCB has been widely adopted in a variety of electronic applications, including silicon and compound semiconductor passivation, interlayer dielectric, flat panel display, IC packaging, integrated passives, MEMS, wafer bonding and 3D integration, and optoelectronic components due to the favorable material properties of BCB such as low dielectric constant (2.65) and low dissipation factor (0.0008) [21]. Several droplets of BCB were dripped on the NWs chip, and then soft baked at 90 °C for 4 min, exposed to UV, and then hard baked at 250 °C for 1 h (Fig. 4a). To expose the tips of NWs, mechanical polishing was first employed to reduce the thickness of BCB and then plasma reactive ion etching (RIE) was used for selective BCB etching. Fig. 4b shows the exposed NW tips. However, as shown in Fig. 4b and 4c, polishing process could result in NW tip damage, and also result in residual voids and cavities between the BCB and the NWs. Such cavities may electrically isolate the NW tip from the top conducting surface.

To eliminate these cavities, a second ALD-W (30 nm) coating was introduced to assure a conformal conductor coating that would cover every NW tip even down and into the cavities. This ALD conductor coating is followed by a thick top W electrode which is deposited by sputtering with a thickness of 170 nm. As a result, a continuous electrical interconnection from top tips of NWs through the surface of NWs to the bottom substrate is formed. We note that the top electrode can be patterned to interconnect a specific number of NWs. This ALD-enabled interconnection scheme is of critical importance for the development of core-sleeve vertically aligned NW LEDs. In other potential applications of nanowire structures, such as supercapacitors, the ALD-alumina dielectric layer may also play an important role. Fig. 5 reveals the detail of the layer-by-layer structure using focused-ion-beam (FIB) cross-sectional cutting. The conformal ALD-Al_2O_3/ALD-W layers on the NWs, and the second ALD-W layer to fill the voids/cavities described earlier are shown in the figure.

3. Nanowires interconnected with tips exposed

For vertical NW-based LEDs or lasers, tip regions of NWs are the passages of light output. Light output could be blocked by the design of a whole surface of metal interconnect on top of encapsulation material and NWs. For NW-based FETs, gate interconnect need to be separated from source and drain interconnects. Apparently a local interconnect process to connect NW-based devices is essential to many practical applications. In order to demonstrate the

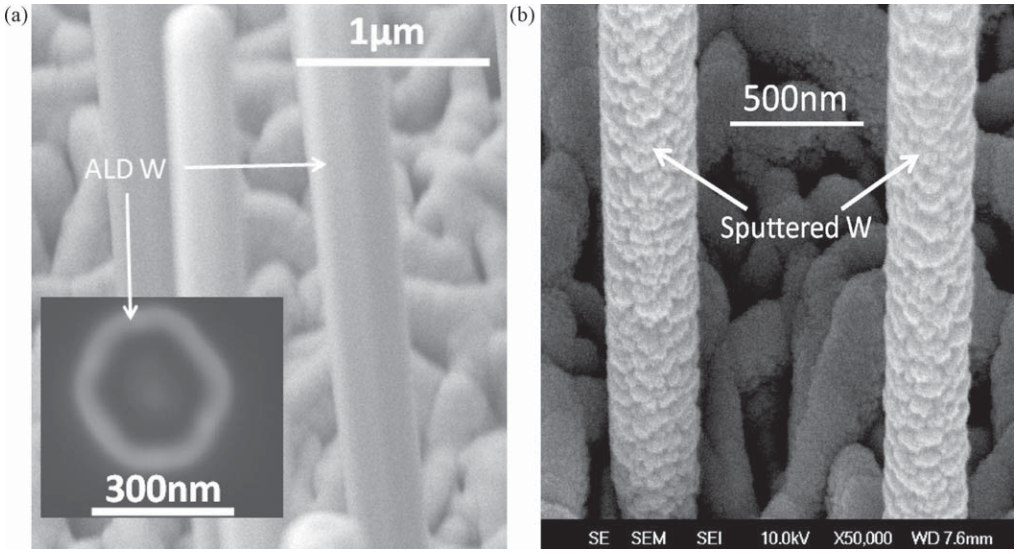

Fig. 3. Tungsten (W) layers deposited on GaN NWs by different coating methods: (a) ALD-W (inset: white shell), (b) sputtered-W. Compared to sputtered W, ALD-W is much smoother and more conformal to the surface of NWs with high aspect ratio (5–10 μm in length and 80–200 nm in diameter). ALD-W layer is used as a metal interconnect for vertical GaN NWs.

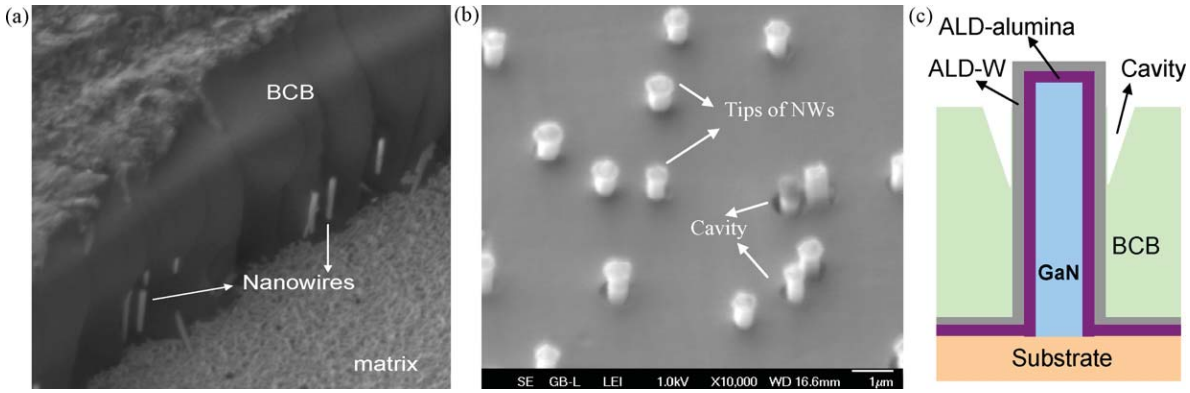

Fig. 4. BCB encapsulation process for vertical GaN NWs. (a) GaN NWs were buried in thick BCB by dripping. (b) Mechanical polishing was employed to reduce thickness of BCB and tips of NWs were then exposed after RIE process. (c) Schematic drawing of cavity shown in (b). Scale bar in (b): 1 μm.

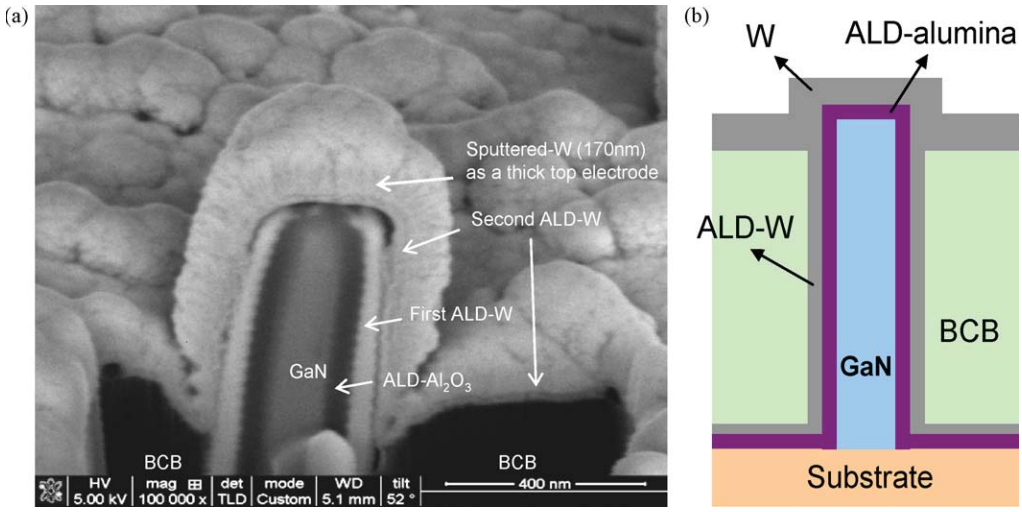

Fig. 5. (a) Cross-sectional view of NW with ALD layers after FIB cutting. Scale bar: 400 nm. (b) The corresponding schematic drawing. Second ALD-W was deposited for conformal coverage in the cavities. Sputtered-W with a thickness of 170 nm was deposited after second ALD as a thick top electrode.

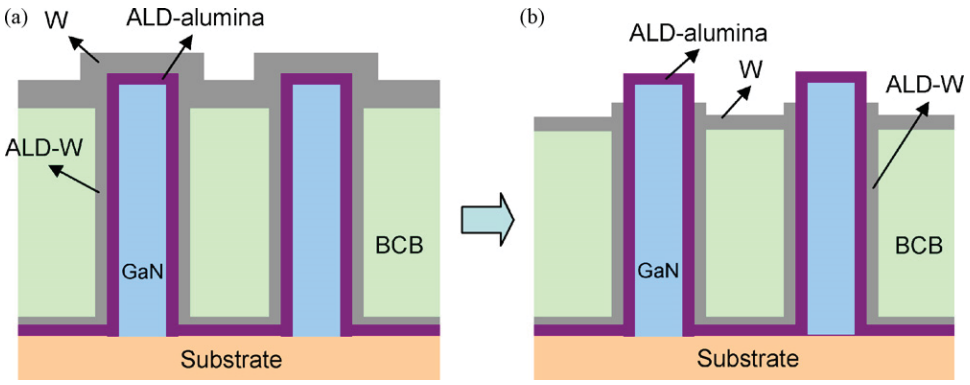

Fig. 6. Schematic drawing of (a) nanowires interconnected with tips covered, and (b) nanowires interconnected with tips exposed after the local interconnect process. Photoluminescence signal can be generated and measured after W at tips is locally removed.

capability of fabricating specific NW-based device configurations by using ALDs as interconnects, we have successfully developed a fabrication process to locally remove metal layer at tip region of NWs. With local interconnect process, ALD-W could provide current injections on NW-based devices while ALD-W at NW tip region is locally removed. These nanowire array devices could then be tested electro-optically as described in Section 4. Fig. 6 shows the schematic drawing of NWs interconnected with tip covered (a), and with tips exposed (b) after the local interconnect process.

The goal of the local interconnect process is to remove the W metallization layer on tips of NWs. Fig. 7 shows the detailed schematic process flow and corresponding experimental results. No photolithography mask is needed in this process. The process starts with as-grown GaN NWs (Fig. 7a) coated with ALD-Al_2O_3 and

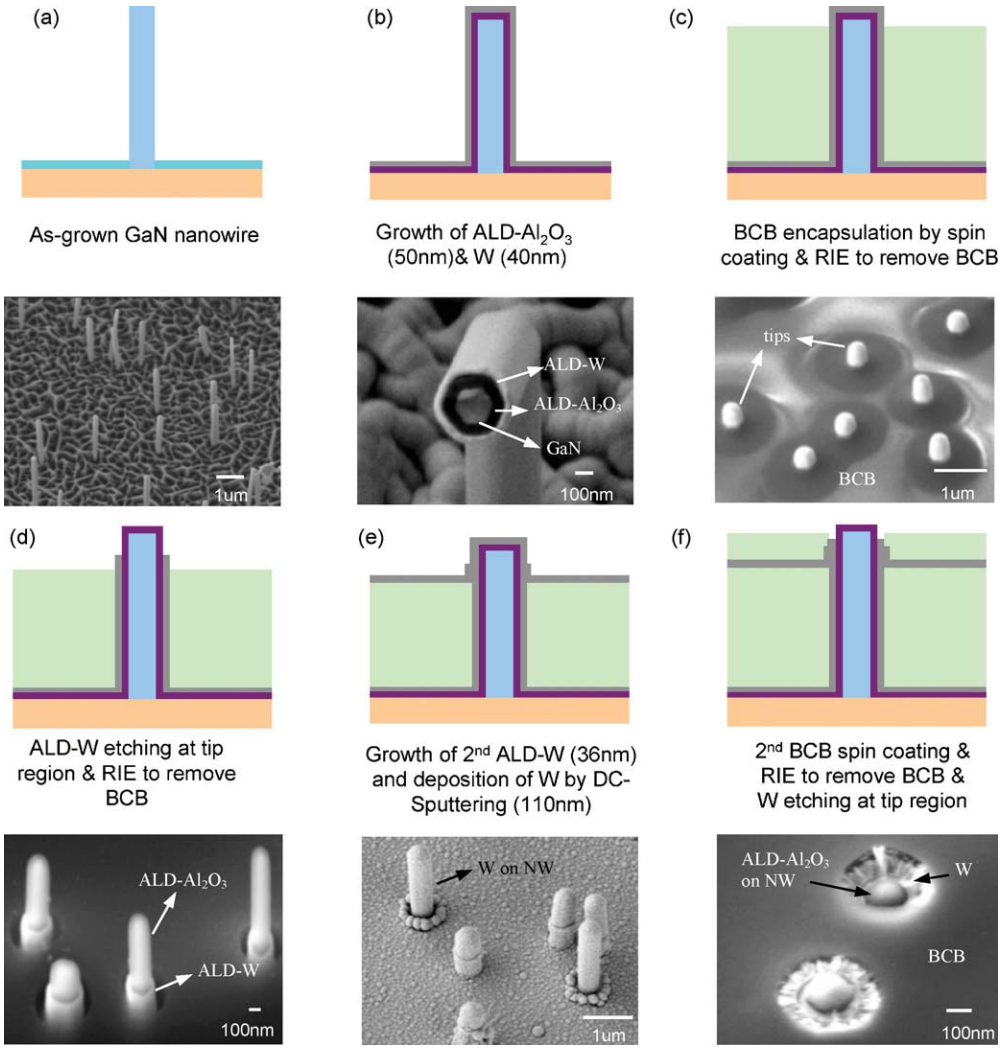

Fig. 7. Fabrication process flow and corresponding experimental results of a local interconnect process that results in nanowires interconnected with tips exposed (no W-layer on the NW tip).

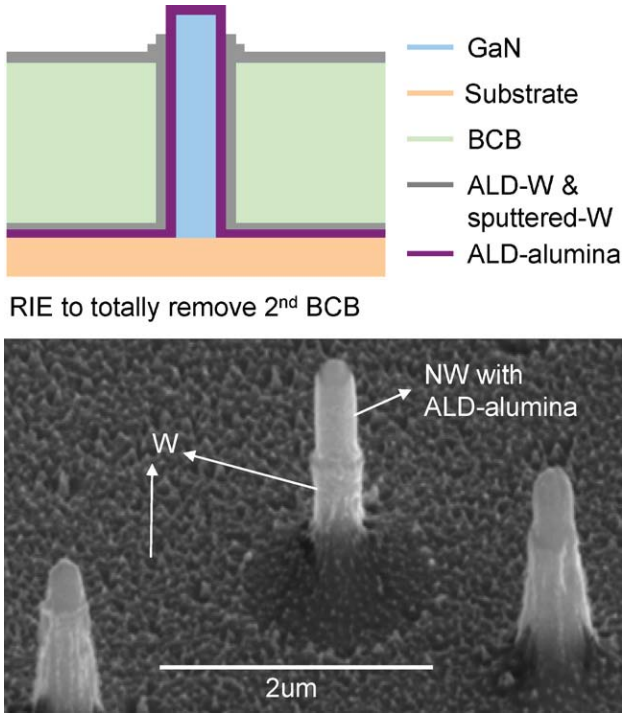

Fig. 8. (Top) Schematic drawing of final step of local interconnect process and (bottom) SEM image of GaN NWs with tip exposed (no W on tip region) after local interconnect process.

W (Fig. 7b). Fig. 7b shows a cross-sectional image of ALD-Al_2O_3 and W on a NW. SEM image was taken at the edge of a NW chip cut from a NW wafer. The NW was broken due to the cutting force. Again, Al_2O_3 and W grown by ALD method are conformal. To improve the wettability of NW surfaces, oxygen plasma treatment of 20 s was conducted before BCB spin-coating on NW sample. Next, tips of NWs were exposed by selective RIE etching (Fig. 7c) and ALD-W at tips was removed by W-etchant. ALD-Al_2O_3 is a good passivation layer and can sustain W-etching process. By controlling the etching time, length of W removal at tips can be controlled. We observed the local W removal at tips after further BCB etching by RIE (Fig. 7d). Top W interconnect was made by first a thin ALD-W layer (36 nm) for making sure that all NWs are covered and interconnected, and then a thick sputtered-W layer (110 nm) (Fig. 7e). Then, BCB was spun on the sample again. Tips of NWs were exposed by RIE and W (ALD-W and sputtered-W) at tips was removed by W-etchant (Fig. 7f). The etching time is critical not only to control the length of W interconnect at tip to be removed, but also not to cut off the top interconnect between NWs. Finally, BCB was removed by RIE as shown in Fig. 8. The ALD-W on NWs are electrically interconnected and W on tips is removed (Fig. 8). In local interconnect process, BCB was spun on NW sample, not by dripping. Thick BCB is not desirable because mechanical polishing process is required to reduce the thickness of BCB. Using BCB spin coating, thickness of BCB can be controlled by the ramping and spinning speed. Thus, polishing process can be eliminated if BCB is thin. Since we have eliminated mechanical polishing process, we do not need to worry about the possibility of NW damage. Cavity issue can also be improved by oxygen plasma treatment before BCB spin coating.

4. Tuning GaN nanowire bandgaps by heating

Wavelength controllability is important for applications of laser and LEDs. Previous studies focused on tuning NW bandgap by changing material compositions [22,23]. Changing the material properties from material itself is one way; applying an external pressure, temperature or electrical field could result in a dynamic tuning of the bandgaps. In our study, we demonstrate the dynamic tuning of GaN nanowire bandgaps by heating the NWs through ALD-W interconnect. With current injection to ALD-tungsten interconnect, the connection quality of ALD-W interconnect along NWs can also be verified by this bandgap tuning demonstration. ALD-W interconnect is locally heated due to joule heating when current passes through. As a result, the NWs are heated. As the temperature of a semiconductor increases, the lattice expands and then leads to a change of energy bandgap [24]. We used photoluminescence (PL) system to characterize the dynamic tuning of GaN nanowires bandgap [25,26]. Since W on tips of NWs was removed by local interconnect process, PL light can be generated and measured from the tips. PL signals are from the tips of the NWs, and verified by spatially-resolved and steady-state PL measurements to be published in another paper. PL signals are tuned by changing the power input supplied to ALD-W on NWs. To control the direction of current flow in ALD-W along the surface of NWs, two metal pads were made by FIB machining as shown in Fig. 9. As illustrated in Fig. 9a, metal pads 1 and 2 are separated by FIB machined trenches but electrically connected through the ALD-W interconnect on NWs and the NW base region.

Fig. 10 shows the experimental setup of PL measurement. NW sample is placed on a thermoelectric device (TEC) (functioning as a substrate heater) and excited with a continuous-wave (CW) HeCd

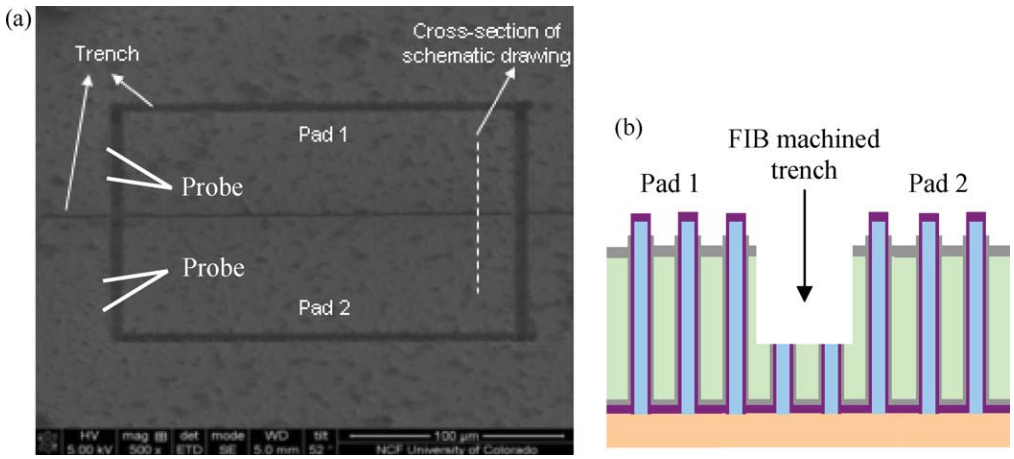

Fig. 9. (a) SEM image of trenches fabricated by FIB and (b) schematic drawing of cross-sectional view. Trenches were fabricated by FIB cutting to isolate pad 1 and pad 2. The dimension of each pad is 200 μm (width) × 100 μm (length). The depth of trenches is 3 μm.

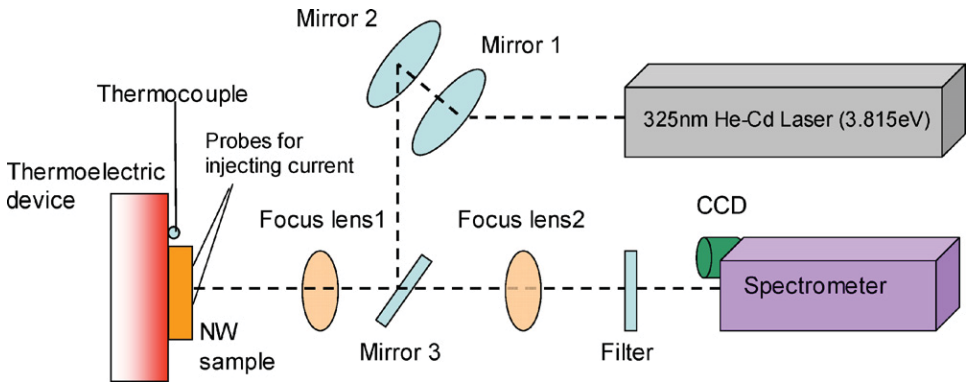

Fig. 10. Experimental setup of PL measurement. Probes were respectively positioned on pads of NW sample under optical microscope to provide current into W interconnect. The laser spot diameter is around 13 μm. Average number of NWs shined by laser is 10 by FESEM examination.

laser operating at 325 nm (3.815 eV). A K-type thermocouple is placed on the TEC to monitor the surface temperature of the TEC. Two electrical probes were respectively positioned and located at the metal pads machined by FIB using microscope. Fig. 11 shows the PL measurement results with/without injecting current into ALD-W interconnect. We first change TEC temperature to tune PL peak wavelength (solid line in blue). This shift can also be achieved by heating the same NWs sample via current injection into ALD-W interconnect as shown in the figure (dash line in red). Red-shifted PL spectrum is observed with power input of 1637 mW into ALD-W interconnect. Bandgap of GaN NW is changed due to the temperature increase by power input into ALD-W interconnect, thus changing the PL peak wavelength. The connection of ALD-W interconnect is also verified by PL measurement with injecting current. We also note that there is slightly change of the PL slope for different heating mechanisms (TEC heating or current injection) which could be due to the non-uniformity of the temperature distribution along the NWs. More PL tuning results are shown in Fig. 12. In experiment, temperature dependence of PL peak wavelength was first measured. We change the input power of the TEC and record PL signals at different TEC temperatures. There is no power input into ALD-W interconnect via electrical probes. It should be noted that PL peak wavelength is determined by using the quadratic fit to the neighboring data of raw peak. At one TEC temperature condition we record 6 measurements and make one error bar with one standard deviation. Afterward, we start to inject current into ALD-W interconnect on NWs via probes and tune the PL peak wavelengths. In Fig. 12, two target wavelengths, 368 and 366.04 nm, were chosen when surface temperatures of the TEC were 88 and 55.5 °C, respectively. At lower temperature conditions of the TEC (27.3 and 38.8 °C), we start to heat NWs by injecting current into ALD-W interconnect on NWs. By changing the input current supplied to ALD-W interconnect, PL peak wavelengths were tuned to our targets. The only flowing path for injected current is first from pad 1 through the ALD-W interconnect on NWs to the base region, and then flow back from base region to pad 2 through ALD-W interconnect on NWs. Tunable GaN NWs by heating demonstrates a feasible method to fast tune bandgap of GaN NWs. Also, this heating effect is also important to the NW-based devices with interconnect along NWs.

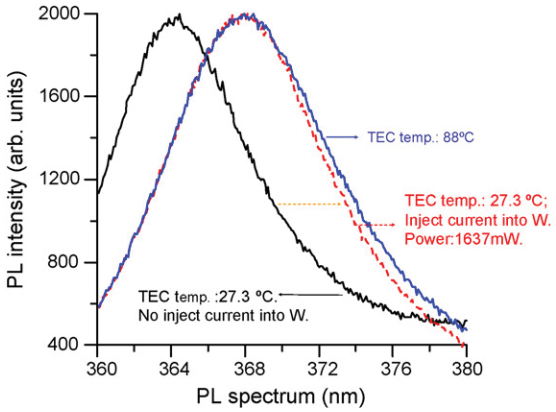

Fig. 11. Experimental results of PL tuning by using TEC to heat NWs (solid line in blue) and by injecting current into W interconnect to heat NWs (dash line in red). The connection of W interconnect on NWs was confirmed by current injection into W interconnect to tune PL wavelength. The difference in PL slope could be due to the non-uniformity of the temperature distribution along the NWs under different heating mechanisms (TEC heating or current injection). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of the article.)

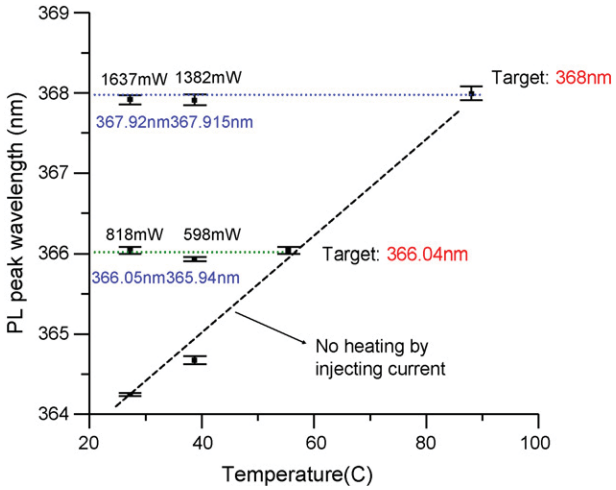

Fig. 12. Experimental results of tunable PL wavelength by heating. PL peak wavelength of NW array can be dynamically tuned to target wavelengths by changing the input power supplied to ALD-tungsten interconnect. PL peak wavelength is determined by using the quadratic fit to the neighboring data of raw peak.

5. Conclusions

We have demonstrated an ALD-enabled interconnect technology for vertical nanowire arrays. The nano-scaled conductor/dielectric multilayer is essential to the interconnect technology. FESEM images and cross-sectional image by FIB confirm the conformal ALD-Al_2O_3 and W layer along the GaN NWs with high aspect ratio. We have also developed a fabrication process to locally remove and connect W interconnect on NWs. By injecting current into W interconnect along NWs, PL wavelengths can be tuned

dynamically by changing input current. PL tuning experiment also verifies the connection of interconnect on NWs. This interconnect technology can be applied to various vertical nanowire-based devices, such as nanowire LEDs, nanowire-based FETs, resonators, batteries or biomedical applications.

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