The Negative Bias Temperature Instability vs. High-Field Stress Paradigm

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***Abstract*—A new and more accurate fast-I_DV_G measurement methodology is utilized to examine the transient degradation and recovery associated with the negative-bias temperature instability (NBTI). The results reveal that the anomalously large initial degradations reported in the recent literature are actually due to high-field stress acceleration and are not representative of low-field NBTI phenomena. Our observations at these higher fields reveal the presence of an, as yet unaccounted for, electron trapping/de-trapping component. The electron trapping is a signature of high-field stress degradation. While this high-field stress acceleration is unavoidable, care must be taken to account for this component in NBTI analysis. Collectively, our observations indicate that this high-field stress component is present and unaccounted for in a large portion of the recent NBTI literature.**

***Keywords*—NBTI, high-field stress, electron trapping**

I. Introduction

The negative bias temperature instability (NBTI) has become the major reliability issue in advanced CMOS technologies [1]. While the symptoms of NBTI are well known (negative threshold voltage shift and transconductance degradation in p-channel devices subject to negative gate voltages at elevated temperatures), the mechanism responsible for these parametric shifts is still hotly debated [2]. Many researchers link NBTI to an interface state generation process via hydrogenous depassivation (reaction-diffusion model) [3]. Others believe that NBTI also involves additional hole trapping/de-trapping phenomena [4]. Separation of these mechanisms is further complicated by measurement error due to NBTI relaxation [5]. Regardless of the identity of the offending mechanism, we note that the recent increase in device operation voltages has led many researchers to accelerate NBTI stresses to higher dielectric fields far greater than those used to develop the original NBTI models (<6 MV/cm) [6, 7]. The extreme acceleration invokes additional degradation mechanisms (high-field stress) which make it difficult to interpret results strictly within the NBTI framework. Despite the common observation of large "NBTI-induced" parametric shifts which fall outside nearly all lifetime specifications [7, 8], many researchers use these high-field accelerated observations to infer information about the lower-field NBTI mechanisms.

In this work, we utilize a fast-I_DV_G measurement methodology which monitors stress-induced threshold voltage shifts (ΔV_{TH}) and channel transconductance degradation (ΔG_M) with minimal measurement time interruption (2 μs). This measurement technique is used to examine the "NBTI" induced parametric degradation and relaxation in fully processed SiON pMOSFETs. We find that the large initial ΔV_{TH} reported in much of the recent NBTI literature is only observable for exceedingly high stress voltages (≥10 MV/cm). At operation conditions, we observe no measurable degradation. Analysis of the corresponding peak-ΔG_M values

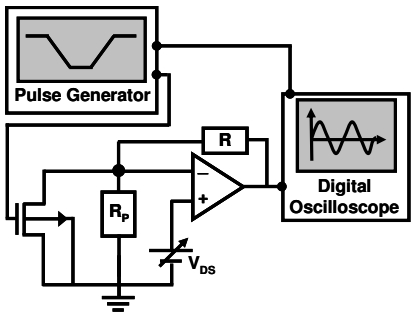

Figure 1: Fast-I_DV_G experimental set-up used in this work.

as a function of stress and relaxation times reveals the presence of an, as yet unaccounted for, electron trapping/de-trapping component. The electron trapping/de-trapping component is a known signature of high-field stress phenomena. Identification of this electron trapping/de-trapping component and the realization that the large ΔV_{TH} and ΔG_M parametric shifts only occur for exceedingly high stress voltages lead us to conclude that much of the recent "NBTI" literature is actually dominated by a combination of NBTI and high-field stress degradation mechanisms. Consequently, it is very likely that the high-field accelerated data's incompatibility with low-field NBTI theory is a major source of the confusion surrounding the NBTI mechanism.

II. Experimental Methods

In an attempt to minimize the fast and significant relaxation at the conclusion of NBTI stress, alternative fast measurements are commonly employed. The most promising of these utilizes a high-speed oscilloscope to capture the entire I_DV_G characteristic curve within microseconds after stress removal. Typically, the ΔV_{TH} shift is extracted from the I_DV_G curve by either (1) tracking the gate voltage required to maintain a low level drain current or (2) by the linear extrapolation of the I_DV_G characteristic at maximum G_M. Method (1) poses a problem due to the limited dynamic range of the high-speed digitizer (typically 8 bit). This forces ΔV_{TH} extraction at much higher drain current levels and introduces significant error. Method (2) also presents obstacles associated with G_M extraction. The fast-I_DV_G characteristic curve has significant noise inherent to oscilloscope acquisition and, if not careful, amplifier distortion. This translates to distorted G_M-V_G characteristics ($G_M = dI_D/dV_G$) and inaccurate $G_M/\Delta V_{TH}$ extractions. Our experimental set-up (Fig. 1) is similar to earlier reports [7] and with the help of an additional post-processing filter [9] utilizes the ΔV_{TH} extraction method (2). Fig. 2 illustrates the filtered I_DV_G and G_M-V_G characteristics collected using our fast-I_DV_G apparatus as well as those obtained using a semiconductor parameter analyzer. We note that our filtered I_DV_G curves exhibit very good agreement with the DC characteristics. The general agreement between the two measurements is sufficient to allow for accurate ΔV_{TH} and

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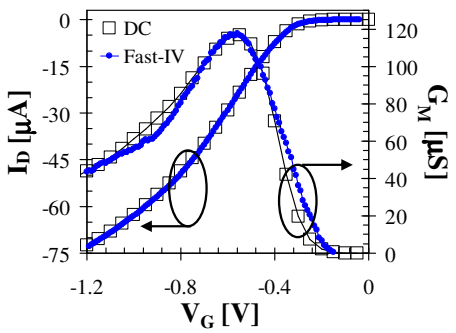

Figure 2: Comparison of the extracted fast-I_DV_G and DC measurements.

peak-G_M extraction using the preferable V_{TH} extraction methodology.

This study utilizes 2 x 0.07 μm^2 and 2 x 0.06 μm^2 (physical gate area) fully processed pMOSFETs with SiON gate dielectrics (thickness = 1.6 nm). All measurements were performed with -50 mV on the drain electrode while the source and substrate terminals were grounded. All stress and relaxation measurements were made at 125 ^{o}C. A representation of the gate voltage pulse sequences used in this study is schematically shown in Fig. 3. The sequence consists of a trapezoidal "stress" pulse and a triangular post-relaxation "sense" pulse separated by a variable relaxation time where the gate voltage is held at 0 V. Fast-I_DV_G measurements were taken at the rising and falling edges of the pulse train to obtain pre-stress (a), post-stress (b), and post-relaxation (c) fast-I_DV_G characteristics. The extracted values from the post-relaxation measurement consist of the average of the falling and rising measurements of the sense pulse (c). Throughout this manuscript we report two different sets of ΔV_{TH} and ΔG_M degradation values as per the following relations with reference to Fig. 3:

$$\Delta V_{TH}(ab) = V_{TH}(b) - V_{TH}(a) \quad (1a)$$

$$\Delta V_{TH}(ac) = V_{TH}(c) - V_{TH}(a) \quad (1b)$$

$$\Delta G_M(ab) = \frac{G_M(a)-G_M(b)}{G_M(a)} \times 100 \quad (1c)$$

$$\Delta G_M(ac) = \frac{G_M(a)-G_M(c)}{G_M(a)} \times 100 \quad (1d).$$

$\Delta V_{TH}(ab)$ and $\Delta G_M(ab)$ are measures of the stress-induced degradation (with 2 μs relaxation), and $\Delta V_{TH}(ac)$ and $\Delta G_M(ac)$ are measures of the stress-induced degradation after a given relaxation time. Alternatively, a comparison of the *(ab)* and *(ac)* measurements is a measure of how much of the stress-induced degradation has recovered.

III. Results and Discussion

Fig. 4a shows $\Delta V_{TH}(ab)$ as a function of stress voltage (-1.2 V to -2.7 V) for various stressing times (0.1 s to 1000 s). To improve the accuracy of the ΔV_{TH} extraction, we repeat the measurement sequence (Fig. 3) 12 times for the 0.1 s, 1 s, and 10 s stress times, 3 times for the 100 s stress time, and 1 time for the 1000 s stress time. Clearly, the stress voltage plays a large role in the stress-induced ΔV_{TH}. Contrary to many recent

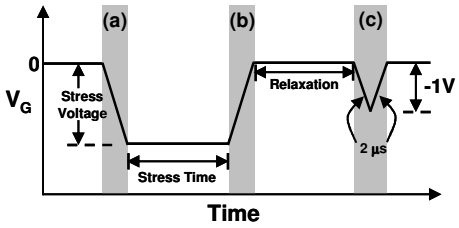

Figure 3: Schematic illustration of the stress/relaxation sequence utilized in this work.

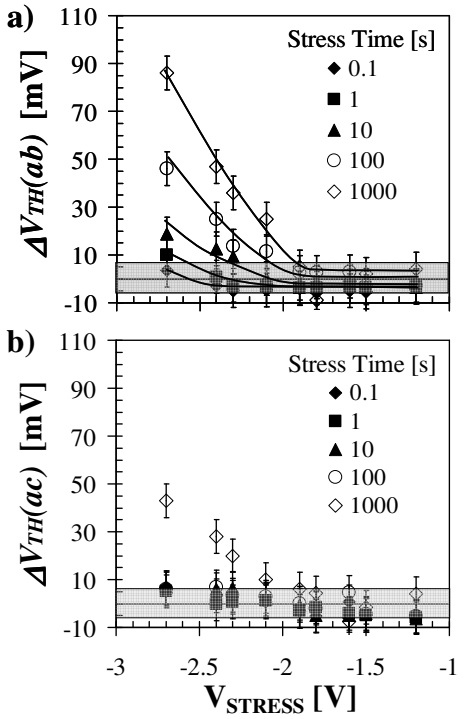

Figure 4: Stress-induced (a) and relaxed (b) ΔV_{TH} as a function of V_{STRESS} for several stress times in 2 x 0.07 μm^2 pMOSFETs. The measurement time is 2 μs, and the recovery time is 5 s.

reports [7, 8], no large ΔV_{TH} is observed for moderate short term stresses. Even at V_{STRESS} = -1.8 V, a level which is not exactly moderate, no clear degradation is observed even after 1000 s. Large stress-induced ΔV_{TH} is only observed for *exceedingly high* stress voltages and longer stress times. The steep rise in ΔV_{TH} at V_{STRESS} < -1.8 V, particularly after longer stress time, clearly suggests that there is a shift in the dominating degradation mechanism. A crude estimation (accounting for quantum confinement, poly-depletion, and the flat band voltage) of the dielectric field at this boundary (V_{STRESS} = -1.8 V) yields ≈10 MV/cm. This is well above the 6 MV/cm boundary of traditional defined NBTI and is approaching fields which are considered too high even for high-field stress TDDB studies [10].

Fig. 4b shows the complementary $\Delta V_{TH}(ac)$ as a function of gate bias for the same stress voltages and times as in Fig. 4a (relaxation time = 5 s). With the exception of the 1000 s stress at higher stress voltages, all other stress voltages and times show no measurable residual degradation or "permanent" ΔV_{TH}. We attribute the residual degradation (after 5 s relaxation) in the 1000 s high V_{STRESS} case to increased interface state generation at these extreme stress conditions.

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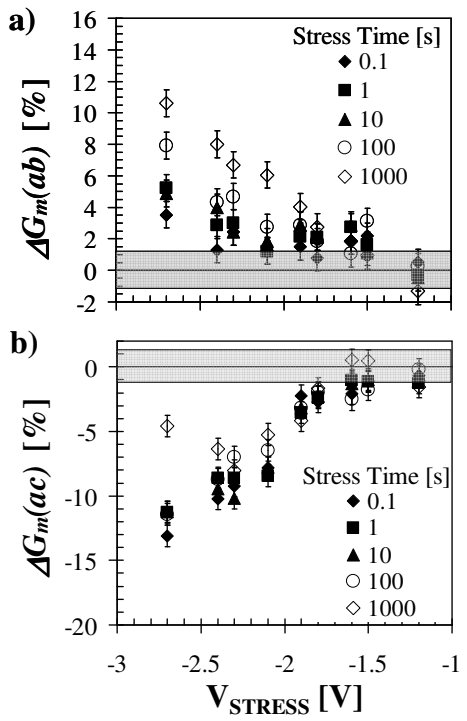

Figure 5: Corresponding stress-induced (a) and relaxed (b) ΔG_M as a function of V_{STRESS} in 2 x 0.07 μm² pMOSFETs. The measurement time is 2 μs, and the recovery time is 5 s.

Since both NBTI and high-field stress are known to exhibit relaxation behavior, looking purely at the ΔV_{TH} is insufficient to differentiate the two mechanisms.

Fig. 5a illustrates the corresponding $\Delta G_M(ab)$ as a function of stress voltage and stress times. The $\Delta G_M(ab)$ trend mimics the $\Delta V_{TH}(ab)$ trend (increased G_M degradation at higher stress voltages and longer stress times) and also exhibits a very strong dependence on the stress voltage. Since both NBTI and high-field degradation mechanisms are known to degrade G_M, the observed dependence is as expected. However, an examination of the $\Delta G_M(ac)$ (post 5 s relaxation) reveals a surprising result. As the stress voltage and stress duration increase, we observe negative $\Delta G_M(ac)$ values (Fig. 5b). Negative $\Delta G_M(ac)$ is an indication that, after 5 s of relaxation, the measured peak G_M has improved to values which are greater than before stress. Clearly, this atypical G_M behavior cannot be explained by reaction-diffusion kinetics. Even if a hole trapping/de-trapping component is added to the explanation, it is difficult to argue for G_M improvement. Thus, we must seek an alternate explanation outside of the common NBTI models.

NBTI *degradation* has been linked to interface state generation, hole trapping, or both [1, 4, 11]. NBTI *relaxation* is then explained by the annihilation of these interface states, the de-trapping of holes, or both [1, 4, 11]. These mechanisms can be used to explain our observations in Figs. 4a, 4b, and 5a (negative recoverable ΔV_{TH} and G_M degradation). However, no combination of these positive charge NBTI paradigms can explain our post-stress G_M improvement observation (Fig. 5b). G_M improvement is only possible if the as-processed interface states are somehow compensated to reduce the Coulombic scattering. Realization that (1) the G_M improvement is only observed at high-field stress conditions (≥ 10 MV/cm) and (2) high-field stress is known to trap both holes *and electrons* in the dielectric as well as generate interface states [12, 13] provides the necessary components to explain our observations.

The explanation is as follows: in the "stress" phase, hole *and electron* trapping takes place in the gate dielectric as well as the generation of interface states. At the conclusion of stress, the net positive charge associated with the trapped holes and the interface states collectively dominates the negative charge due to the trapped electrons. This results in a negative ΔV_{TH} and a degraded peak G_M. During relaxation, both holes and electrons de-trap but at different rates (holes de-trap faster than electrons). After 5 s of relaxation, the holes are largely de-trapped while electron de-trapping is still incomplete. The net negative charge due to the electrons compensates the positively charged interface states which effectively reduces the Coulombic scattering and improves G_M.

We can use the fact that electrons and holes de-trap at different rates to further test the validity of our assumptions. Fig. 6 shows $\Delta G_M(ab)$ and $\Delta G_M(ac)$ as a function of relaxation time for a device that was stressed at -2.5 V / 125 °C / 10 s. As before, to improve statistics each data point represents the average of 12 repeated measurements with a fresh device for each relaxation time. The $\Delta G_M(ab)$ is, as expected, invariant of the relaxation time. However, the $\Delta G_M(ac)$ is a strong function of relaxation time. The conclusion of stress leaves the device with increased interface states and both trapped holes and electrons. The combination of trapped holes and interface states again overwhelms the trapped electrons, and we observe a net increase in positive charge and Coulombic scattering ($\Delta G_M(ac)$ degradation at short relaxation times). As the relaxation time increases, the hole concentration decreases and the net positive charge and Coulombic scattering also decreases. This leads to a reduction in $\Delta G_M(ac)$. This process continues until the trapped holes are largely depleted, leaving only the trapped electrons in the bulk. The net positive charge is now at a minimum. If the net positive charge is less than the amount before stress (due to as-processed interface states), the peak-G_M will improve (Fig. 6). At longer relaxation times, the electrons eventually also de-trap, leaving only positively charged interface states and $\Delta G_M(ac)$ returns to degradation.

These results confirm our assumptions of an electron trapping/de-trapping component and are also completely consistent with the snapshot of our 5 s relaxation observations (Fig. 5b). While G_M improvement due to electron trapping is rare, it is not without precedent. Charpenel *et al.*, for example, observed G_M improvement after injecting electrons into the gate dielectric [14]. Additionally, Weber *et al.* suggest that trapped electrons could effectively "tie up" interface states and prevent them from charging or discharging [15].

Further evidence supporting our high-field stress electron trapping/de-trapping argument stems from the fact that G_M improvement is only observable when the measurement time is sufficiently fast. Fig. 7 illustrates $\Delta G_M(ac)$ as a function of measurement time (rising/falling time of the gate pulse) for various relaxation times. Depending on the relaxation time, $\Delta G_M(ac)$ exhibits improvement or degradation. Clearly, this

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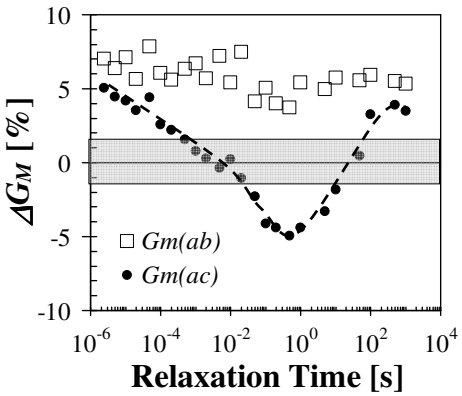

Figure 6: Stress-induced (ab) and relaxed (ac) ΔG_M as a function of relaxation time in 2 x 0.06 μm^2 pMOSFETs subject to -2.5 V at 125 °C for 10 s. The measurement time is 2 μs.

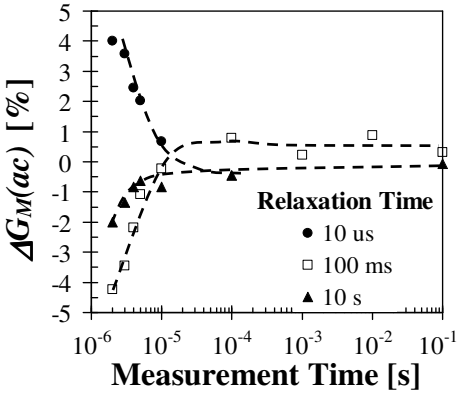

Figure 7: Relaxed ΔG_M as a function of measurement time for various relaxation times in 2 x 0.07 μm^2 pMOSFETs subject to -2.5 V at 125 °C for 10 s.

transient G_M behavior is only observable when the measurement time is less than 10 μs. The need for very fast measurements is due to the fact that the formation of an inversion layer of holes will neutralize any trapped electrons via tunneling. Since the gate dielectric is only 1.6 nm thick, the tunneling front rapidly reaches the trapped electrons [16].

The evidence of electron trapping/de-trapping strongly supports the conclusion that the V_{STRESS} < -1.8 V data in Fig. 4 is dominated by high-field stress. It also conclusively shows that the presence of a high-field stress mechanism affects many recent NBTI reports that utilize extreme accelerated stress voltages. It is common knowledge that extraneous mechanisms may be introduced by highly accelerated stress fields. What we found here should be expected. What is surprising is that so much effort has been spent trying to explain recent (high field) NBTI experiments within the traditional reaction-diffusion NBTI framework.

IV. Conclusions

We have utilized a fast-I_DV_G methodology to examine the transient ΔV_{TH} and ΔG_M in devices subject to "NBTI-like" stresses. Our results clearly show that the unreasonably large ΔV_{TH} often reported in the recent literature is very likely a consequence of an additional high-field stress degradation mechanism. Analysis of the ΔG_M extracted from the fast-I_DV_G measurements clearly shows a post-relaxation G_M improvement to values better than before stress. This is attributed to an electron trapping/de-trapping component which is a signature of high-field stress degradation (not NBTI). Our results collectively indicate that the majority of the recent "NBTI" literature actually reports degradation which is composed of both NBTI and high-field stress degradation modes. This additional high-field stress mode must be included in future analysis to ensure accurate reliability predictions.

V. Acknowledgments

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