The Role of High-Field Stress in the Negative-Bias Temperature Instability

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***Abstract*—In this paper, a fast drain-current measurement methodology which supports the standard threshold voltage and transconductance extractions associated with the fast dynamic negative-bias temperature instability (NBTI) is presented. Using this methodology, we show that production quality transistors exhibit only minimal degradation after a brief stress at moderate to high dielectric fields (contrary to the excessive degradation reported in the recent literature). The degradation at stress conditions which are consistent with many recent NBTI studies is shown to be dominated by high-field stress, instead of NBTI. The ability to extract transconductance from fast drain-current measurements helps to identify the existence of a latent electron trapping/detrapping component which provides further support of a degradation mechanism dominated by high-field stress. This high-field-stress component, while dominating, has not been accounted for in most of the recent NBTI literature.**

***Index Terms*—Electron trapping, high-field stress, hole trapping, negative-bias temperature instability (NBTI).**

I. Introduction

THE NEGATIVE-BIAS temperature instability (NBTI) in p-channel metal–oxide–semiconductor field-effect transistors (pMOSFETs) has been a known degradation mode for half a century [1]. For the majority of this time period, most researchers were primarily concerned with hot-carrier degradation failure modes and NBTI remained a topic of academic curiosity. However, the last decade has seen an explosion of interest in NBTI due to its dominance (more than hot carrier) in devices with ultrathin nitrided gate dielectrics [2], [3].

Despite extensive work in recent years, the present understanding of the NBTI phenomenon is far from complete and still quite confusing. It is well established that NBTI manifests as a negative threshold-voltage shift ($\Delta V_{\rm TH}$) and peak transconductance (G_M) degradation in pMOSFETs subject to negative gate voltages at elevated temperatures [4]. The confusion surrounding NBTI is heightened by the recent emphasis on the poststress fast relaxation of these parametric shifts [5]. While the relaxation phenomenon is not new [6], it has recently been re-examined with great scrutiny [7]. A variety of "fast" measurement techniques have been introduced by many research groups to either capture the "unrelaxed" degradation [8]–[10] or to capture the relaxation process in detail [7], [11], [12]. In all of these new measurements, the standard $V_{\rm TH}$ and G_M extraction methodology (linear extrapolation of the I_D–V_G characteristic at maximum G_M) cannot be employed and the measurements require alternative extraction procedures. The majority of the studies using these techniques report severe NBTI degradation after accelerated short stresses ($\geq$ 100-mV $V_{\rm TH}$ after 1-s stress) [12]–[16]. However, such severe degradation would have prevented the qualification of most advanced CMOS technologies presently in use. The fact that products from these advanced technologies are already in many everyday applications indicates that these reports cannot be correct and should be discounted. Instead, they account for a large fraction of the controversy surrounding the fundamentals of NBTI.

The NBTI-induced positive-charge accumulation (which leads to the negative $\Delta V_{\rm TH}$ and G_M degradation) has been linked to the generation of interface states via hydrogenous depassivation (reaction–diffusion kinetics) [17]–[19] or to bulk dielectric hole trapping/detrapping [20] or some combination of both mechanisms [21], [22]. For much of the last few decades, the reaction–diffusion model has dominated the NBTI literature [17]. However, recent detailed observations of relaxation has led many researchers to instead advocate an NBTI mechanism heavily influenced by a hole trapping/detrapping process [11], [12], [20], [21]. While the mechanism debate rages on, few researchers [23] notice that the majority of recent NBTI experiments involve stress conditions well outside of the traditionally accepted NBTI range. Historically, NBTI is defined to occur at lower dielectric stress fields ($\leq$ 6 MV/cm) where carrier injection is negligible [18]. The absence of carrier injection is, at least partly, responsible for the original introduction of NBTI mechanisms to differentiate them from those which carrier injection dominates, such as high-field stress. The scaling trends of the last decade have forced the operation gate-oxide field to increase to $>$ 6 MV/cm in advanced technologies [24]. This has led many researchers to accelerate NBTI stress at fields much higher than the 6-MV/cm (with some $>$ 15 MV/cm [25]) boundary that defines the original NBTI phenomenon. Such high stress fields are traditionally relegated to the high-field-stress category, such as time-dependent dielectric breakdown (TDDB) [26]. In fact, some of the stresses utilized in recent

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NBTI literature are considered too extreme even for the high-field-stress standard [26]. The common failure to recognize the high-field-stress component in NBTI measurements has led to significant efforts to modify the reaction–diffusion model to better fit the observations [27].

In this paper, we extend some of our earlier results [28]–[31] which show that the degradation and relaxation phenomena observed at stress conditions that are typical in the recent NBTI literature are dominated by a high-field-stress degradation mechanism. The key point of this work is that many of the recent "NBTI" reports do not consist purely of an NBTI phenomenon but also involve a high-field-stress component. This work is *not* meant to address the validity of the commonly used NBTI models. Considering that much of the confusion in the literature originates from the various measurement techniques, a key feature of our work is the introduction of a high-speed measurement methodology which captures relaxation phenomena using the standard (linear extrapolation) procedure to extract $\Delta V_{\rm TH}$. Our results on production quality devices are inconsistent with the extreme degradation phenomena reported in the recent literature.

II. Experimental Methods

Due to the fast and significant relaxation at the conclusion of NBTI stress, many researchers employ a technique where the transistor drain current (I_D) degradation is monitored at the stress condition (without interruption) [8], [10]. This on-the-fly (OTF) methodology produces relaxation-free measurements but requires significant modeling to extract $\Delta V_{\rm TH}$ values [9]. Other researchers tackle the relaxation issue by employing fast measurements which utilize a high-speed oscilloscope and fast amplifier circuit to capture the entire I_DV_G characteristic curve within microseconds after stress removal [11], [12]. These fast-I_DV_G measurements avoid the reliance on $\Delta V_{\rm TH}$ modeling, but have their own $V_{\rm TH}$ extraction issues. Typically, the $\Delta V_{\rm TH}$ shift is extracted from the I_DV_G curve by either of the following methods: (1) monitoring the gate voltage required to maintain a low level drain current, and (2) linear extrapolation of the I_DV_G characteristic at maximum G_M [32]. Method (1) poses a problem due to the limited dynamic range of the amplifier and high-speed digitizer. This forces $\Delta V_{\rm TH}$ extraction at much higher drain-current levels which introduces significant error, similar to OTF methods. Method (2) also presents obstacles associated with finding the maximum G_M. The fast-I_DV_G characteristic curve is acquired with significant noise inherent to oscilloscope acquisition and, if not careful, amplifier distortion. This translates to distorted G_M–V_G characteristics ($G_M = dI_D/V_G$) and inaccurate $G_M/\Delta V_{\rm TH}$ extractions. Our experimental setup (Fig. 1) is quite similar to earlier reports [12], [33] and utilizes the $\Delta V_{\rm TH}$ extraction method (2). In this measurement, a voltage pulse is applied to the gate electrode while the drain current is monitored by a fast operational amplifier circuit. Great care was exercised to minimize amplifier distortion by minimizing cable lengths and insuring good impedance matching. The G_M–V_G accuracy was further improved by careful minimization of experimental noise and a postprocessing data filtering scheme [30].

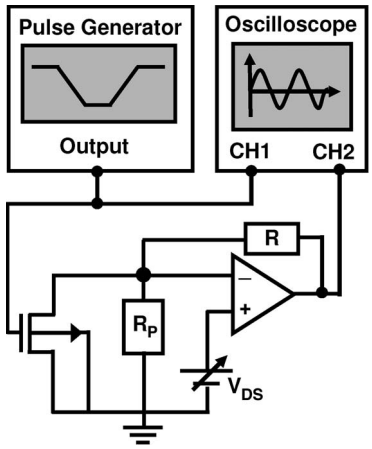

Fig 1. Fast-I_DV_G experimental setup using a pulse generator, digital oscilloscope, and fast amplifier circuit. The approach is quite similar to that proposed in [12] and [33]. Note that R_p is a resistor (typically equal to R) which is used to insure circuit stability when the device is off [52].

Our filter is formally equivalent to the well-known Savitzky–Golay method [34], but is far less efficient in computation. Its ability to handle unequally spaced data is the motive for developing our own routine [30]. Fig. 2(a) and (b) shows the raw and filtered room-temperature I_DV_G characteristics collected using our fast-I_DV_G apparatus as well as those obtained using a semiconductor parameter analyzer. We note that our filtered I_DV_G curves exhibit very good agreement with the dc characteristics. Fig. 2(c) shows the corresponding G_M–V_G characteristic curves extracted from the fast-I_DV_G and dc parameter analyzer measurements. Again, we observe very good agreement between the fast-G_M and dc-G_M measurements. We were careful to make these calibration measurements at room temperature and to utilize relatively low gate voltages to minimize any degradation. Thus, the general agreement between the two measurements is sufficient to allow for accurate $\Delta V_{\rm TH}$ and peak-G_M extraction. Our fast-I_DV_G approach [30] allows us to measure degradation and relaxation with only minimal (2-μs) stress interruption using the standard maximum G_M $V_{\rm TH}$ extraction methodology which is relatively immune to many of the pitfalls that plague the other $\Delta V_{\rm TH}$ extraction methodologies. It should be noted that the operational amplifier response is much faster than the 2 μs reported here. The 2-μs limit was imposed to insure accurate $V_{\rm TH}$ and G_M extractions.

This study utilizes 2×0.07 μm^2 and 2×0.06 μm^2 (physical gate area) fully processed pMOSFETs with SiON gate dielectrics (thickness = 1.6 nm). All measurements were performed with -50 mV on the drain electrode while the source and substrate terminals were grounded. All stress and relaxation measurements were made at 125 °C. A representation of the gate-voltage pulse sequences used in this study is schematically shown in Fig. 3. Fast-I_DV_G measurements were taken at the rising and falling edges of the pulse train to obtain prestress (a), poststress (b), and postrelaxation (c) fast-I_DV_G characteristics. The extracted values from the postrelaxation measurement consist of the average of the falling and rising measurements of the sense pulse (c). Throughout this paper, we report two

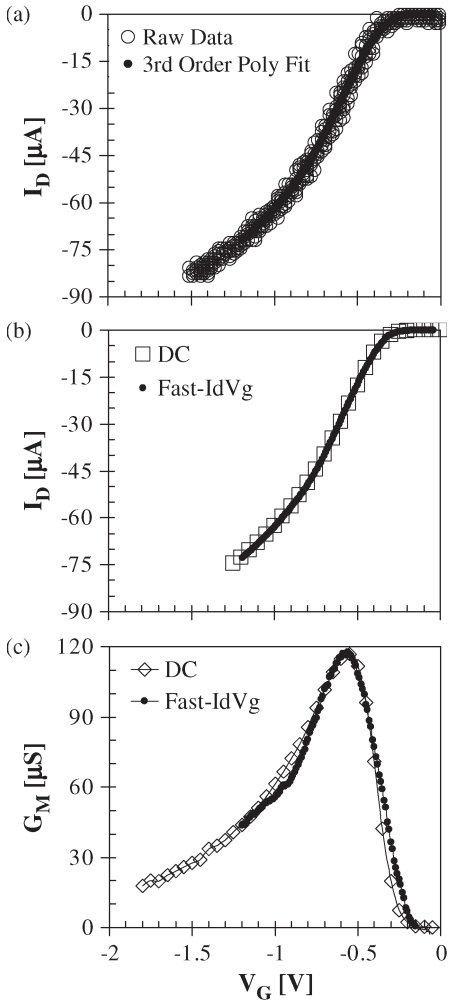

Fig. 2. (a) Comparison of raw and filtered fast-I_DV_G characteristics for a 2×0.07 μm^2 SiON pMOSFET with $V_{\rm DS} = -50$ mV at room temperature. The fast-I_DV_G curve arises from the rising edge of a single gate pulse. The measurement time (rise time of the pulse) is 2 μs. Our filter employs a third-order polynomial least-squares smoothing differentiation routine [30]. (b) Comparison of the filtered fast-I_DV_G characteristic [from (a)] with a "dc" characteristic obtained using a semiconductor parameter analyzer shows a good correlation. (c) Extracted $G_M - V_G$ characteristics from the filtered fast-I_DV_G and dc measurements show good correlation which is sufficient to monitor the peak-G_M values as a function of stress and relaxation.

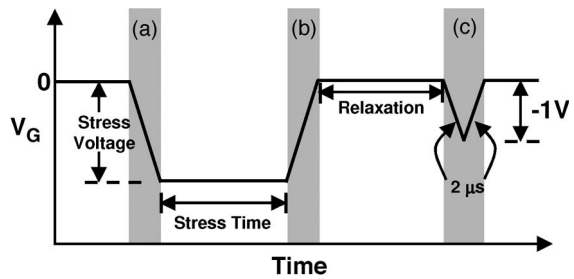

Fig. 3. Schematic diagram of the gate-voltage pulses during stress and measurement sequences. The sequence consists of a trapezoidal "stress" pulse and a triangular postrelaxation "sense" pulse separated by a variable relaxation time where the gate voltage is held at 0 V. $V_{\rm TH}$ and G_M values are extracted at the (a) prestress, (b) poststress, and (c) postrelaxation transitions. The postrelaxation values are an average of the up and down transition measurements.

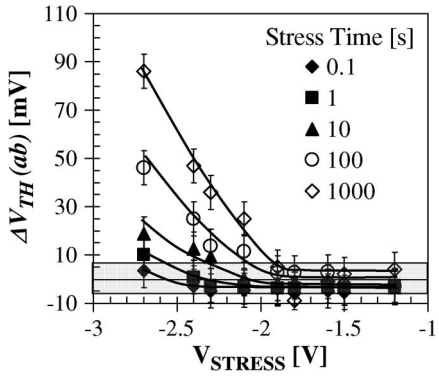

Fig. 4. $\Delta V_{\rm TH}(ab)$ (stress induced) as a function of gate stress voltage for various stress times in 2×0.07 μm^2 pMOSFETs at 125 °C. It is clear that the fast NBTI degradation only occurs for exceedingly high stress voltages and longer stress times. Throughout this paper, we argue that the stress voltages required to observe these $\Delta V_{\rm TH}$'s invoke an additional high-field-stress degradation mechanism. The measurement time is 2 μs. The box centered at 0 mV represents ± 1 standard deviation error bar. The lines are only a guide for the eye.

different sets of $\Delta V_{\rm TH}$ and ΔG_M degradation values as per the following relations with reference to Fig. 3:

$$\Delta V_{\rm TH}(ab) = V_{\rm TH}(b) - V_{\rm TH}(a) \tag{1a}$$
$$\Delta V_{\rm TH}(ac) = V_{\rm TH}(c) - V_{\rm TH}(a) \tag{1b}$$
$$\Delta G_M(ab) = \frac{G_M(a) - G_M(b)}{G_M(a)} \times 100 \tag{1c}$$
$$\Delta G_M(ac) = \frac{G_M(a) - G_M(c)}{G_M(a)} \times 100. \tag{1d}$$

$\Delta V_{\rm TH}(ab)$ and $\Delta G_M(ab)$ are measures of the stress-induced degradation (with 2-μs relaxation), and $\Delta V_{\rm TH}(ac)$ and $\Delta G_M(ac)$ are measures of the stress-induced degradation after a given relaxation time. Alternatively, a comparison of the (ab) and (ac) measurements is a measure of how much of the stress-induced degradation has recovered.

III. Results

Fig. 4 shows $\Delta V_{\rm TH}(ab)$ as a function of stress voltage (-1.2 to -2.7 V) for various stressing times (0.1–1000 s). Each data point in Fig. 4 represents a fresh device. We repeated the measurement sequence (Fig. 3) 12 times for the 0.1-, 1-, and 10-s stresses, 3 times for the 100-s stress, and 1 time for the 1000-s stress. Measurement repetition was used to improve the statistics for the shorter stresses which do not generate significant degradation. Clearly, the stress voltage plays a large role in the stress-induced $\Delta V_{\rm TH}$. Contrary to many recent reports [12]–[14], [16], no abnormally large $\Delta V_{\rm TH}$ is observed for moderate short-term stresses [29]. Even at $V_{\rm STRESS} = -1.8$ V, a level which is not exactly moderate, no measurable degradation is observed even after 1000 s. A large stress-induced $\Delta V_{\rm TH}$ is only observed for *exceedingly high* (< -1.8 V) stress voltages and longer stress times.

The steep rise in $\Delta V_{\rm TH}$ at $V_{\rm STRESS} < -1.8$ V, particularly after longer stress time, clearly suggests that there is a shift in the dominating degradation mechanism. We can make a crude conservative estimation of the dielectric field at -1.8 V by assuming the following: 1) an additional 0.4 nm of dielectric

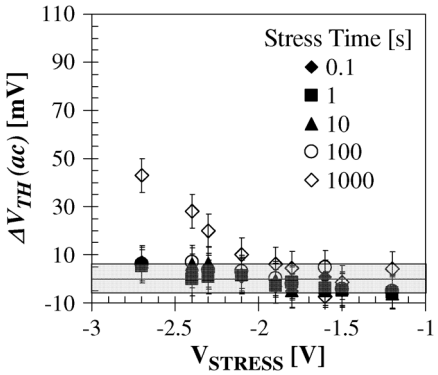

Fig. 5. $\Delta V_{\mathrm{TH}}(ac)$ (relaxed) as a function of gate stress voltage for various stress times in $2 \times 0.07\ \mu\mathrm{m}^2$ pMOSFETs at 125 °C. The relaxation time is 5 s. The measurement time is 2 μs. With the exception of the 1000-s stress, all of the stress-induced ΔV_{TH} is "relaxed." The box centered about 0 mV represents ± 1 standard deviation error bar.

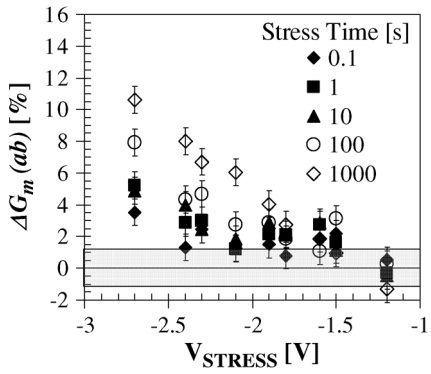

Fig. 6. Corresponding $\Delta G_M(ab)$ (stress induced) as a function of stress voltage for various stress times in $2 \times 0.07\ \mu\mathrm{m}^2$ pMOSFETs at 125 °C. The G_M degradation follows a similar trend (large degradations only at higher voltages) as seen in $\Delta V_{\mathrm{TH}}(ab)$ (Fig. 4). The measurement time is 2 μs. The box centered about 0% represents ± 1 standard deviation error bar.

thickness due to polydepletion; 2) an additional 0.4 nm of dielectric thickness due to quantum confinement; and 3) the realization that, with flatband voltage equal to 1 V and the threshold voltage equal to -0.3 V, there is approximately 0.3 V dropped across the dielectric with no applied bias. This estimate leads to a dielectric field of [(1.8 V + 0.3 V)/(1.6 nm + 0.4 nm + 0.4 nm)] $\approx$ 9 MV/cm. This is well above the 6-MV/cm boundary of traditional NBTI and is approaching fields which are considered too high even for high-field-stress TDDB studies [26]. Rapid gate dielectric degradation due to extreme high-field stress is a well-known phenomenon which has been reported in detail in the literature [26].

Fig. 5 shows the complementary $\Delta V_{\mathrm{TH}}(ac)$ as a function of gate bias for the same stress voltages and times as in Fig. 4 (relaxation time = 5 s). With the exception of the 1000-s stress at higher stress voltages, all other stress voltages and times show no measurable residual degradation or "permanent" ΔV_{TH}. Since both NBTI and high-field stress are known to have relaxation behavior, looking purely at the ΔV_{TH} is insufficient to differentiate the two mechanisms. After the 1000-s stress at higher V_{STRESS}, we observe residual degradation after 5 s of relaxation. This is likely due to increased interface state generation at these extreme stress conditions. High-field stress is known to generate interface states which are not known to recover significantly upon the removal of stress [26]. In contrast, NBTI reaction–diffusion models attribute relaxation to the recovery of the interface states after the stress is removed [17].

To further examine the V_{STRESS} dependence, we extracted the corresponding changes in the G_M characteristic curves [31]. Fig. 6 shows $\Delta G_M(ab)$ as a function of stress voltage and stress times. The $\Delta G_M(ab)$ trend mimics the $\Delta V_{\mathrm{TH}}(ab)$ trend (increased G_M degradation at higher stress voltages and longer stress times) and also exhibits a strong dependence on the stress voltage. Since both NBTI and high-field degradation mechanisms are known to degrade G_M, the observed dependence is as expected. However, an examination of the $\Delta G_M(ac)$ (postrelaxation) as a function of V_{STRESS} (relaxation time = 5 s) reveals a surprising result. As the stress voltage and stress duration increase, we observe negative $\Delta G_M(ac)$ values (Fig. 7). Negative $\Delta G_M(ac)$ is an indication that, after 5 s

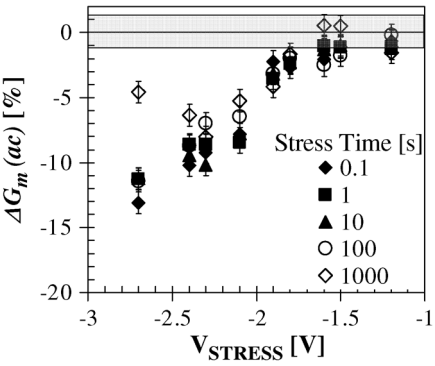

Fig. 7. $\Delta G_M(ac)$ (relaxed) as a function of stress voltage for various stress times in $2 \times 0.07\ \mu\mathrm{m}^2$ pMOSFETs at 125 °C. The relaxation time is 5 s. The measurement time is 2 μs. At higher gate voltages, we observe a surprising improvement in G_M to values better than prestress. We attribute this G_M improvement to an electron trapping/detrapping mechanism which is consistent with our high-field-stress hypothesis. The box centered about 0% represents ± 1 standard deviation error bar.

of relaxation, the measured peak G_M has improved to values which are greater than those before stress. The ability to observe this surprising result is unique to our measurement technique. We must point out that this is not the first observation of stress-induced G_M improvement [35]. In pure-SiO_2 pMOSFETs, poststress G_M improvement was attributed to the passivation of preexisting interface defects by atomic hydrogen [35]. In this scenario, the G_M improvement would be a permanent consequence of the repassivation. As will be shown later in this paper, our observed G_M improvement is a transient effect which diminishes at longer recovery times. This has led us to seek an alternate explanation which is outside of the common NBTI models.

IV. Discussion

The current literature hotly debates the identity of the NBTI mechanism. Degradation has been linked to interface state generation or hole trapping (or both) [36]. Relaxation is then explained by the annihilation of these interface states, the detrapping of the holes (or both) [36]. (Interface states biased in inversion and holes in the gate dielectric are both positively charged.) While the conflicting details of this debate are

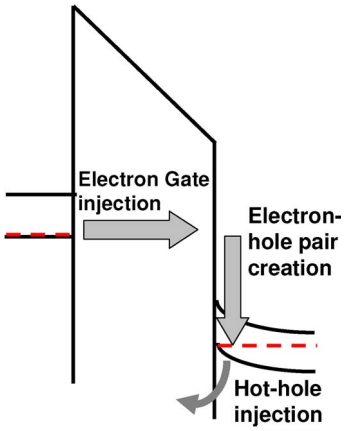

Fig. 8. Schematic illustration of how high-field stress generates an electron injection current through the gate which leads to impact ionization and a back injection of holes into the dielectric.

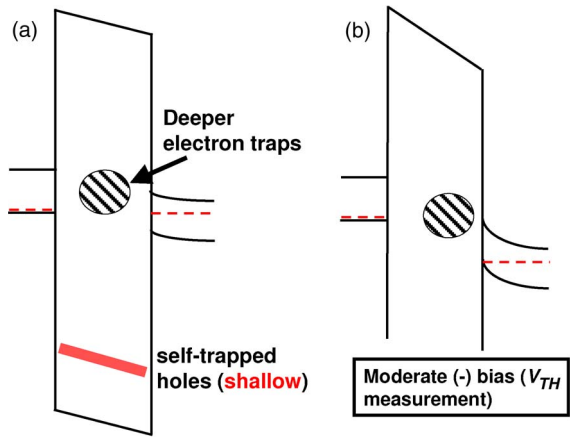

Fig. 9. (a) Schematic illustration of the suspected energy levels involved in electron and hole trapping. The majority of holes are self-trapped and are quite shallow while the electron-trapping sites are much deeper. (b) Schematic illustration of how the applied bias consistent with a $V_{\rm TH}$ measurement (moderate negative voltage) acts to accelerate electron detrapping.

voluminous, in all cases, NBTI is linked to an accumulation (degradation) and depletion (relaxation) of positive charge in the gate stack which shifts the $V_{\rm TH}$ to more negative values and degrades G_M due to increased Coulombic scattering. This positive-charge NBTI paradigm can be used to explain our observations in Figs. 4–6 (negative recoverable $\Delta V_{\rm TH}$ and G_M degradation). However, no combination of these positive-charge NBTI paradigms can explain our poststress G_M improvement observation (Fig. 7). G_M improvement is only possible if negative charges are also present in the form of trapped electrons. Where do these trapped electrons come from?

In the TDDB literature, high-field stress is known to trap both holes *and electrons* in the dielectric as well as generate interface states [37], [38]. At large negative gate biases, high levels of electrons can be injected into the gate dielectric. In nitrided gate dielectrics, significant densities of electron traps can exist in as-processed devices [39], [40]. These electron traps can capture electrons at the onset of stress—when electrons start flowing across the gate dielectric. The application of our stressing conditions to the ultrathin dielectrics used in this study induces a relatively high level of electron current across the gate dielectric (ensuring ample electron trapping) [41], [42]. Note that not all of the gate injected electrons get trapped in the dielectric, but some make it all the way to the substrate (Fig. 8). These gate injected electrons are hot when they reach the substrate and can help generate substrate hot holes (impact ionization). The hot holes can then back inject in the dielectric (trapped holes). The majority of the TDDB literature invokes a process quite similar to this to explain both hole *and electron* trapping with the application of high negative gate biases. As aforementioned, the majority of our measurable $\Delta V_{\rm TH}$ and ΔG_M observations occur at fields $\geq$ 9 MV/cm, putting them squarely in the high-field-stress territory [26] where we should expect both trapped holes and electrons. The addition of an electron-trapping component provides us with an explanation to the collective observations (Figs. 4–7) including the postrelaxation G_M improvement.

A possible explanation of our observations is as follows: In the stress phase, hole *and electron* trapping take place in the gate dielectric as well as the generation of interface states. At the conclusion of stress, the net positive charge associated with the trapped holes and the interface states collectively dominates the negative charge due to the trapped electrons. This results in a negative $\Delta V_{\rm TH}$ and a degraded peak G_M (Figs. 4 and 6). During relaxation, both holes and electrons detrap but at different rates (holes detrap faster than electrons) [43]–[45]. After 5 s of relaxation, the holes are largely detrapped while electron detrapping is still incomplete. The net negative charge due to the electrons can compensate the positively charged interface states and effectively reduce the Coulombic scattering and improve G_M.

From high-field-stress literature, we know that the majority of hole trapping is self-induced (self-trapped hole) with a shallow trap depth of $\approx$1.4 eV [Fig. 9(a)] [46], [47]. These self-trapped holes are also efficiently detrapped. During stress, hole trapping and detrapping occur simultaneously which quickly establishes a steady state. After the stress is removed, the efficient detrapping quickly removes the self-trapped holes from the dielectric. Electron trapping at defect sites is likely far less efficient even though the electron flux is orders of magnitude higher than the hole flux. During stress, electron trapping also reaches a steady state quickly, although this level can increase over time due to the generation of additional electron traps. After the stress is removed, it is quite likely that electron detrapping is less efficient because electron traps are much deeper in energy [40], [48]. We note that the $V_{\rm TH}$ measurement itself (application of low negative voltage) should act to accelerate electron detrapping [Fig. 9(b)]. Together, the shallow self-trapped holes and the deeper trapped electrons make for an obscured charge trapping/detrapping dynamic which is difficult to deconvolute.

However, if the aforementioned scenario is true, we can take advantage of the fact that electrons and holes detrap at different rates to further test the validity of our assumptions and deconvolute the electron and hole trapping/detrapping dynamics. To accomplish this goal, we must be able to tightly control our relaxation time down to the microsecond regime. This is experimentally realized by using a slightly modified

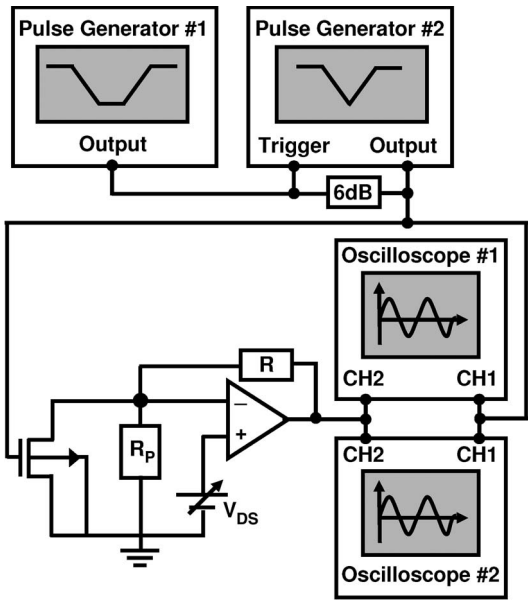

Fig. 10. Slightly modified (from Fig. 1) fast-I_DV_G experimental setup utilized to capture $V_{\rm TH}$ and G_M relaxation very quickly (2 μs) after stress removal. The modification involves the addition of a second pulse generator and oscilloscope. In this approach, the first pulse generator/oscilloscope pair captures the stress pulse, while the second pair captures the postrelaxation pulse. Synchronization of these two pairs allows for very tight control of the measured relaxation time.

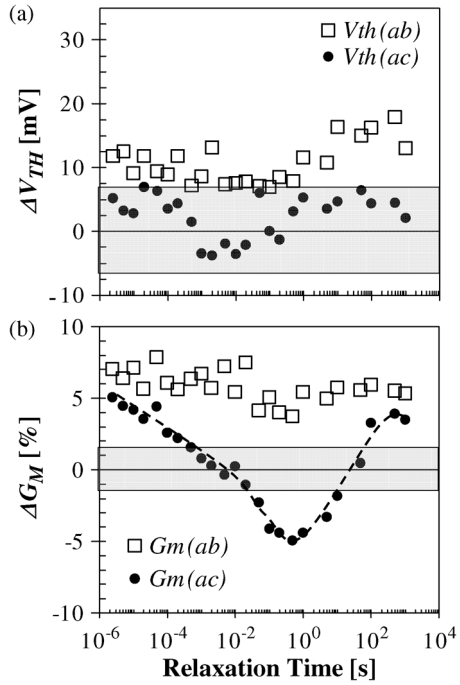

Fig. 11. Stress-induced and relaxed $\Delta V_{\rm TH}$ and ΔG_M as a function of relaxation time for $2 \times 0.06\ \mu{\rm m}^2$ pMOSFETs subject to stress of -2.5 V for 10 s at 125 °C. Each pair of data points represents a fresh device. The measurement time is 2 μs. (a) Stress-induced $\Delta V_{\rm TH}(ab)$ is just slightly larger than the error of the measurement and relaxes ($\Delta V_{\rm TH}(ac)$) very quickly to values within the measurement error. (b) Corresponding stress-induced $\Delta G_M(ab)$ exhibits a similar degradation trend; however, the relaxed $\Delta G_M(ac)$ is a strong function of relaxation time. As the relaxation time increases, $\Delta G_M(ac)$ transitions from degradation to improvement and then back to degradation. The boxes centered about 0 mV and 0% represent ± 1 standard deviation error bars.

measurement apparatus which includes an additional pulse generator and digital oscilloscope (Fig. 10). The additional pulse generator/oscilloscope pair is required to avoid the finite time required to, first, switch the pulse generator from the stress to the postrelaxation pulse and, second, to switch the oscilloscope trigger edge. In the modified approach, the first pulse generator/oscilloscope pair is programmed to only capture the pre- and poststress waveforms and the second pulse generator/oscilloscope pair is programmed to only capture the postrelaxation waveforms (via a trigger offset). A 6-dB attenuator was also used to provide added triggering headroom between the two pulse generators (one pulse generator has a higher trigger threshold than the other). Careful synchronization of the two pulse generator/oscilloscope pairs allows us to make the first relaxation measurements 2 μs after stress has ended while simultaneously controlling the long relaxation time (up to 1000 s). This allows for both $\Delta V_{\rm TH}$ and ΔG_M measurements as a function of relaxation time.

Fig. 11(a) shows $\Delta V_{\rm TH}(ab)$ and $\Delta V_{\rm TH}(ac)$ as a function of relaxation time for devices that were subject to a stress of -2.5 V at 125 °C for 10 s. $\Delta V_{\rm TH}(ab)$, as expected, is invariant of relaxation time and is shown only as a reference. As before, each data point represents a fresh device and is the average of 12 successive measurement sequences. This relatively short stress results in a moderate $\Delta V_{\rm TH}$ (just above the error of our measurement) which recovers to values within the error of our measurement very quickly after the stress is removed. However, the corresponding $\Delta G_M(ab)$ and $\Delta G_M(ac)$ responses reveal a dramatic transient behavior [Fig. 11(b)]. The $\Delta G_M(ab)$ is, as expected, invariant of the relaxation time and is again shown only as a reference. However, $\Delta G_M(ac)$ is a strong function of relaxation time. At very short relaxation times (2 μs), $\Delta G_M(ac)$ exhibits degradation. As relaxation time increases, $\Delta G_M(ac)$ decreases and transitions to negative values. This corresponds to postrelaxation peak-G_M values *better* than the prestress measurement. At longer relaxation times, $\Delta G_M(ac)$ reaches a minimum (maximum improvement) and turns around toward the positive initial degradation values. The full relaxation time dependence is also consistent with the snapshot of our 5-s relaxation observations (Fig. 7).

The observed G_M improvement, albeit brief, is a further confirmation of our earlier results and is completely consistent with our high-field induced electron trapping/detrapping hypothesis. The conclusion of stress leaves the device with increased interface states and both trapped holes and electrons [Fig. 12(a)]. The combination of trapped holes and interface states again overwhelms the trapped electrons, and we observe a net increase in positive charge and Coulombic scattering ($\Delta G_M(ac)$) degradation at short relaxation times. As the relaxation time increases, the hole concentration decreases, which reduces the number of Coulomb scattering centers. This leads to a reduction in $\Delta G_M(ac)$. This process continues until the trapped holes are largely depleted, leaving only the trapped electrons in the bulk [Fig. 12(b)]. The net positive charge is now at a minimum. If the net positive charge is less than the amount before stress (due to as-processed interface states), the peak G_M will improve, as is the case for $\Delta G_M(ac)$ in Fig. 11(b). At longer relaxation times, the electrons eventually also detrap, leaving only positively charged interface states, and $\Delta G_M(ac)$

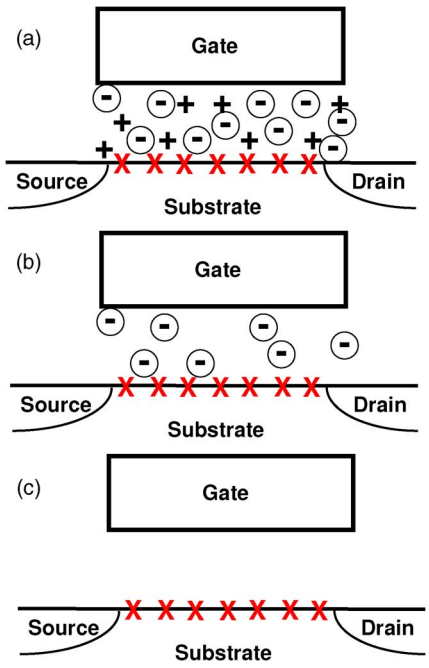

Fig. 12. Schematic representation of the charge dynamics during relaxation. (a) Immediately after stress, the gate stack consists of interface states (positively charged in inversion), trapped holes, and trapped electrons. (b) As relaxation continues, the holes detrap first, leaving only trapped electrons and interface states. The trapped electrons are now in a position to Coulombically screen the positively charged interface states and improve G_M. (c) Finally, at longer relaxation times, the electrons also detrap, leaving only interface states, and G_M returns to degradation.

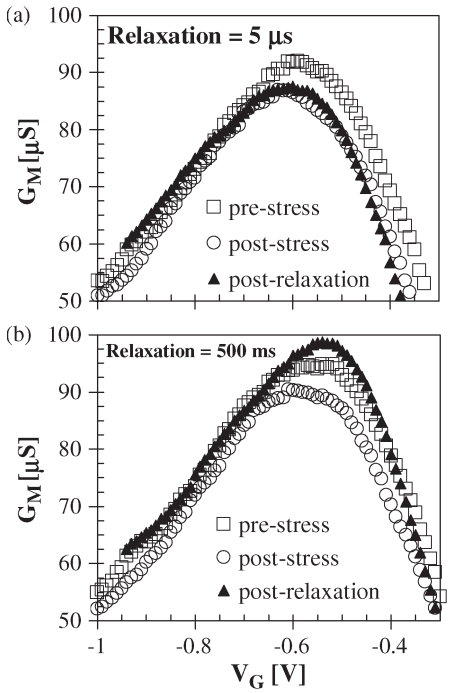

Fig. 13. Prestress, poststress, and postrelaxation $G_M{-}V_G$ characteristics for 2×0.06 μm^2 pMOSFETs subject to stress of -2.5 V for 10 s at 125 °C. The measurement time is 2 μs. (a) At 5 ms, we observe postrelaxation correspondence between $\Delta V_{\rm TH}(ac)$ and $\Delta G_M(ac)$ in the earlier degradation. At 500 ms, we observe postrelaxation improvement.

returns to degradation [Fig. 12(c)]. For completeness, the prestress, poststress, and postrelaxation $G_M{-}V_G$ characteristic curves are shown in Fig. 13(a) for 5-μs relaxation (peak-G_M degradation) and in Fig. 13(b) for 500-ms relaxation (peak-G_M improvement). These results confirm our assumptions of an electron trapping/detrapping component. While reports linking G_M improvement to electron trapping are rare, they are not without precedent. Charpenel et al., for example, observed G_M improvement after injecting electrons into the gate dielectric [49]. Additionally, Weber et al. suggest that trapped electrons could effectively "tie up" interface states and prevent them from charging or discharging [50].

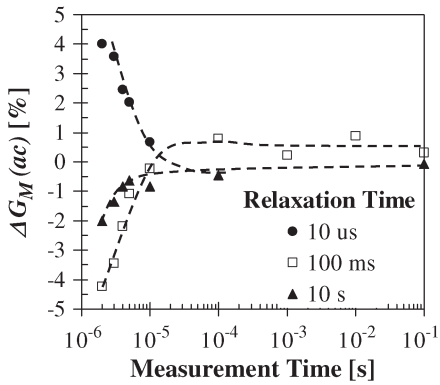

Fig. 14. $\Delta G_M(ac)$ as a function of measurement time (rise and fall time) for 2×0.07 μm^2 pMOSFETs subject to an NBTI stress of -2.5 V for 10 s at 125 °C. G_M degradation/improvement is only observable for measurement times < 10 μs. The lines are only a guide for the eye.

Further evidence supporting our high-field-stress electron trapping/detrapping argument stems from the fact that G_M improvement is only observable when the measurement time is sufficiently fast. Fig. 14 shows $\Delta G_M(ac)$ as a function of measurement time (rising/falling time of the gate pulse) for various relaxation times. Depending on the relaxation time, $\Delta G_M(ac)$ exhibits improvement or degradation. Clearly, this transient G_M behavior is only observable when the measurement time is less than 10 μs. The need for very fast measurements is due to the fact that the formation of an inversion layer of holes will neutralize any trapped electrons via tunneling [44]. Since the gate dielectric is only 1.6 nm thick, the tunneling front rapidly reaches the trapped electrons [44]. Thus, fast-I_DV_G measurements provide a small experimental window where G_M improvement is observable. In slower I_DV_G measurements, the inversion layer holes are given sufficient time to neutralize the trapped electrons (tunneling) and the G_M transients vanish.

With regard to Fig. 11, one might wonder why there is little correspondence between the $\Delta V_{\rm TH}(aC)$ and $\Delta G_M(ac)$ measurements. We believe that this is a simple problem of low signal-to-noise ratio (i.e., the $\Delta V_{\rm TH}$ generated is relatively small) and any variation is buried within the error of our experiment. In an effort to increase the magnitude of $\Delta V_{\rm TH}(ac)$, the experiment of Fig. 11 was repeated using a harsher stress condition (-2.7 V at 125 °C for 1000 s). Fig. 15(a) shows $\Delta V_{\rm TH}(ab)$ and $\Delta V_{\rm TH}(ac)$ and Fig. 15(b) shows $\Delta G_M(ab)$ and $\Delta G_M(ac)$ as a function of relaxation time. Similarly to Fig. 11, $\Delta V_{\rm TH}(ab)$ and $\Delta G_M(ab)$ are only shown as a reference. Since this harsher stress very likely introduces a permanent degradation, no averaging was used for these measurements. In this case, we note that the magnitude of the $\Delta V_{\rm TH}$

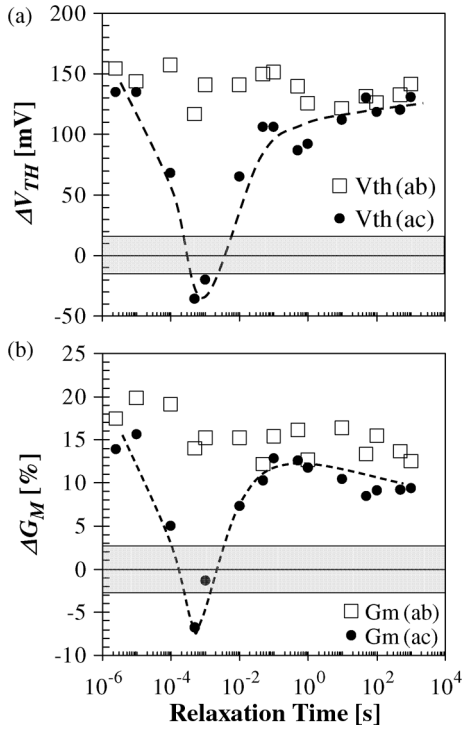

Fig. 15. Stress-induced and relaxed $\Delta V_{\rm TH}$ and ΔG_M as a function of relaxation time for 2×0.07 μm^2 pMOSFETs subject to stress of -2.7 V for 1000 s at 125 °C. Each pair of data points represents a fresh device. The measurement time is 2 μs. For this harsher stress condition, the $\Delta V_{\rm TH}(ac)$ trend in (a) mimics the $\Delta G_M(ac)$ trend in (b). The boxes centered about 0 mV and 0% represent ± 1 standard deviation error bars.

is large enough to easily be resolved by our measurements and exhibits a relaxation dependence $\Delta V_{\rm TH}(ac)$ which tracks quite well with the $\Delta G_M(ac)$ relaxation dependence. Thus, the lack of correspondence between $\Delta V_{\rm TH}(ac)$ and $\Delta G_M(ac)$ in the earlier measurements (Fig. 11) is very likely due to our measurement resolution. However, an important consequence of this "check" experiment is that the G_M turnaround now occurs at a much shorter relaxation time. This suggests that both holes and electrons detrap much faster. The perceived faster hole detrapping may be due to a much higher trapped hole concentration or may simply be a consequence of faster electron detrapping which obscures the actual hole detrapping. It is even possible that the hole detrapping rate may not have changed. However, the faster electron detrapping is, without question, real. It is difficult to explain why a harsher stress would increase the electron detrapping rate if the electrons detrap to either the conduction or valence bands. (The harsher stress should have no effect.) However, the harsher stress would likely generate more interface states. This leads us to the conclusion that the electron detrapping must be assisted by interface states and that the electrons must detrap to the substrate, not the gate electrode. This implies that the electron traps are indeed very deep. This also implies that electron detrapping is dependent on stress history. Longer stress produces higher interface state density and faster electron detrapping. Furthermore, from device to device, the electron detrapping time, or the transient behavior of G_M, will likely vary significantly.

The evidence of electron trapping/detrapping strongly supports the conclusion that the $V_{\rm STRESS} < -1.8$ V data in Fig. 4 is dominated by high-field stress. It also conclusively shows that the presence of a high-field-stress mechanism affects many recent NBTI reports that utilize extreme accelerated stress voltages. While determination of the boundary between low- and high-field stress is nontrivial, it is quite clear from earlier NBTI carrier separation experiments [51] as well as TDDB observations that 10 MV/cm very likely represents a high-field accelerated stress which can invoke extraneous degradation mechanisms [23]. What we found here should be expected. What is surprising is that so much effort has been spent trying to explain recent (high-field) NBTI experiments within the traditional reaction–diffusion NBTI framework [22], [27].

Since the operation field for advanced devices has already surpassed 6 MV/cm, it is entirely reasonable to use higher fields to accelerate NBTI stress. Thus, the avoidance of high-field stress is becoming less practical. However, one must account for the contribution of high-field stress to NBTI to ensure accurate NBTI lifetime projections. Additionally, the net dominance of each mechanism is likely dependent on device processing and circuit environment (ac/dc). Thus, the proper choice of stress conditions and measurement technique is no longer trivial.

V. Conclusion

We have presented a fast-$I_D V_G$ measurement methodology which supports standard $\Delta V_{\rm TH}$ extraction (linear extrapolation at maximum G_M). This technique enables the dynamics of NBTI degradation and relaxation to be studied in detail. The observed $\Delta V_{\rm TH}$ and ΔG_M clearly reveal an accelerated degradation at exceedingly high gate voltages. It is shown that these voltages, which are commonly used in NBTI characterizations, introduce an additional high-field-stress degradation mechanism which is inconsistent with the lower field NBTI phenomenon. The dominance of the high-field-stress mechanism is supported by the surprising observation of a postrelaxation G_M improvement. This G_M improvement is attributed to an electron trapping/detrapping component which is a known characteristic of high-field stress.

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