Large Random Telegraph Noise in Sub-Threshold Operation of Nano-Scale nMOSFETs

J.P. Campbell[1], L.C. Yu[1,2], K.P. Cheung[1*], J. Qin[1,3], J.S. Suehle[1], A. Oates[4], K. Sheng[2]
[1]Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD 20899 *kpckpc@ieee.org
[2]Department of Electrical and Computer Engineering, Rutgers University, Piscataway, NJ 08854
[3]Departmemt of Mechanical Engineering, University of Maryland, College Park, MD 20740
[4]TSMC Ltd., Hsin-Chu, Taiwan 300-77, R.O.C.

***Abstract*--We utilize low-frequency noise measurements to examine the sub-threshold voltage (sub-V_{TH}) operation of highly scaled devices. We find that the sub-V_{TH} low-frequency noise is dominated by random telegraph noise (RTN). The RTN is exacerbated both by channel dimension scaling and reducing the gate overdrive into the sub-V_{TH} regime. These large RTN fluctuations greatly impact circuit variability and represent a troubling obstacle that must be solved if sub-V_{TH} operation is to become a viable solution for low-power applications.**

***Keywords*—RTN, Sub-V_{TH} operation**

I. Introduction

Traditional device scaling focuses on a balance between performance and power consumption. However, the emergence of power-sensitive products (cell phones, pacemakers, implantable devices) has led to the exploration of circuits which operate in the sub-threshold voltage (sub-V_{TH}) regime [1]. The sub-V_{TH} paradigm sacrifices a small amount of performance for a comparatively huge power reduction (~V_G^2) while maintaining the benefits of scaling [2] . Quite recently, this sub-V_{TH} approach has been experimentally realized in prototype microprocessors and SRAM arrays [3, 4]. However, the benefits of sub-V_{TH} scaling do not come without penalty. Since sub-V_{TH} operation reduces device drive current, circuits become significantly less tolerant of noise [2]. While several recent reports detail clever approaches to combat this noise intolerance [2, 3, 5], they do not account for the possibility of large noise increases as device dimensions continue to scale. Specifically, in nano-scaled devices a particularly troubling noise phenomenon called random telegraph noise (RTN) [6] has the potential to severely limit sub-V_{TH} circuit design. RTN is a digital fluctuation in device drain current (I_D) which has already been identified as a large obstacle in *super-V_{TH}* operation of both SRAM and FLASH memory technologies [7-9]. However, the impact of RTN on sub-V_{TH} operation is only sporadically debated in the literature with very little consensus. Some researchers report a $\Delta I_D/I_D$ inverse channel length dependence (1/L) [10] while others report a more pessimistic $1/L^2$ dependence [11, 12]. Some researchers report no dependence on channel width (W) [11] while others report a $1/\sqrt{W}$ dependence [13]. However, most of these reports focus on larger channel area devices with particular emphasis on the super-V_{TH} regime. Asenov *et al.* was the first to report simulations of highly-scaled devices [13, 14]. These simulations predict an enhanced $\Delta I_D/I_D$ RTN in the sub-V_{TH} regime. If this enhancement were to be experimentally observed, the implication to sub-V_{TH} circuits would be serious. Surprisingly, there is almost no experimental evidence to examine the validity of this prediction.

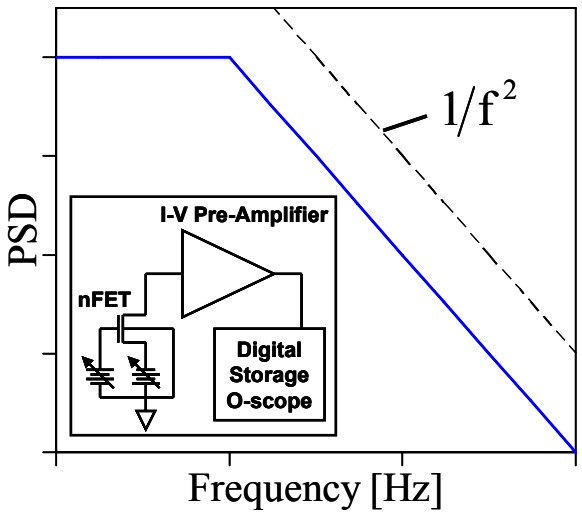

Figure 1. Schematic illustration of the power spectral density (PSD) of an RTN fluctuation (Lorentzian line shape with slope $1/f^2$). The schematic representation of our experimental approach is shown in the inset.

In this paper we present low-frequency noise characteristics of highly-scaled nMOSFETs as a function of gate overdrive (V_G-V_{TH}) for a variety of channel lengths and widths. As expected, reduction of the channel dimensions reveals a noise mechanism dominated by RTN. This RTN is largest in the sub-V_{TH} regime and reduces as the gate-overdrive is increased to super-V_{TH} values. We also note the presence of occasional giant $\Delta I_D/I_D$ RTN in a small number of the most highly scaled devices. Our collective observations represent a grim outlook for the viability of sub-V_{TH} circuit scaling and identify RTN as a topic which merits further attention.

II. Experimental Methods

Our experiments utilize silicon oxynitride (SiON) n-channel MOSFET devices with a physical dielectric thickness of 1.4 nm. The nominal channel widths ranged from 0.085 μm to 1 μm and the nominal channel lengths ranged from 0.055 μm to 1 μm. The RTN measurement apparatus is schematically illustrated in the inset of fig. 1. Source and gate electrodes are biased using battery-powered variable voltage sources, while the substrate electrode is grounded for all measurements. The drain current is monitored by a low-noise

978-1-4244-2934-9/09/$25.00 ©2009 IEEE

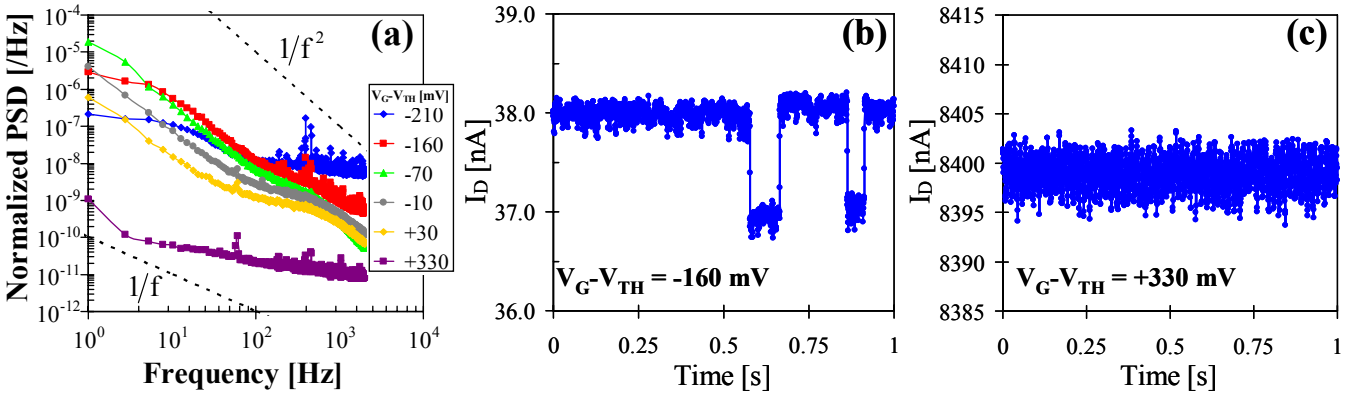

Figure 2. Noise characteristics from a 0.090 x 0.055 μm² nMOSFET as a function of gate overdrive. The normalized PSD (a) exhibits a large increase in noise around the threshold voltage with the most significant noise in the sub-V_{TH} regime. The corresponding time series data in the sub-V_{TH} region (b) is dominated by RTN and the super-V_{TH} region (c) is dominated by 1/f noise.

current amplifier with 2 kHz bandwidth. The amplifier output is directly captured using a digital storage oscilloscope with a large memory depth (10^7 Samples). This time series data is then analyzed offline. The noise response is often reported asthe power spectral density (PSD) in the frequency domain. In our measurements, the PSD is normalized to the drain current to allow for meaningful comparisons as a function of gate overdrive. In the absence of RTN, the normalized PSD should yield a noise spectrum that goes as 1/f (flicker noise) [15]. However, the presence of RTN fluctuations in the time domain results in a Lorentzian PSD spectrum with slope $1/f^2$ in the frequency domain (fig. 1) [15]. These normalized PSD spectra, along with the extracted drain current variation ($\Delta I_D/I_D$), are used throughout the rest of this manuscript to examine variously scaled devices at an array of gate overdrives in the sub-V_{TH} and super-V_{TH} regimes. All measurements were performed at room temperature with the source electrode fixed at -50 mV.

III. Results And Discussion

Fig. 2 illustrates the noise response for a 0.09x 0.055 μm² nMOSFET. The noise response in this device is representative of many devices measured in this study and also provides an illustrative data set to clearly explain our observations. Fig. 2a shows the normalized PSD as a function of gate-overdrive. We note that the low-frequency noise is much larger sub-V_{TH} with the largest values observed at sub-V_{TH} gate-overdrives closer to V_{TH}. At super-V_{TH} gate overdrives, the low frequency noise is considerably less. We also note that the sub-V_{TH} and super-V_{TH} noise characteristics are quite different. With the exception of the lowest gate overdrive, all other sub-V_{TH} overdrives exhibit a Lorentzian PSD with slope close to $1/f^2$. This is an indication that the noise is dominated by RTN [15].

Further evidence of a sub-V_{TH} noise mechanism dominated by RTN and a super-V_{TH} noise mechanism closer to 1/f is seen in the corresponding time series data (fig. 2b and fig. 2c respectively). Curiously, the lowest gate-overdrive PSD is also quite large, but has a slope much closer to 1/f. The mechanism which causes 1/f to dominate at the lowest gate overdrives is still unknown and is currently under investigation.

Fig. 3 shows the normalized PSD as a function of gate overdrive for three different devices. Together (figs. 3a, 3b, and 3c) they demonstrate some generally observed behavior of the noise as a function of the channel dimensions and gate overdrive. It is clear that a restriction on the channel length or width increases the observed low-frequency noise and that this increase is dominated by RTN ($1/f^2$ slope). For short channel devices (figs. 3a and 3b), RTN is the dominant mechanism with larger values in the sub-V_{TH} regime. For narrow width devices (figs. 3b and 3c), the noise is less significant for longer channel lengths, but is still quite large for sub-V_{TH} overdrives. We note that we are somewhat limited in our

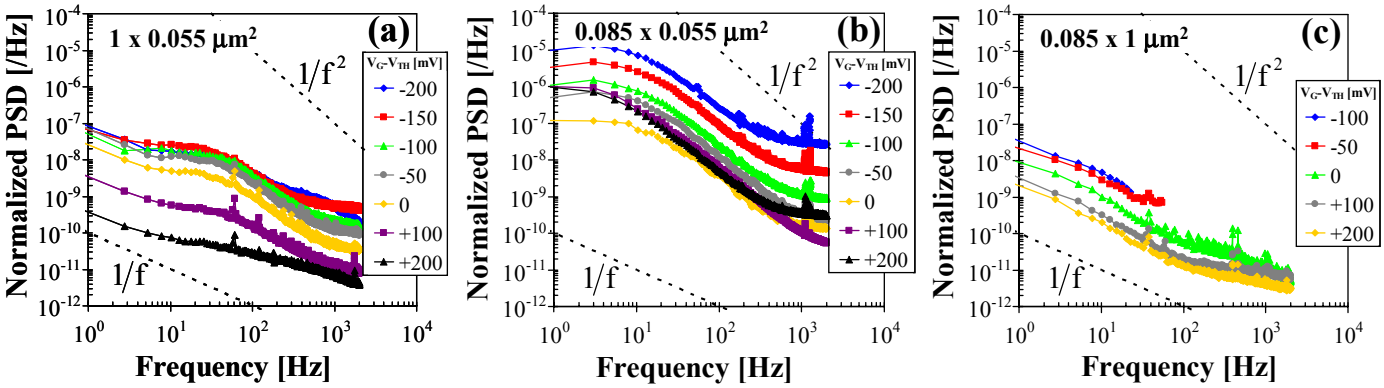

Figure 3. Normalized PSD as a function of gate overdrive for channel width (W) x length (L) of (a) 1 x 0.055 μm², (b) 0.085 x 0.055 μm². and (c) 0.085 x 1 μm².

978-1-4244-2934-9/09/$25.00 ©2009 IEEE

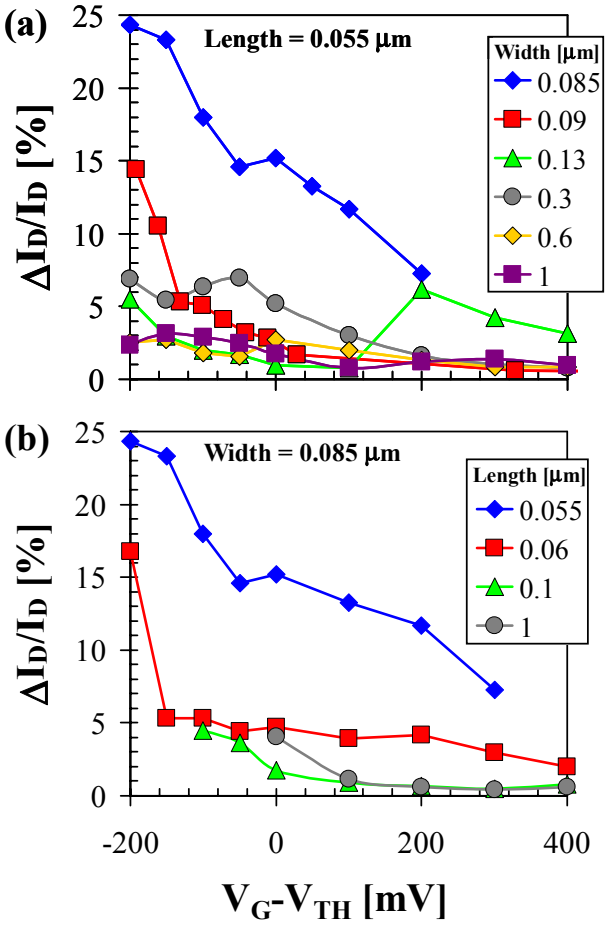

Figure 4. RTN amplitude ($\Delta I_D/I_D$) as a function of gate overdrive for various (a) channel widths and (b) channel lengths. Sub-V_{TH} RTN increase as the channel length and width are reduced

observations in fig 3c since the longer channel device yields much lower sub-V_{TH} noise which limits our measurement resolution. The general observation from fig. 3 is that the largest noise is observed sub-V_{TH} and that in most cases this sub-V_{TH} noise is dominated by RTN.

A more systematic study of the channel length, width, and gate overdrive dependencies on the magnitude of RTN is shown in fig. 4. Here we directly show the RTN amplitude ($\Delta I_D/I_D$) instead of the PSD to more clearly illustrate these dependencies. In fig. 4a, it is clear that the RTN noise increases rapidly as the overdrive decreases and reaches as high as $\Delta I_D/I_D \approx 25\%$ for the device with the shortest channel width. This same trend (dominant sub-V_{TH} low frequency noise) is also observed in fig. 4b for the device with the narrowest channel length ($\Delta I_D/I_D \approx 25\%$). These RTN fluctuations are somewhat larger than predicted [14], but the basic trend of increased sub-V_{TH} noise as the channel dimensions are reduced is in agreement with the simulations.

Further analysis of fig. 4 allows us to extract channel length and width dependencies. Unfortunately, we observe inconsistent sub-V_{TH} and super-V_{TH} trends ($L^{-0.5}$ to $L^{-1.5}$ and $W^{-0.5}$ to W^{-1}). This large variation is likely and indicator of (1) the "random" nature of the noise phenomenon and (2) the possibility that neither number nor mobility fluctuations completely dominate the noise characteristics [12].

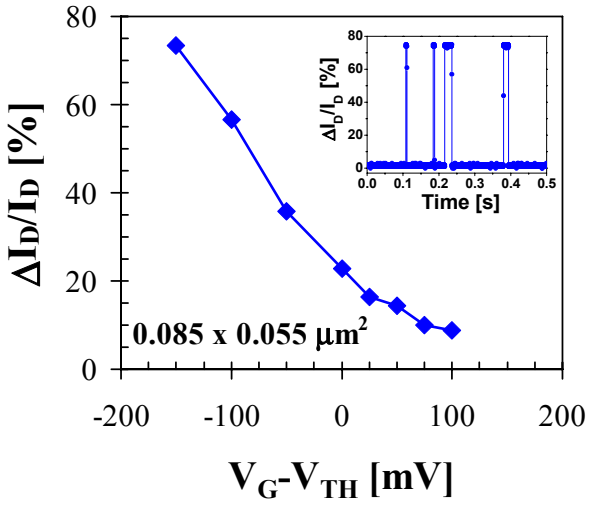

Figure 5. Large RTN amplitude ($\Delta I_D/I_D$) as a function of gate overdrive for an additional 0.085 x 0.055 µm^2 nMOSFET. The time series data for V_G-V_{TH} = -150 mV is shown in the inset for completeness.

Our observations (sub-V_{TH} $\Delta I_D/I_D \approx 25\%$) provide a troubling outlook for sub-V_{TH} operation in highly scaled devices. This variability seriously impacts advance circuit designs and must be minimized in order to continue scaling in the sub-V_{TH} regime [2]. Unfortunately, the origin of these large RTN fluctuations is still unknown. Early reports linked RTN to both bulk dielectric defects and/or interface state defects [16, 17]. While the mitigation of both bulk dielectric and interface state defects is always good practice, it is unclear which type of defect should receive the most attention. More importantly, it is possible that careful minimization of intrinsic defect densities will still eventually lead to a large variability in highly scaled devices. This notion is even more alarming with the realization that we occasionally observe extremely large sub-V_{TH} RTN characteristics ($\Delta I_D/I_D \approx 75\%$) in some of the most highly scaled (0.085 x 0.055 µm^2) devices (fig. 5). It has been proposed that these occasional large sub-V_{TH} RTN fluctuations are due to the random position of discrete dopant atoms [13, 14]. In a highly scaled device, the "unlucky" placement of a dopant atom can reduce the effective channel dimensions such that the RTN-induced Coulombic scattering has a much larger effect. The chance occurrence of a dopant-induced large RTN is unfortunately finite and inescapable in highly-scaled devices. These large fluctuations induce an impossibly large device variability that must be solved if sub-V_{TH} circuit operation with highly-scaled devices is to become a viable approach.

IV. Conclusions

We have examined the low-frequency noise characteristics in highly-scaled devices as a function of gate-overdrive. Our observations reveal that as the channel dimensions are reduced (length and/or width), the low-frequency noise becomes dominated by large RTN. These large RTN characteristics are exacerbated in the sub-V_{TH} regime. We also note the occasional observation of giant RTN fluctuations ($\Delta I_D/I_D \approx$

978-1-4244-2934-9/09/$25.00 ©2009 IEEE

75%). These collective observations provide a grim outlook for sub-V_{TH} nano-scaled devices.

V. Acknowledgments

The authors acknowledge funding from the NIST Office of Microelectronic Programs. J.P.C also acknowledges funding support by the National Research Council.

VI. References

[1] S. Hanson, B. Zhai, K. Bernstein, D. Blaauw, A. Bryant, L. Chang, K. K. Das, W. Haensch, E. J. Nowak, and D. M. Sylvester, "Ultralow-voltage, minimum-energy CMOS" *Ibm J Res Dev,* **50**, pp. 469-490 (2006)

[2] S. Hanson, M. Seok, D. Sylvester, and D. Blaauw, "Nanometer device scaling in subthreshold logic and SRAM" *IEEE Trans. Electron Dev,* **55**, pp. 175-185 (2008)

[3] I. J. Chang, J. J. Kim, S. P. Park, and K. Roy, "A 32 KB 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS" *IEEE J. Solid-St Circ,* **44**, pp. 650-658 (2009)

[4] J. Kwong, Y. Ramadass, N. Verma, M. Koesler, K. Huber, H. Moormann, and A. Chandrakasan, "A 65nm Sub-V_t Microcontroller with Integrated SRAM and Switched-Capacitor DC-DC Converter" *Proc. of the IEEE International Solid-State Circuits Conference* pp. 318-319, 616 (2008)

[5] B. H. Calhoun and A. P. Chandrakasan, "Static noise margin variation for sub-threshold SRAM in 65-nm CMOS" *IEEE J. Solid-St Circ,* **41**, pp. 1673-1679 (2006)

[6] K. S. Ralls, W. J. Skocpol, L. D. Jackel, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, "Discrete Resistance Switching in Submicrometer Silicon Inversion-Layers - Individual Interface Traps and Low-Frequency (1-F Questionable) Noise" *Phys Rev Lett,* **52**, pp. 228-231 (1984)

[7] P. Fantini, A. Ghetti, A. Marinoni, G. Ghidini, A. Visconti, and A. Marmiroli, "Giant Random Telegraph Signals in Nanoscale Floating-Gate Devices" *IEEE Electron Device Lett.,* **28**, pp. 1114-1116 (2007)

[8] H. Kurata, K. Otsuga, A. Kotabe, S. Kajiyama, T. Osabe, Y. Sasago, S. Narumi, K. Tokami, S. Kamohara, and O. Tsuchiya, "Random Telegraph Signal in Flash Memory: Its Impact on Scaling of Multilevel Flash Memory Beyond the 90-nm Node" *IEEE J. Solid-St Circ,* **42**, pp. 1362-1369 (2007)

[9] N. Tega, H. Miki, M. Yamaoka, H. Kume, M. Toshiyuki, T. Ishida, M. Yuki, R. Yamada, and T. Kazuyoshi, "Impact of Threshold Voltage Fluctuation Due to Random Telegraph Noise on Scaled-Down SRAM" *IEEE Int. Rel. Phys. Symp.* pp. 541-546 (2008)

[10] E. Simoen and C. Claeys, "Gate Length Effect on the RTS Noise Amplitude in SOI MOSFET's" *IEEE Electron Device Lett.,* **17**, pp. 181-183 (1996)

[11] S. T. Martin, G. P. Li, E. Worley, and J. White, "The Gate Bias and Geometry Dependence of Random Telegraph Signal Amplitudes" *IEEE Electron Device Lett.,* **18**, pp. 444-446 (1997)

[12] M. H. Tsai and T. P. Ma, "The Impact of Device Scaling on the Current Fluctuations in Mosfets" *IEEE Trans. Electron Dev,* **41**, pp. 2061-2068 (1994)

[13] A. Asenov, R. Balasubramaniam, A. R. Brown, J. H. Davies, and S. Saini, "Random Telegraph Signal Amplitudes in Sub-100 nm (Decanano) MOSFETs: a 3D `Atomistic' Simulation Study" *IEEE Int. Electron. Dev. Meeting* pp. 279-282 (2000)

[14] A. Asenov, R. Balasubramaniam, A. R. Brown, and J. H. Davies, "RTS Amplitudes in Decananometer MOSFETs: 3-D Simulation Study" *IEEE Trans. Electron Dev,* **50**, pp. 839-845 (2003)

[15] M. J. Kirton and M. J. Uren, "Noise in Solid-State Microstructures - A New Perspective on Individual Defects, Interface States and Low-Frequency (1/F) Noise" *Adv Phys,* **38**, pp. 367-468 (1989)

[16] K. K. Hung, P. K. Ko, C. M. Hu, and Y. C. Cheng, "A Unified Model for the Flicker Noise in Metal Oxide-Semiconductor Field-Effect Transistors" *IEEE Trans. Electron Dev,* **37**, pp. 654-665 (1990)

[17] A. Ohata, A. Toriumi, M. Iwase, and K. Natori, "Observation of Random Telegraph Signals - Anomalous Nature of Defects at the Si/SiO_2 Interface" *J Appl Phys,* **68**, pp. 200-204 (1990)

978-1-4244-2934-9/09/$25.00 ©2009 IEEE