

Constraint effect in deformation of copper interconnect lines subjected to cyclic Joule heating

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The manuscript was received on 19 February 2009 and was accepted after revision for publication on 27 May 2009.

DOI: 10.1243/03093247JSA532

Abstract: Temperature distributions and von Mises strains produced by cyclic Joule heating of damascene copper interconnect structures of varying geometries were calculated by finite element analysis. Constraining the top surface of the lines with rigid dielectric increased the temperature range required to produce a given strain range, relative to unconstrained lines. Much narrower lines required much higher temperatures to reach this same range of strain. Electrical tests to failure of actual structures were conducted. Scanning electron microscope images of unconstrained damascene copper lines after testing showed significant topographic features that have been associated in previous reports with mechanical fatigue. None of the constrained lines – including those cycled at ranges of total strain similar to those of the unconstrained lines – exhibited these features, but they did have large voids. Present and previously reported observations suggest that both cyclic plastic deformation and void formation can contribute to damage and failure of small-scale structures subjected to cyclic Joule heating, and that mechanical constraint has a strong effect on the operation of these mechanisms.

Keywords: alternating current, damascene, fatigue, lifetime, reliability, strain, voids

1 INTRODUCTION

Interconnect structures are a critical component of the ultra-large-scale integration (ULSI) semiconductor ‘chips’ that power digital electronic devices from cell telephones to supercomputers. The mechanical integrity and reliability of these structures are important because ULSI devices are the basis of the technologically and economically crucial electronics industry. Each ULSI chip contains a plate of single-crystal silicon carrying approximately one billion transistors, fabricated by nanoscale lithography. Present-day interconnect structures consist of ten or more levels of nanometre-scale copper conductors formed in trenches in dielectric layers, referred to as damascene structures, on top of the silicon surface. The interconnect structures carry electrical signals among the various individual

devices and functional blocks on a ULSI chip, and also form the first level in the hierarchy of structures linking the transistors within the chip to the outside world. They may also provide a useful path for conducting heat away from the chip. The design of present-day copper interconnect structures has been described in detail, for example, by Jackson *et al.* [1] and Bohr [2]. Each successive layer is produced by: (a) adding a layer of dielectric; (b) etching trenches that define the geometry of the thin-film copper conductors, including the vias that connect the layers; (c) depositing a very thin (few nm) copper seed layer by physical vapour deposition, followed by electrodeposition to fill the trenches; and (d) performing chemical mechanical polishing (CMP) to remove the excess copper and planarize the structure. In addition to these general features, present ULSI interconnect structures often include additional layers with specific purposes, such as diffusion barrier layers surrounding and capping the copper [3, 4]. Although leading-edge interconnect lines are now well below 100 nm wide, calculations and experimental results for lines from 5 μm to 300 nm

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wide are reported here, with the purpose of improved understanding of the failure mechanisms driven by cyclic Joule heating.

Both manufacturing processes and service conditions impose temperature cycles on ULSI chips. These temperature cycles, along with material interactions within the interconnect structure, lead to reliability issues such as void formation, fracture, and delamination. Void formation is presently recognized as a critical service reliability issue for interconnect structures on leading-edge commercial chips. It is classified into two types: electromigration voiding [5], where the flow of electrical current has a predominant role; and stress-induced voiding [6], where the relaxation of process-induced stresses plays the key role. Temperature cycling is a classical 'stressing' method used to test the integrity and reliability of electronic structures and devices [7].

The concept that mechanical fatigue can be produced by low-cycle thermal stressing was explored at book length by Manson [8]. Manson did not anticipate the large number of thermal cycles that can be reached by Joule heating with alternating current (AC), but he did recommend the adaptation of the usual approaches to mechanical fatigue, such as the plastic-strain-versus-life and total-strain-versus-life correlations, for analysing thermal fatigue. The von Mises equivalent strain is commonly used as a single-parameter measure of the shear strain under multiaxial loading, although care must be taken to account for possible changes of sign during cyclic loading.

Recent observations have been reported on the effect of local thermal cycling, induced by Joule heating resulting from high current density AC, on thin films of copper and aluminium on silicon substrates [9–15]. Because silicon has a considerably lower thermal expansion coefficient than aluminium and copper, moderate temperature excursions of a few hundreds of degrees Celsius were shown to produce stresses of the order of the yield strength of the metal conductors. Microstructural damage characteristic of mechanical fatigue was shown to result from the application of high amplitude AC to aluminium lines on silicon substrates [16, 17].

Practically all of the studies to date on cyclic Joule heating have reported on unconstrained conductive metal lines on substrates, but some studies of buried lines have been reported [12, 15, 18, 19]. The behaviour of conductors buried within a dielectric structure is expected to be influenced by the constraint exerted by the surrounding structure. The mechanical behaviour of multilayer intercon-

nect structures has recently been reviewed by Shen [20]. The presence of high stresses in such structures has been verified by Murray *et al.* [21] and by Paik *et al.* [22]; these are cited here as examples of the multitude of reports on the behaviour and effects of stresses in interconnect structures that can be found in the literature. However, the vast majority of these reports are concerned with static temperatures.

The present paper reports calculations of cyclic strains in copper lines within copper damascene interconnect test structures from a commercial source, and applies the results to the interpretation of experimental tests of such lines by high amplitude AC. The material properties used include initial stresses and strain hardening values that are specific, and possibly unique, to copper damascene interconnect structures. The focus is on the relevant material properties for these structures and on the different temperature ranges needed to reach cyclic strain values in the range of 0.01 in different conductor and dielectric geometries. This strain level corresponds to easily observable mechanical fatigue lives of a few hundred to a few thousand cycles in bulk metals. Also, it is of the order of the transition between low cycle, or strain controlled, and high cycle, or stress controlled, mechanical fatigue in electrodeposited copper [23], although for most bulk metals this transition occurs at somewhat lower strains. To the extent that AC fatigue is truly a mechanical fatigue mechanism, it should exhibit behaviours similar to those observed in mechanical fatigue tests, including quantitative characteristics such as the slopes of the strain-life curve in the low and high cycle fatigue regimes. Scanning electron microscope (SEM) observations of the tested structures are included to clarify the damage mechanisms. The proposed interpretation of these observations is that a more comprehensive modelling approach, beyond mechanical fatigue and even beyond continuum mechanics, is needed to describe and understand the effect of cyclic Joule heating on the types of structures studied here.

2 CALCULATIONS

The geometries analysed consisted of one- and two-layer damascene copper lines on silicon wafers. Two main types were modelled: lines 3 μm wide contained on all sides within silicon oxide dielectric (type 1, Fig. 1) and referred to as constrained; and lines 5 μm wide with no dielectric on the top side (type 2, Fig. 2) and referred to as unconstrained. The cross-section used for the type 1 specimens is shown

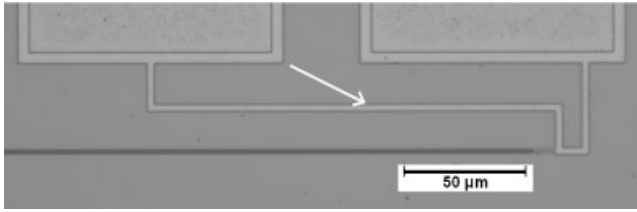


Fig. 1 Optical image of a copper damascene test structure, type 1, constrained. The background is silicon oxide dielectric on the silicon substrate. The large rectangles at the top are electrical contact pads. The arrow indicates the 3 μm wide line, clearly visible through the overlying dielectric. The darker strip is the 300 nm line, with additional lines of the same width parallel to it

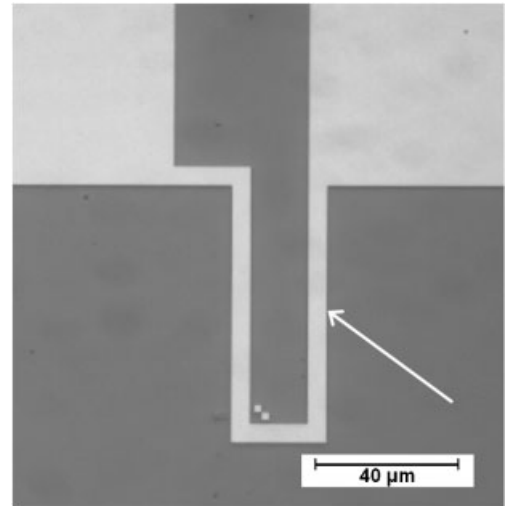


Fig. 2 Optical image of a copper damascene test structure, type 2, unconstrained. The background is dielectric on the silicon substrate. The large, lighter-grey rectangles at the top are electrical contact pads. The arrow indicates the U-shaped 5 μm wide line connecting the pads

in Fig. 3; the total structural width modelled, 8000 nm from the mid-line, was sufficiently large that the lateral boundary did not affect the temperature and strain distributions in the neighbourhood of the line. A similar-section geometry, but with the topmost layer of dielectric absent and a wider copper line, was used for the type 2 specimens. One geometry was analysed in three dimensions to show the behaviour of the temperature and stress near the ends of the lines. To check the effect of line width, analyses of narrow lines of width 300 nm

contained both in silicon oxide and in ‘low-k’ dielectric, which is less stiff than silicon oxide, were also performed.

Shen *et al.* [20], Paik *et al.* [24], and other investigators have carried out continuum-mechanics

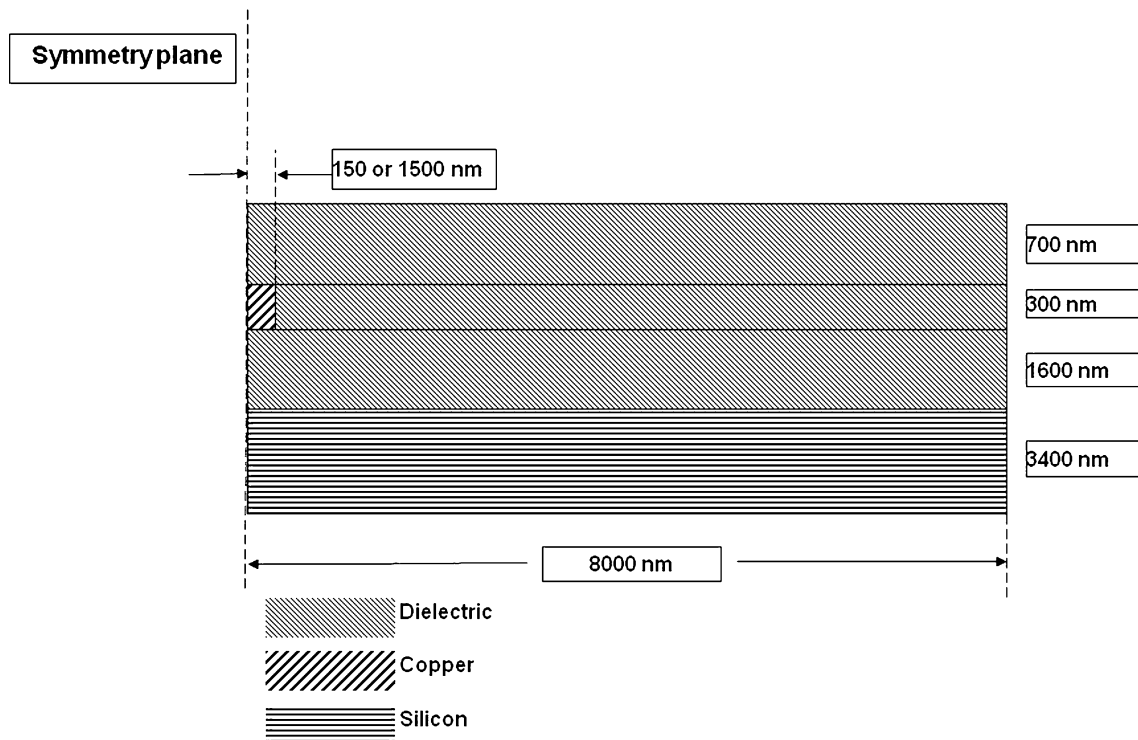


Fig. 3 Idealized section analysed for the type 1 specimens. Additional very thin layers may be present in the actual structures; these are expected to have negligible effects on the mechanical behaviour and are not modelled explicitly

analyses of interconnect structures by use of finite element analysis (FEA) implemented in commercial software. This same approach was followed here. The temperature-independent material properties used are listed in Table 1, in the units actually employed in the calculation; they represent typical physical property values as found in handbooks and used by previous investigators for calculating mechanical effects. The Young's modulus and Poisson's ratio values for copper and silicon are average values for polycrystalline forms. All the analyses were carried out in two stages: first, a calculation of the temperature distribution produced by heat dissipated in the copper; and, second, calculation of the resulting static or cyclic stresses and strains caused by imposing ramped temperature cycles between the distributed temperature values and the reference temperature, which was taken as zero. The purpose of the temperature calculation was only to obtain a realistic temperature distribution in the copper. The result in every case was that the temperature throughout the copper was essentially constant, as might have been postulated based on the high thermal conductivity of copper. The separate calculation of temperature and strain assumes that the thermal properties are independent of stress and strain, an accurate assumption for the experimental situation considered here.

Residual tensile stress is a key feature of copper damascene interconnect structures, as described, for example, by Shen *et al.* [20] and Paik *et al.* [22]. These stresses arise because the electroplating process leaves volatile impurities that are driven out of the copper during annealing. The copper is

considered to reach a stress free state at the annealing temperature, 200 to 400°C. On cooling back down to room temperature, the copper contracts but the surrounding structure, to which the copper is tightly bonded, contracts much less. Initial stresses up to 400 MPa were considered here. The initial stress is considered significant because it may alter the plastic deformation in the copper and also may promote voiding [25]; it has no effect on the behaviour of the linear elastic dielectric materials.

Conductors constrained with dielectric have been described as passivated. Shen and Ramamurty [26], abbreviated below as SR, reported on the inelastic stress-strain response of passivated copper films in wafer-curvature experiments. Their result was that films encased in dielectric have very high strain hardening, much higher than has been seen in tensile tests of free-standing films, for example in reference [27]. Therefore, two different sets of material properties for copper were used: one, for the constrained copper, by which is meant copper that is enclosed on all sides within dielectric; and another, for unconstrained copper, which has its top surface unpassivated. These two parameterizations of copper differ in the yield strength and the strain hardening; the values are listed in Table 2. The values referred to as SR fit are an approximation to the behaviour described in reference [26]. The values for unpassivated copper represent a bilinear approximation to typical tensile stress-strain curves for electrodeposited copper, combined with the expected temperature dependence for face-centred-cubic materials. SR also recommend the use of the kinematic hardening model; this model was used for

Table 1 Temperature-independent material property values used in the analyses

Material	Thermal conductivity (W/nmK)	Thermal expansion (K ⁻¹)	Young's modulus (GPa)	Poisson's ratio	Initial stress (GPa)
Silicon	1.5×10^{-7}	2.6×10^{-6}	160	0.2	0
Silicon oxide	1.38×10^{-9}	5.5×10^{-7}	69	0.25	0
Low-k dielectric	1.38×10^{-9}	1.0×10^{-5}	30	0.25	0
Copper	4.01×10^{-7}	1.73×10^{-5}	130	0.35	0.36

Table 2 Key values for two sets of plastic properties of copper used in the analyses. The FEA software interpolates between the key values

Passivated copper, to approximate the high work hardening of the SR results						
Temperature (°C)	0	800	1600			
Yield stress (GPa)	0.4	0.1	0.001			
Tangent modulus (GPa)	60	30	0.0001			
Unpassivated copper, low work hardening						
Temperature (°C)	0	200	400	600	800	1500
Yield stress (GPa)	0.2	0.175	0.15	0.1	0.05	0.02
Tangent modulus (GPa)	8	7	6	5	4	3

all calculations. No mechanical property changes resulting from temperature cycling or from line width were implemented.

The temperature cycling was handled by use of the load step facility of the FEA package. For each of the maximum temperature values reported, the static temperature distribution produced by a uniform, constant rate of heat dissipation in the copper only was calculated. The minimum temperature was taken as the chuck temperature everywhere; it has been verified, by modelling and by experimental observations of cyclic minimum and maximum temperatures by use of electrical resistance as a temperature monitor [10], that the lines studied here cool down to the chuck temperature during each temperature cycle. After the initial heating, the temperature was ramped repeatedly between its maximum and minimum values, in order to model the cyclic plastic strain. Each ramp consisted of four to six individual quasi-static analyses, in which a set of temperatures was imposed and the stresses and strains were allowed to reach equilibrium. Slight differences in strains between the initial and the following temperature excursions were seen, but then the behaviour stabilized. The total cyclic strain range values reported here are the differences between the average maximum and average minimum values of the von Mises equivalent total strain for three temperature cycles.

The reported strain values were based on two-dimensional FEA calculations, in which the total strain in the out-of-plane direction, taken along the length of the line, is zero. This procedure is appropriate for the present case because the line lengths were large compared with their widths, so that temperature and strain did not vary along the lines except near the ends. The results of two-dimensional calculations matched those of three-dimensional (3D) calculations for test cases. As the total strain included a thermal part, the calculation was capable of, and did, produce non-zero values for the out-of-plane mechanical strain. The usual strategy of choosing the mesh refinement, based on insensitivity of the results to further refinement, was used. The strain values reported include only the mechanical parts, both elastic and plastic. Care was taken to allow for the possibility of a change of sign of the physical von Mises strain, ε_{vm} , so that strain ranges covering both compressive and tensile strains were reported properly, as shown in equation (1)

$$\varepsilon_{vm} = \pm \frac{2}{3} \sqrt{\frac{1}{2} [(\varepsilon_1 - \varepsilon_2)^2 + (\varepsilon_2 - \varepsilon_3)^2 + (\varepsilon_3 - \varepsilon_1)^2]} \quad (1)$$

Here ε_1 , ε_2 , and ε_3 are the total principal strains. The factor of 2/3 would be appropriate for highly plastic strains; it was used for consistency in all cases. For each set of strains, the sign was taken as the sign of $\varepsilon_{yy} - \varepsilon_{zz}$, where the z -direction is along the length of the line, and the y -direction is out of the plane of the damascene structure.

3 RESULTS

3.1 Results of strain calculations

Figures 1 and 2 show that the specimen lines end at electrical contact pads 100 μm square. The current density in these pads was much lower than in the lines, so they were heated much less than the lines. The extent of the temperature gradient was modelled in three dimensions for a covered 300 nm wide line by constraining the temperature to 0°C at the line end while imposing heat dissipation along the whole length of the line. The results, plotted in Fig. 4, show that temperatures, stresses, and strains at the line centre all reached 95 per cent of their steady state value by 15 μm from the end of the line. Only small variations of the stresses and strains, 10 per cent or less, were found across the width of the 300 nm wide lines. Larger variations were seen across the wide lines, as illustrated by the von Mises stress displayed in Fig. 5.

The results for von Mises equivalent total strain range as a function of temperature are summarized in Fig. 6. The values plotted are the ranges of the von Mises total strain, including consideration of sign changes through the strain cycle, at the centres of the various lines. The 5 μm wide, unconstrained line reaches a total strain range of 0.01 with a temperature range of about 350°C. The 3 μm wide buried line, with its higher strain hardening, needs only a slightly higher temperature range, about 400°C, to reach the same strain range. This is because the width of the line is several times the thickness of the dielectric layer covering the line, so that the elastic deformation of the dielectric is able to partially relax the constraint in the centre of the line. The narrow lines, with width less than half the thickness of the dielectric layer above them, need a temperature range of around 850°C to reach a strain range of 0.01. The initial stress was found to have only a small effect on the cyclic strain range for a given temperature; in one example, for 300 nm wide lines in low- k dielectric, an initial stress of 400 MPa reduced the maximum strain range by less than 3 per cent relative to the value for no initial stress.

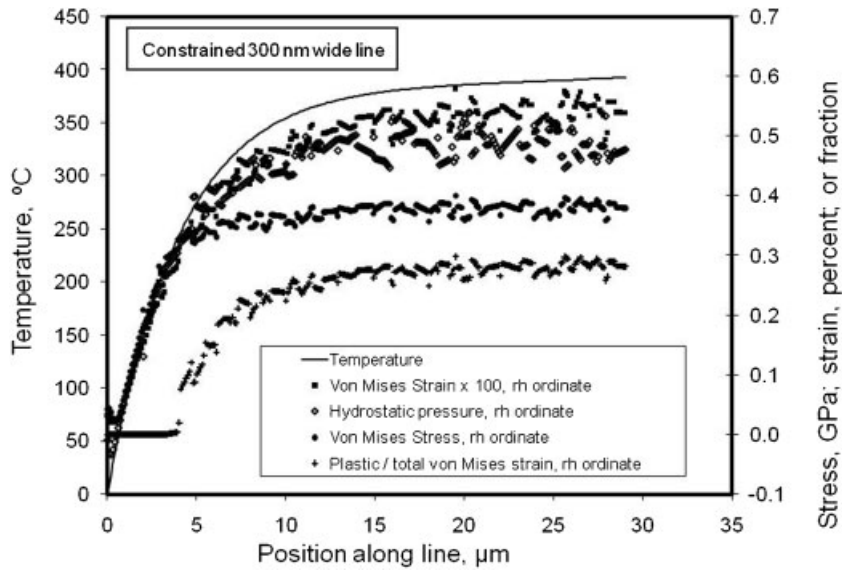


Fig. 4 Variation of temperature (left-hand ordinate), and von Mises total strain, hydrostatic pressure, von Mises stress, and fraction of plastic von Mises strain (all plotted to the right-hand ordinate) along the centre of a covered 300 nm wide line near the end. The noise in the stress and strain quantities is an artefact of the FEA and has no physical significance, but is difficult to avoid in three-dimensional models with components of different sizes like this

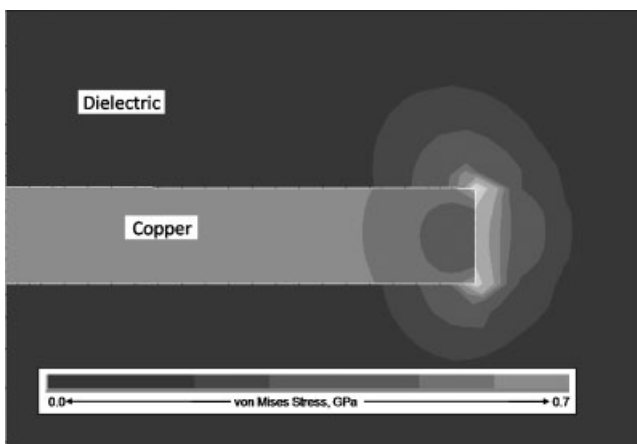


Fig. 5 Contour plot of von Mises stress across half of a covered 3 μm wide line at a peak temperature of 665°C, showing the decrease of the stress near the line edge. Only the right-hand half of the line is shown; the stress distribution is symmetric across the line

3.2 SEM observations and lifetimes

Actual specimens of the types illustrated in Figs 1 and 2 were tested electrically and examined by SEM afterward. All electrical tests were conducted with sinusoidal excitation at 100 Hz under voltage control. Current was introduced through the bonding pads shown in the figures, either by sharp tungsten probes (type 1) or by wire-bonding (type 2). The

type 2 specimens were tested under high vacuum to avoid oxidation of the copper. All the specimens were imaged after testing in the SEM. For the type 1 specimens, the dielectric covering the copper lines was removed by etching in a 10 per cent hydrofluoric acid solution, so that SEM images could be produced.

Figure 7 shows the surface of an unconstrained (type 2), wide line after AC testing at 100 Hz over a temperature range of 252°C, corresponding through the FEA results to a strain range of 0.0071. Its lifetime to electrical failure was 1751 s. Note the regular intrusions and extrusions. The shortest-lived of the type 2 lines had a lifetime of 192 s, at a temperature range of 315°C, which produced a total strain range of 0.0092; the longest-lived had a lifetime of 3264 s, at a temperature range of 221°C and a strain range of 0.0060. The type 2 lines tested at lower AC amplitudes developed multiple voids.

Figure 8 shows the surface of a dielectric-constrained line after AC testing at a calculated strain range of 0.0091, at a temperature range of 396°C for a lifetime of 1497 s. The surface appearance includes voids, but no intrusion–extrusion features were found on this specimen. Likewise, no such features were found on a specimen tested at a strain range of 0.0059 and a temperature range of 276°C, which reached a lifetime of 8782 s. The fatigue-like features were also not found on constrained lines tested at

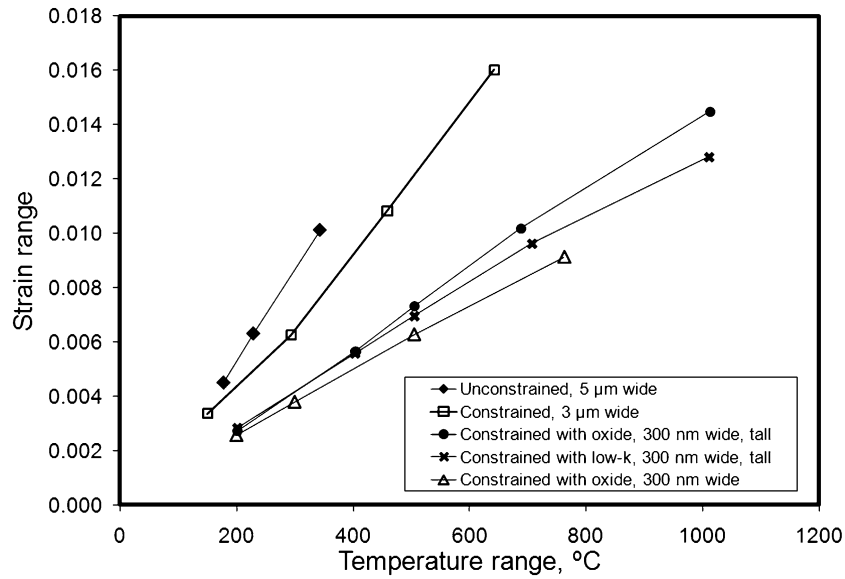


Fig. 6 Ranges of the total von Mises strain plotted against temperature range for copper lines of various geometries

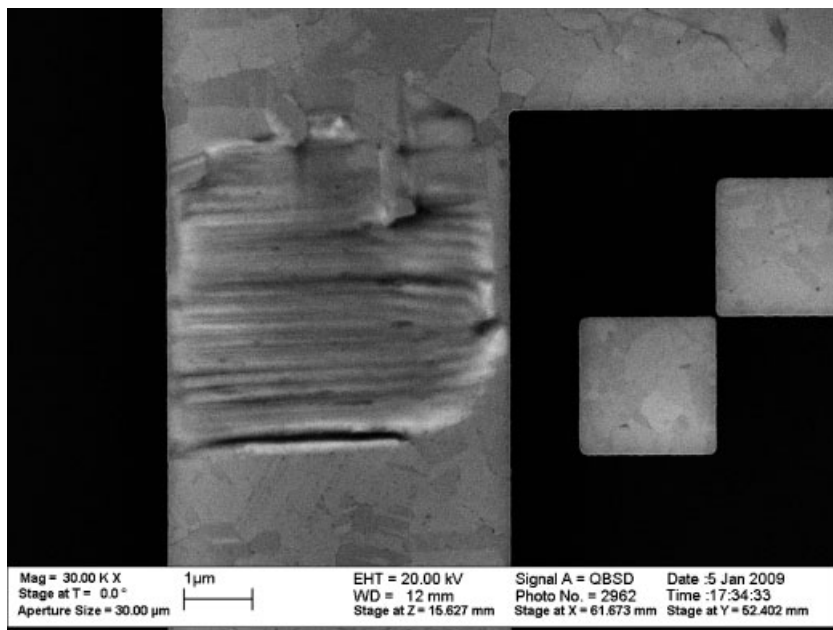


Fig. 7 SEM micrograph of tested type 2 specimen line, unconstrained copper damascene. This specimen was tested at 100 Hz at a peak current density of 10 MA/cm². The temperature range was 252°C, the strain range was 0.0071, and the lifetime was 1751 s. Note the topography, particularly the regularly spaced intrusions and extrusions, similar to those previously reported for aluminium [9, 11]. This image reveals hints of additional features that formed on this set of copper lines during AC testing, which were not seen in the tests of aluminium

higher cyclic temperatures; the extreme case observed had a calculated cyclic strain range of 0.016, with a lifetime of 112 s.

Figure 9 plots experimental results for total strain range against lifetime; each strain point plotted

represents a single test. The failure criterion was electrical open-circuit; the strain ranges were obtained from the strain-temperature dependences plotted in Fig. 6. The maximum current densities used in these tests ranged from 9.4 to 10.9 MA/cm²

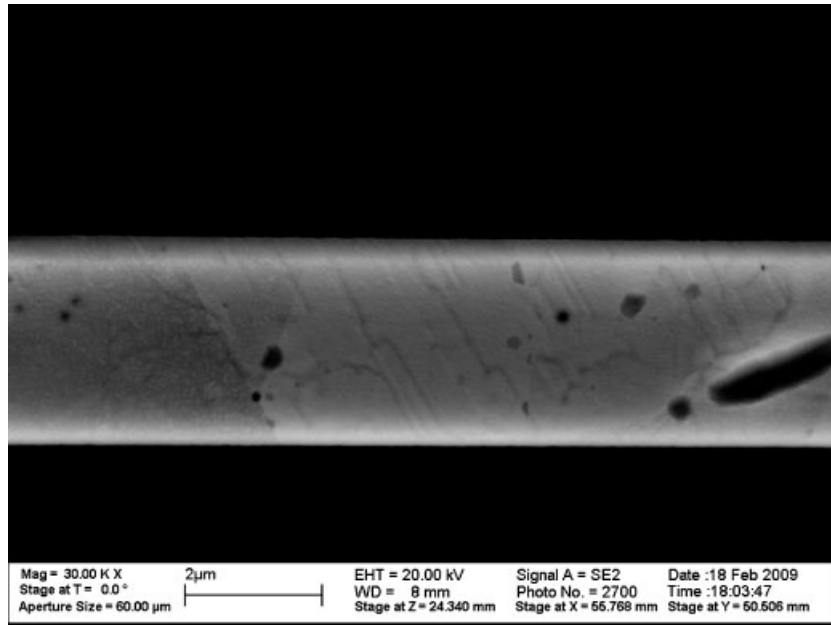


Fig. 8 SEM micrograph of a type 1 specimen, a constrained copper damascene line $3\ \mu\text{m}$ wide. This specimen was tested at 100 Hz at a peak current density of $18\ \text{MA}/\text{cm}^2$. The temperature range was 396°C , the total von Mises strain range was 0.0091, and the lifetime was 1498 s. On this specimen and others of this type tested under similar conditions, the authors found voids as shown, but no features like the regular intrusions and extrusions shown for the type 2 specimen in the previous figure

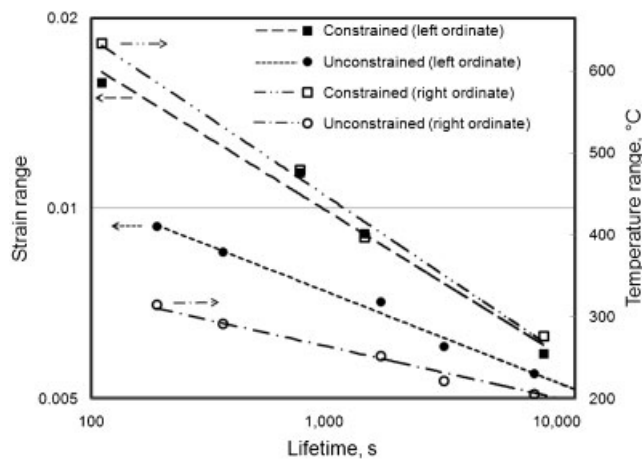


Fig. 9 Plot of strain and temperature ranges against lifetime for constrained (type 1) and unconstrained (type 2) wide damascene copper lines stressed by AC at 100 Hz. Each single test is plotted as both a solid point, which gives the strain range, and an open point, which gives the temperature range. The strain range axis is at the left, and the temperature range axis is at the right. The dashed lines show attempted fits of the strain data to the Basquin equation; interpretation is discussed in the text. The chain-dashed lines are drawn through the temperature data as a guide for the eye

for the unconstrained lines, and from 13.9 to $15.5\ \text{MA}/\text{cm}^2$ for the constrained lines. This figure also shows the temperature ranges.

Values for the temperature range during AC stressing were obtained from measurements of the electrical resistance [28]. The particular value of the calibration factor used here was obtained from static measurements of heated specimens. The experimental temperature values were considered to be correct to within 15°C , owing to the possibility of specimen-to-specimen differences of the resistance-temperature calibration factor. These uncertainties in temperature propagated proportionally to strain, through the dependences shown in Fig. 6. These considerations imply a relative uncertainty of about 5 per cent in the strain range values reported in Fig. 9.

4 DISCUSSION AND CONCLUSIONS

The strain-temperature results of Fig. 6, derived from static calculations, are used to analyse experiments in which electrical currents at 100 Hz produced temperature and strain cycles at 200 Hz. The application of static elastic analysis to tests at this frequency on copper films up to at least 450°C is supported by the results of Choi and Nix [29]. They

were able to describe resonance experiments up to 2000 Hz and 500°C on bi-layer silicon–copper specimens using an anelastic analysis that included numerically small – though for their purposes important – perturbations from linear elasticity. The data of Fig. 6 also depend on the value used for the yield strength of copper, but not sensitively, as shown by a test calculation for a fully passivated 300 nm wide line at 760°C. A reduction of the strain hardening parameters listed in Table 2 to half the values shown resulted in a relative increase of only 3 per cent in the von Mises strain at the centre of the line.

Figure 6 shows that the strain–temperature relationship is quantitatively different for different line geometries; the existence of the differences and the trend toward lower strains for narrower lines are not surprising. The result reported by Moreau *et al.* [12] that narrower lines have longer lifetimes than wide ones under AC cycling would be generally consistent with this trend, if the relevant failure mechanism were dependent on the magnitude of the von Mises strain.

The present peak current density values in unconstrained lines are approximately half to two-thirds of values previously reported for similar specimens, cyclic temperature ranges, and lifetimes [10, 12]. It is difficult to draw any detailed conclusions from these differences, because the controlling variables are temperature and strain. Geometrical or material differences between the structures could change both the dependence of temperature on current density and the dependence of strain on temperature. For example, while the current density given in reference [10] for failure at around 500 s was higher than in the present study, the cyclic temperature range for that test was reported as 190°C, while the trend of the present data for unpassivated lines indicates that a lifetime of 500 s would correspond to a cyclic temperature range of about 250°C.

Topographic features produced by Joule heating from AC current, similar to those shown in Fig. 7 for the type 2 specimens, are called intrusions and extrusions and have been associated with mechanical fatigue [10, 14, 16–17]. The surface appearance of the type 1 (constrained) lines after testing, as shown in Fig. 8, was much different from that of the unconstrained lines. These had large voids, and did not have the intrusions and extrusions. The absence of fatigue-like intrusions and extrusions on buried lines was reported previously for narrow lines in another study [12] and for 300 nm wide lines on this

same set of specimens [18]. The voids that appeared in all of the type 1 lines tested, as illustrated by Fig. 8, indicate that a diffusion mechanism is being driven by the AC cycling of constrained lines.

As the number of cycles to failure and the strain amplitude for the present type 2 (unconstrained) specimens, Fig. 9, fall in the high-cycle fatigue range established by the data of reference [23] for thick electrodeposited copper, an attempt was made to analyse both data sets with a Basquin equation [16, 30]

$$\frac{\Delta\varepsilon}{2} = \frac{\sigma_f}{E} (2N)^b$$

Here $\Delta\varepsilon$ is the strain range, E is Young's modulus, σ_f is the fatigue strength coefficient, $2N$ is the number of load reversals to failure, and b is the fatigue strength exponent. The fitted strain–lifetime dependences are shown in Fig. 9. The value of the fatigue strength exponent obtained by fitting the data of Fig. 9 for the unconstrained (type 2) lines, -0.145 , was slightly outside the usual range of -0.05 to -0.12 for stress-controlled mechanical fatigue [30]; the strength coefficient value, 3.1 GPa, was about 10 times the ultimate tensile strength of copper films, which is around 300 MPa [31]. The data for constrained lines were fitted by an exponent of -0.23 and a coefficient of over 10 GPa. Both of these strength coefficient values are inconsistent with stress-controlled fatigue, because the strength coefficient is expected to be approximately equal to the ultimate tensile strength [30]. Such values could have resulted from applying the fit procedure to data in the transition region between stress- and strain-controlled fatigue, where the full strain–life equation [30] would be required. This equation gives the strain range as the sum of two terms of the same form as the power-law term of the Basquin equation. The Basquin term is retained. The additional term has a fatigue ductility coefficient in place of σ_f/E , and a ductility exponent in place of the strength exponent. Hypothetical strain–life curves were plotted and compared to the present data. Neither set of data could be replicated with a reasonable set of strain–life parameters. For example, to fit the data for the constrained specimens, a fatigue ductility exponent of about -0.25 is needed, while reference [23] found that this parameter ranged between -0.38 and -0.56 for several electrodeposited copper films, and the normal range for metals is -0.5 to -0.7 [32]. The hidden temperature variation within the strain–lifetime data in Fig. 9 might be considered as the cause of the discrepancy; but, in order for

temperature variation to strongly influence the observed behaviour, a strong temperature dependence of the strain–lifetime curve would be required. However, the strain–lifetime behaviour of copper appears insensitive to temperature, at least at room temperature and below [33]. The differences in the values of the coefficients between the two specimen types might be attributed to the temperature difference of up to 300°C between the two sets of test conditions; a counterargument is that this interpretation would imply an increase in fatigue lifetime with increasing temperature, which is inconsistent with previous results for copper alloys [34].

It is proposed that the data for the two types of specimens studied experimentally here are inconsistent with the single damage mechanism of mechanical fatigue, because of the substantial differences between them in both the surface appearances reported in Figs 7 and 8 and the lifetime trends with strain range shown in Fig. 9. It is proposed that two different damage mechanisms, mechanical fatigue and diffusion, are operating simultaneously in both types of specimens tested. Both mechanisms lead to electrical failure by reduction of the effective current-carrying cross-sectional area of the line to the point where thermal runaway brings rapid final failure. The proposed dominant mechanism of area loss in the unconstrained lines (type 2) at shorter lifetimes is mechanical fatigue [10, 14, 16, 17]; plastic deformation leads to local thinning and ultimately to failure at much deeper intrusions of the same basic type shown in Fig. 7, with some diffusion-related behaviour also appearing because of the elevated temperatures present. The proposed dominant mechanism of area loss in the constrained lines (type 1) is void growth and accumulation, caused by diffusive mechanisms promoted by the higher temperatures in these lines and possibly aided by the electrical current. The obliteration of the lines at their failure sites in AC testing, noted previously [12, 18], has prevented determination of the actual failure mechanisms by direct observation.

A more basic conclusion from this series of experiments is that the surface constraint available in micro- and nanoscale structures, with their much higher surface-to-volume ratios, may be capable of altering the mechanical behaviour of the materials much more significantly than surface conditions in macroscale materials can. Present and previously reported observations suggest that crystallography, dislocation behaviour, and void formation should be

considered in modelling the behaviour of small-scale constrained structures subjected to thermal cycling. The roles of crystallographic orientation and dislocation activity in the response of unconstrained aluminium lines to AC were clarified by transmission electron microscope observations [17]. Additional features of the behaviour of the specimens discussed here, which are not clearly related to the strain range, will be described in a separate report.

ACKNOWLEDGEMENT

The Office of Microelectronics Programs of NIST provided substantial financial support for this work.

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REFERENCES

- 1 Jackson, R. L., Broadbent, E., Cacouris, T., Harrus, A., Biberger, M., Patton, E., and Walsh, T. Processing and integration of copper interconnects. *Solid State Technol.*, 1998, **41**(3), 49–55.
- 2 Bohr, M. T. Interconnect scaling: the real limiter to high performance ULSI. *Solid State Technol.*, 1996, **39**(9), 105.
- 3 Kaloyeros, A. E. and Eisenbraun, E. Ultrathin diffusion barriers/liners for gigascale copper metallization. *A. Rev. Mater. Sci.*, 2000, **30**, 363–385.
- 4 Li, B. Z., Sullivan, T. D., Lee, T. C., and Badami, D. Reliability challenges for copper interconnects. *Microelectronics Reliability*, 2004, **44**(3), 365–380.
- 5 Ogawa, E. T., Lee, K. D., Blaschke, V. A., and Ho, P. S. Electromigration reliability issues in dual-damascene Cu interconnections. *IEEE Trans Reliability*, 2002, **51**(4), 403–419.
- 6 Nucci, J. A., Keller, R. R., Sanchez, J. E., and Shacham-Diamand, Y. Local crystallographic texture and voiding in passivated copper interconnects. *Appl. Phys. Lett.*, 1996, **69**(26), 4017–4019.
- 7 US Department of Defense. *MIL-STD 883G, Test Method Standard, Microcircuits*, 2006 (US Department of Defense, Washington DC).
- 8 Manson, S. S. *Thermal Stress and Low-Cycle Fatigue*, 1966 (McGraw-Hill, New York).
- 9 Philofsky, E., Ravi, K., Hall, E., and Black, J. Surface reconstruction of aluminum metallization: a new potential wearout mechanism. 9th Annual IEEE Reliability Physics Symposium, Las Vegas, Nevada, 1971, pp. 120–128.
- 10 Monig, R., Keller, R. R., and Volkert, C. A. Thermal fatigue testing of thin metal films. *Rev. Sci. Instrum.*, 2004, **75**(11), 4997–5004.
- 11 Keller, R. R., Geiss, R. H., Barbosa, N., Slifka, A. J., and Read, D. T. Strain-induced grain growth during rapid thermal cycling of aluminum interconnects. *Metall. Mater. Trans. A: Phys. Metall. Mater. Sci.*, 2007, **38A**(13), 2263–2272.

- 12 Moreau, S., Maitrejean, S., and Passemard, G. Fatigue of damascene copper lines under cyclic electrical loading. *Microelectronic Engng*, 2007, **84**(11), 2658–2662.
- 13 Biesemans, L., Vanstreels, K., Brongersma, S. H., D’Haen, J., De Ceuninck, W., and D’Olieslaeger, M. Microstructural evolution of Cu interconnect under AC, pulsed DC and DC current stress. *Conference Proceedings AMC XXII Advanced Metallization Conference*, Materials Research Society, 2007, pp. 453–458.
- 14 Keller, R. R., Geiss, R. H., Cheng, Y.-W., and Read, D. T. Microstructure evolution during electric current induced thermomechanical fatigue of interconnects. *Mater. Res. Soc. Proc.*, 2005, **863**, 295–300.
- 15 Moreau, S., Maitrejean, S., and Passemard, G. Fatigue of damascene copper lines under AC loading. *Mater. Res. Soc. Proc.*, 2007, **990**, 0990-B07-17.
- 16 Barbosa, N., Keller, R. R., Read, D. T., Geiss, R. H., and Vinci, R. P. Comparison of electrical and microtensile evaluations of mechanical properties of an aluminum film. *Metall. Mater. Trans. A: Phys. Metall. Mater. Sci.*, 2007, **38A**(13), 2160–2167.
- 17 Geiss, R. H. and Read, D. T. Defect behavior in aluminum interconnect lines deformed thermomechanically by cyclic joule heating. *Acta Mater.*, 2008, **56**(2), 274–281.
- 18 Read, D. T. and Geiss, R. Thermal cycling of 300 nm buried damascene copper interconnect lines by Joule heating. *Conference Proceedings on Nanotechnology*, 2008, Vol. 1, pp. 218–221.
- 19 Read, D. T., Geiss, R. H., and Alers, G. A. Study of fatigue behavior of 300 nm damascene interconnect using high amplitude AC tests. *Mater. Res. Soc. Proc.*, 2007, **990**, 121–126.
- 20 Shen, Y. L. Externally constrained plastic flow in miniaturized metallic structures: A continuum-based approach to thin films, lines, and joints. *Prog. Mater. Sci.*, 2008, **53**(5), 838–891.
- 21 Murray, C. E., Goldsmith, C. C., Shaw, T. M., Doyle, J. P., and Noyan, I. C. Thermal stress evolution in embedded Cu/low-k dielectric composite features. *Appl. Phys. Lett.*, 2006, **89**(1), 011913.
- 22 Paik, J. M., Park, H., and Joo, Y. C. Effect of low-k dielectric on stress and stress-induced damage in Cu interconnects. *Microelectronic Engng*, 2004, **71**(3–4), 348–357.
- 23 Merchant, H. D., Minor, M. G., and Liu, Y. L. Mechanical fatigue of thin copper foil. *J. Electronic Mater.*, 1999, **28**(9), 998–1007.
- 24 Paik, J. M., Park, H., Joo, Y. C., and Park, K. C. Effect of dielectric materials on stress-induced damage modes in damascene Cu lines. *J. Appl. Phys.*, 2005, **97**(10), 104513.
- 25 Borgesen, P., Lee, J. K., Gleixner, R., and Li, C. Y. Thermal-stress-induced voiding in narrow, passivated Cu lines. *Appl. Phys. Lett.*, 1992, **60**(14), 1706–1708.
- 26 Shen, Y. L. and Ramamurty, U. Constitutive response of passivated copper films to thermal cycling. *J. Appl. Phys.*, 2003, **93**(3), 1806–1812.
- 27 Read, D. T., Cheng, Y.-W., and Geiss, R. Morphology, microstructure, and mechanical properties of a copper electrodeposit. *Microelectronic Engng*, 2004, **75**(1), 63–70.
- 28 Schuster, C. E., Vangel, M. G., and Schafft, H. A. Improved estimation of the resistivity of pure copper and electrical determination of thin copper film dimensions. *Microelectronics Reliability*, 2001, **41**(2), 239–252.
- 29 Choi, D. H. and Nix, W. D. Anelastic behavior of copper thin films on silicon substrates: Damping associated with dislocations. *Acta Mater.*, 2006, **54**(3), 679–687.
- 30 Dieter, G. *Mechanical metallurgy*, 3rd edition, 1986, pp. 392–392 (McGraw-Hill, New York).
- 31 Read, D. T., Geiss, R., Ramsey, J., Scherban, T., Xu, G., Blaine, J., Miner, B., and Emery, R. D. Nanoindentation and tensile behavior of copper films. *Mater. Res. Soc. Proc.*, 2003, **778**, 93–98.
- 32 Sandor, B. I. *Fundamentals of cyclic stress and strain*, 1972, p. 49 (University of Wisconsin Press, Madison).
- 33 Lukas, P. and Kunz, L. Effect of low-temperatures on the cyclic stress–strain response and high cycle fatigue life of polycrystalline copper. *Mater. Sci. Engng A: Struct. Mater. Properties Microstructure and Processing*, 1988, **103**(2), 233–239.
- 34 Li, G., Thomas, B. G., and Stubbins, J. F. Modeling creep and fatigue of copper alloys. *Metall. Mater. Trans. A: Phys. Metall. Mater. Sci.*, 2000, **31**(10), 2491–2502.