Test Chip to Evaluate Measurement Methods for Small Capacitances

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ABSTRACT

We designed and fabricated a test chip to evaluate the performance of new approaches to the measurement of small capacitances (femto-Farads to atto-Farads range). The test chip consists of an array of metal-oxide-semiconductor (MOS) capacitors, metal-insulator-metal (MIM) capacitors, and a series of systematically varying capacitance structures directly accessible by an atomic force microscope probe. Nominal capacitances of the test devices range from 0.3 fF (10^{-15} F) to 1.2 pF (10^{-12} F). Measurement of the complete array of capacitances by using an automatic probe station produces a "fingerprint" of capacitance values from which, after correction for pad and other stray capacitances, the relative accuracy and sensitivity of a capacitance measurement instrument can be evaluated.

MOTIVATION

Due to the continual scaling of the individual devices in integrated circuits to ever smaller dimensions, the component capacitance of these nm-scale devices defy easy measurement. Emerging nanoelectronic devices fabricated from semiconductor nanowires and quantum dots, as well as double-gate fin field-effect transistor (FinFET) devices also have capacitances that are smaller than those measurable by conventional inductance-capacitance-resistance (LCR) meters. The interior device capacitances of these deep-submicron devices (such as the gate-source, source-drain, or gate-channel capacitances) determine the operational characteristics of the device, and an accurate knowledge of their values is required for accurate device modeling and predictive computer-aided design. These internal device capacitances are often difficult to directly contact and measure with probe stations and external instrumentation. Thus, an effective method to experimentally extract these capacitances will have an immediate technological impact. As an example of "small capacitance" in this context, consider calculated capacitance-voltage (C-V) curves of nanowire MOS devices with a maximum capacitance of 4 aF (10^{-18} F) and a minimum capacitance of 1 aF [1]. Measurement of such a C-V curve would require better than aF accuracy.

Measurement of the small capacitances of nanoelectronic devices is inherently difficult. A single device fabricated with pads accessible by a probe station will display pad, probe, cable, and other stray capacitances that can be orders of magnitude larger than the device capacitance of interest. A more difficult problem is the actual measurement of small capacitance. A commonly available, high-performance LCR meter, like the Agilent 4284A[2], has a lower measurement range of 0.01 fF (10^{-17} F) and base accuracy of 0.1 %. In practice, the lower limit of detectable capacitance, signal-to-noise, and the accuracy of a capacitance measurement depend on the measurement frequency, the test signal level, and the measurement averaging time.

We have recently begun a project to evaluate the sensitivity of available capacitance measurement instrumentation to small device capacitances and best practices to achieve optimal performance for this instrumentation. It is clear that existing off-the-shelf instrumentation will have a difficult time measuring the details of device capacitances below around 0.1 fF. Towards this end we are also looking at on-chip capacitance sensors where devices could be contacted directly to the sensor without bonding pads or probe stations. To help evaluate and compare the performance of various capacitance measurement approaches, we have developed a test chip with an array of multiple capacitors of different geometries and areas. This paper will describe the test chip structure, characterization of device capacitances, and how the chip could be used to extend capacitance metrology.

CHIP LAYOUT AND FABRICATION

The test chip was designed by using the design rules for the 1.6 µm complementary metal-oxide-semiconductor (CMOS) process from AMI

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[2] Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the materials or equipment used are necessarily the best available for the purpose.

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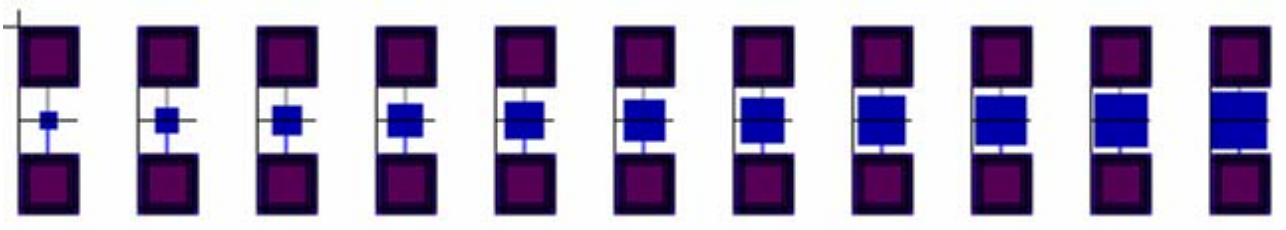

Fig. 1. A typical series of 11 devices. Bonding pads are at the top and bottom, with the MIM device in the middle.

Series	Min (fF)	Mid (fF)	Max (fF)	Notes
1	11.3	25.5	39.7	Minimum size series
2	77.9	99.2	119.7	Variation around 100 fF
3	159.4	201.9	250.8	Variation around 200 fF
4	405.6	497.3	595.7	Variation around 500 fF
5	794.8	995.9	1190.7	Variation around 1000 fF
6	987.4	997.3	1011.5	Small variation around 1000 fF
7	63.8	102.0	148.8	Variation around 100 fF, square devices
8	148.8	204.7	269.2	Variation around 200 fF, square devices
9	425.0	516.4	616.3	Variation around 500 fF, square devices
10	892.5	1022.8	1161.7	Variation around 1000 fF, square devices
11	11.3	119.7	1133.3	Maximum range series
12		101.9		Variation in perimeter-to-area ratio
13	102	612	1122	Equal 102 fF steps
14	102	102	102	Repeatability at 102 fF
15	516.4	516.4	516.4	Repeatability at 516 fF
16	1022.8	1022.8	1022.8	Repeatability at 1022 fF

Table 1. Designed oxide capacitance of each series of MOS capacitors.

Semiconductor available from the MOSIS Foundry Service. MOS capacitors were chosen for their voltage dependence and metal-insulator-metal (MIM) capacitors were chosen for their smaller total capacitance values. Both types of devices were designed with probe pads to each side of the capacitor. MOS devices were encircled by a highly doped guard band to prevent depletion edge spreading. Devices were arranged to facilitate automatic probing.

Sixteen series of 11 MOS devices were fabricated as summarized in Table 1. Series 4 of the MIM devices is shown as Figure 1. The ability to resolve a given capacitance value was tested by producing a range of devices which varied systematically around the target oxide capacitance, C_{ox}, according to the following sequence: 80 %, 90 %, 95 %, 98 %, 99 %, 100 %, 101 %, 102 %, 105 %, 110 % and 120 % of C_{ox}. Similar MIM devices were fabricated by using the intermetal dielectric, resulting in correspondingly smaller capacitances. This design yields a total of 176 devices. Two groups (A and B) of MOS and MIM devices were laid out on each chip.

MEASUREMENT RESULTS

The MOS devices were first measured with an Agilent 4284A LCR meter. Capacitance-voltage curves were measured over a range of frequencies and test signals to determine optimum measurement conditions. C-V curves measured at 100 kHz with a 50 mV test signal and dc bias swept from -3 V to +3 V in 50 mV steps were found to have minimal series resistance effects and to produce stable capacitance values from relatively high speed measurements. Oxide capacitance was estimated by averaging the measured capacitance over a small range of voltages in accumulation. Data were acquired using an automatic probe station.

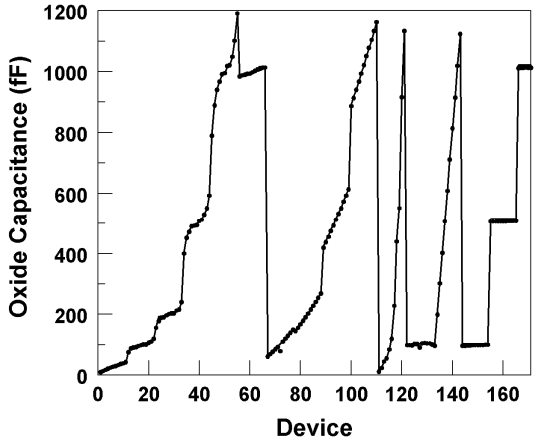

Fig. 2. Calculated oxide capacitance (solid line) and measured maximum capacitance (points) versus device number.

Excellent agreement between the designed and measured MOS oxide capacitances was seen. C_{ox} was close to the value reported from the MOSIS process monitor. Figure 2 shows the measured and modeled C_{ox} values for one complete set of devices. For a sample of ten different sets of capacitors, the slope of the measured and designed C_{ox} was 0.96 with an intercept of 137 fF. The variation of the slope from 1 is probably mostly due to how we estimated C_{ox}. The intercept is close to the simulated pad plus stray capacitance of 133 fF. In general, capacitance is resolved to within about 0.5 fF (500 aF). This resolution is sufficient to see variations due to the gate metal to substrate fringe capacitance (0.5 fF to 4.5 fF, depending on device perimeter).

When the voltage is biased in accumulation, the total capacitance of each MOS device is the parallel sum of the pad capacitance, C_{pad}, the perimeter fringe capacitance, C_{fringe}, and the oxide capacitance, C_{ox}. The test structures are designed so that the pad capacitance is MOS geometry independent, the fringe capacitance is proportional to the device perimeter, P, and the oxide capacitance is proportional to the device area, A.

$$C_{total} = C_{pad} + P \times C_{fringe} + A \times C_{ox} \qquad [1]$$

Since most of the devices are approximately square, we introduce a parameter S, where the area, A, of the device is S^2, the perimeter of the device is kS, and k is the perimeter-to-$A^{½}$ ratio of the device. The k-values of our devices vary from 4 (for a square device) to 12.3 (for a high aspect ratio rectangle), with an average of 4.14. Dividing by A and substituting S^2 for A yields:

$$\frac{C_{total}}{A} = \frac{C_{pad}}{S^2} + \frac{kC_{fringe}}{S} + C_{ox}\,. \qquad [2]$$

Hence, a plot of 1/S versus the measured capacitance per unit area should yield a 2nd order polynomial curve with a y-intercept of C_{ox}, a slope of C_{fringe}, and a curvature of C_{pad}. Figure 3 shows this universal capacitance curve for all the devices in a series on a single chip. For this chip we get a C_{ox} of 1.10 fF/μm^2 (compared to 1.12 fF/μm^2 reported for the MOSIS process monitor), C_{fringe} of 11 aF/μm (compared to 34 aF/μm for the monitor), and a C_{pad} of 131.5 fF (compared to our simulated value of 133 fF). This excellent agreement confirms that our test chip can function as a reliable test vehicle for evaluating the performance of capacitance measurement circuits applied to on-chip test structures.

Chip-to-chip variation was less than ±10 % for C_{ox} and C_{pad}, though C_{fringe} was difficult to extract precisely using this technique without time consuming remeasurement, or exclusion, of outlier devices. This is probably because C_{fringe} is no more than 1 % of the other capacitances. Figure 4 shows a systematic variation between the group A and group B MOS devices seen across all chips received from MOSIS. The residual capacitance is the difference in capacitances between equivalent devices in group A and in group B. For each of the 16 series of devices, a similar residual capacitance is seen and is correlated with the position of the device on the chip. Since the residual capacitance is between two identically designed devices, the observed variation must be due to some systematic process variation. These small variations make comparison of measured and designed capacitance more challenging.

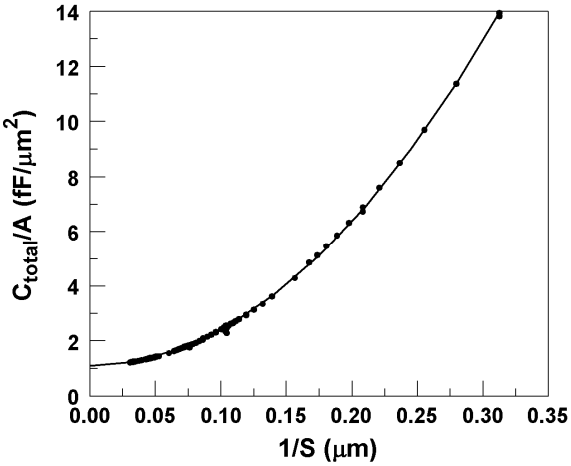

Fig. 3. Universal capacitance curve for chip C3B. Points are measured data, and the curve is the fit to data.

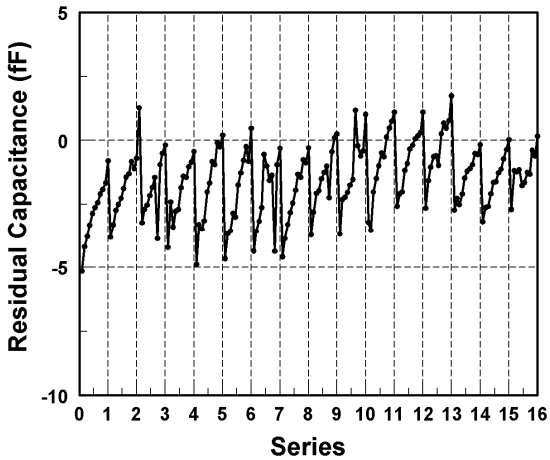

Fig. 4. Residual capacitance between devices with identical designs in different groups on the same chip. Each series consists of 11 devices.

The MIM devices display similar behavior, with corresponding smaller capacitances; their design capacitances range from 240 fF down to 0.38 fF. These devices were measured with both the Agilent 4282A LCR meter and an Andeen-Hagerling AH2700A ultra-precision capacitance bridge. In order to optimize the measurement performance of both

instruments, these devices were measured at 1 kHz, using a 1 V test signal and 5 minutes averaging time, substantially longer than required to resolve the MOS capacitance-voltage responses. Initial analysis of the data by plotting all the measured capacitances versus the design capacitance yielded lines with slopes of around 1.22 and intercepts of ~15 fF. The variation of the slope from 1 is due to a difference in the thickness of actual intermetal dielectric compared to the value used for calculating the initial model. The 15 fF intercept represents the stray probe and cable capacitance remaining after instrumentally removing the pad capacitance. Capacitances measured by the two instruments differed by about 1.2 fF over the range of devices measured. After taking this offset into account, the two instruments agreed to within an average of 50 aF. A summary of the 77 devices in the MIM series is included as Fig. 5.

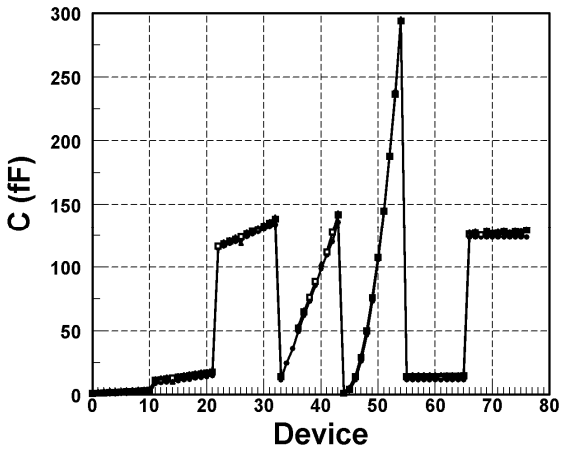

Fig. 5. Calculated and measured MIM capacitances versus device series. Theoretical data corrected for stray capacitance (solid circles) and measured capacitance for the two instruments (solid squares and open circles) are plotted.

The slope and intercept of the measured capacitance versus the design capacitance change slightly for each series of the MIM devices. This implies that as these instruments autoscale they have slightly different sensitivities to capacitance.

SUMMARY AND FUTURE APPLICATIONS

We have designed and fabricated a test chip which enables us to measure variations in capacitance down to the 0.1 fF level. This level of performance meets our needs for a test structure to quantify the behavior of capacitance measurement instruments. This test chip will be used to evaluate various approaches to small capacitance measurement that exceed the lower bounds of the existing meters and can be implemented in a single chip or hybrid configuration. We are particularly interested in approaches that measure capacitance through measurement of the time constant of resistance-capacitance (RC) circuits or resonant frequency shifts of LCR circuits. A second version of this test chip in a more aggressive technology allowing smaller capacitances is planned.

ACKNOWLEDGMENTS

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