Advanced Metrology for Nanoelectronics at the National Institute of Standards and Technology

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Introduction

On May 3, 1900, The US House Committee on Coinage, Weights and Measures met to consider the possibility of creating a national standardization laboratory. Two hours later, the Committee issued a statement to their colleagues in the house that partly said:

> It is therefore the unanimous opinion of your committee that no more essential aid could be given to manufacturing, commerce, the makers of scientific apparatus, the scientific work of the Government, of schools, colleges, and universities than by the establishment of the institution proposed by this bill (1).

In March 3, 1901, the bill founding the National Bureau of Standards (NBS) passed both houses of Congress (2).

In 1988, the U.S. Congress changes the name from NBS to the National Institute of Standards and Technology (NIST) with four parts to accomplish its functions. They are the following:

- the **NIST Laboratories**, conducting research that advances the nation's technology infrastructure and is needed by U.S. industry to continually improve products and services;
- the **Baldrige National Quality Program**, which promotes performance excellence among U.S. manufacturers, service companies, educational institutions, and health care providers; conducts outreach programs and manages the annual Malcolm Baldrige National Quality Award which recognizes performance excellence and quality achievement;
- the **Hollings Manufacturing Extension Partnership**, a nationwide network of local centers offering technical and business assistance to smaller manufacturers; and
- the **Advanced Technology Program**, which accelerates the development of innovative technologies for broad national benefit by co-funding R&D partnerships with the private sector.

NIST’s mission is to develop and promote measurement, standards, and technology to enhance productivity, facilitate trade, and improve the quality of life.

Presently, NIST consists of 8 measurement laboratories, the Manufacturing Extension Program (MEP), and the Baldrige National Quality Program. There are approximately 2,800 employees in

Gaithersburg, Maryland, Boulder, Colorado, and Charleston, South Carolina, 1,800 guest researchers from all over the world, and 850 users of facilities. The 8 measurement laboratories are: Building and Fire Research, Chemical Science and Technology, Electronics and Electrical Engineering, Manufacturing Engineering, Materials Science and Engineering, Physics, Technology Services, and Information Technology. There are three Nobel laureates in Physics working at NIST: Bill Phillips (1997), Eric Cornell (2001), and Jan Hall (2005).

NIST serves a broad base of customers in environmental technologies, transportation, pharmaceuticals, law enforcement, food and nutrition, biotechnology, computer software and equipment, construction, manufacturing, and microelectronics. In serving these customers, NIST partners with companies, National Laboratories, academia, and other Agencies of the State and Federal governments.

The Microelectronics Industry

In 1990, the U.S. Congress created the National Semiconductor Metrology Program (NSMP) to address the metrology needs of the semiconductor industry. NIST, in turn, created the Office of Microelectronics Programs (OMP) to manage these programs internally. OMP funds researchers in different NIST laboratories to address semiconductor industry needs. Personnel from OMP spend significant time working with semiconductor companies, e.g., IBM, Intel and TI; consortia, e.g., the Semiconductor Research Corporation (SRC), the Semiconductor Equipment and Materials International (SEMI) and SEMATECH; and academia. These interactions allow the NIST researchers to stay current on the fast changing, increasingly demanding, industry needs. In 2007, NIST joined the Nanotechnology Research Initiative (NRI), part of the Semiconductor Research Corporation (SRC), by contributing $2.8M a year for five years starting in 2007.

OMP has research programs in the following areas: Lithography, Critical Dimension and Overlay, Front-End Processing, Interconnect and Packaging, Process, Analysis Tools and Techniques, Device Design and Characterization, System Design and Test, and Manufacturing Support. There are several projects within each program area being conducted throughout NIST.

The Semiconductor Industry Association (SIA) has developed a way of communicating with research institutions to inform them of their needs in the future called the International Technology Roadmap for Semiconductors (ITRS) which is published every two years with an update on the intermediate years. Table I shows one of the tables in the 2007 ITRS[(3)] indicating the critical dimensions (CD) expected during the forthcoming years for the different products that the industry manufactures. CD is the minimum width of the lines printed on a chip. There are different definitions depending on the type of chip. Table II[(3)] shows a typical depiction of some properties that, according to the ITRS, will be of important in future years for different technologies. The ITRS uses a color code to identify the state of the technology that addresses those issues: white indicates that manufacturable solutions exist, and are being optimized; yellow, manufacturable solutions are known; and red, manufacturable solutions are not known. When interim solutions are known, a white background with yellow lines and a red rhombus appears.

	Table 1a&bProduct Generations and Chip Size Model Technology Trend Targets					
	Year of Production	***2007***	***2008***	***2009***	***2010***	***2011***
	Flash ½ Pitch (nm) (un-contacted Poly)(f)	**54**	**45**	**40**	**36**	**32**
WAS	*DRAM ½ Pitch (nm) (contacted)*	65	57	50	45	40
IS	***DRAM ½ Pitch (nm) (contacted)***	68	59	52	45	40
IS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	68	59	52	45	40
WAS	***MPU Printed Gate Length (nm)***	**42**	**38**	**34**	**30**	**27**
IS	***MPU Printed Gate Length (GLpr) (nm) ††***	**54**	**47**	**41**	**35**	**31**
WAS	***MPU Physical Gate Length (GLph) (nm)***	**25**	**23**	**20**	**18**	**16**
IS	***MPU Physical Gate Length (GLph) (nm)***	**32**	**29**	**27**	**24**	**22**
WAS	***ASIC/Low Operating Power Printed Gate Length (nm) ††***	**54**	**48**	**42**	**38**	**34**
IS	***ASIC/Low Operating Power Printed Gate Length (nm) ††***	**64**	**54**	**47**	**41**	**35**
WAS	***ASIC/Low Operating Power Physical Gate Length (nm)***	**32**	**28**	**25**	**23**	**20**
IS	***ASIC/Low Operating Power Physical Gate Length (nm)***	**38**	**32**	**29**	**27**	**24**
ADD	***ASIC/Low Standby Power Physical Gate Length (nm)***	**45**	**38**	**32**	**29**	**27**
ADD	***MPU Etch Ratio GLpr/GLph (nm)***	**1.6818**	**1.6039**	**1.5296**	**1.4588**	**1.4237**

Table I. Part of the Product Generation and Chip Size Model Technology Trends-Near Term Years from the ITRS 2008 update to the 2007 version.

Table MET2	*Metrology Technology Requirements*				
Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*
Microscopy					
Inline, nondestructive microscopy process resolution (nm) for P/T=0.1	**0.22**	**0.2**	**0.18**	**0.16**	**0.14**
Microscopy capable of measurement of patterned wafers having maximum aspect ratio/diameter (nm) (DRAM contacts) [A]	**16**	**17**	**17**	**>20**	**>20**
	76	**67**	**60**	**50**	**40**
Materials and Contamination Characterization					
Real particle detection limit (nm) [B]	**25**	**22**	**20**	**18**	**16**
Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	**22**	**19**	**17**	**15**	**13**
Specification limit of total surface contamination for critical GOI surface materials (atoms/cm^2) [C]	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**
Surface detection limits for individual elements for critical GOI elements (atoms/cm^2) with signal-to-noise ratio of 3:1 for each element	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**

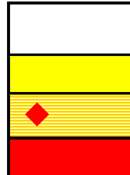

Table II. Part of the Metrology Requirements Table from the 2007 ITRS.

We will now address in more details some of the OMP supported projects.

Discussion of Pr3ojects

Spintronics

As device dimensions shrink to below about 200 nm the spin degree of freedom allows for new ways to control and manipulate magnetism. What could previously be done only with applied magnetic fields can now be done with spin polarized currents flowing through device structures. This has allowed the investigation and development of a number of new device concepts. The fundamental reason for this is that in nanostructured devices the angular momentum associated with the electron spins in a current, can now be coherently transferred to the magnetization state of a ferromagnetic material.

NIST is developing the metrologies to understand these interactions with a particular focus on how these new effects can be harnessed for new devices. We are focusing on how these spin interactions can be used to generate new kinds of nanoscale microwave devices and to control magnetization for information storage in magnetic RAM, as well as more "far out" ideas to develop spin batteries, spin-voltage readout schemes, and spin based logic concepts. See Fig.1.

Figure 1. (top) This shows the basic concept behind the "spin transfer" effect: that information from one magnetic layer can be coherently transferred to another through spin polarized electroncs. This provides a new means of controlling and manipulating magnetism. (bottom) This effect holds the promise to allow the development of spin batteries, efficient readout of high frequency information, and new spin-based logic. The basic concepts behind these devices have been experimentally demonstrated. The focus of the NIST spin electronics program is to investigate their performance in practical device architectures.

Other aspects that NIST is also considering are looking at architectures that use spinwaves to transmit and receive information. One example of this is shown in Fig. 2 where we fabricated two spin based high frequency oscillators about 500 nm apart on a magnetic film.

The most mature field that these new spin interactions has found potential application is in the area of magnetic random access memory (MRAM). The basic idea of MRAM is shown in the

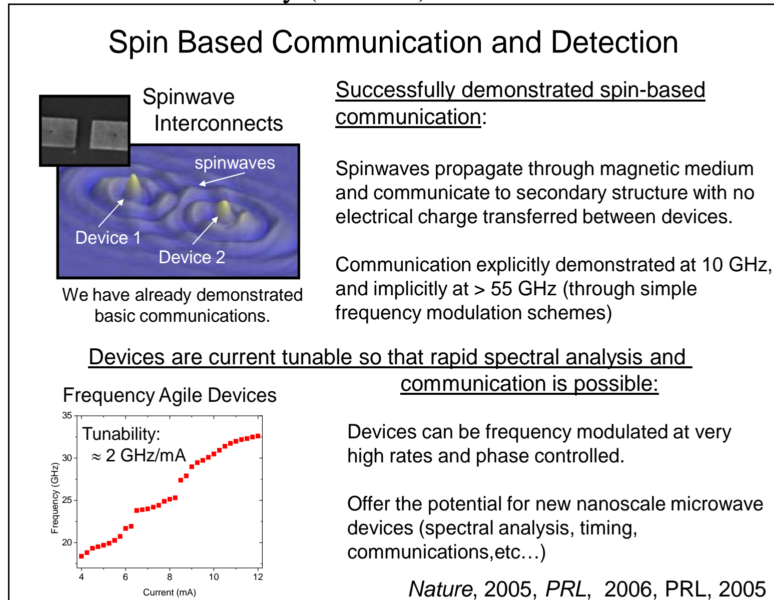

Figure 2. (top) Micomagnetic simulation of spin-based communication between two spin oscillators. The devices transfer information without any electrical charge transfer between them. This experimental demonstration was performed at 10 GHz. (bottom) Output from a single device showing that the oscillator frequency can be tuned between 20 GHz and 30 GHz by varying the current through the device. More recent results show devices working as high as 55 GHz.

upper left of Fig. 3. The simplest incarnation of MRAM has two magnetic layers. One of these is engineered to be fixed (as the reference layer) and the other is made to point left or right and acts as the storage layer. A more complete description could be found in the references (

Carbon Nanotubes and Graphene

Carbon based materials have interested many scientists and engineers as potential materials for future semiconductor manufacturing.

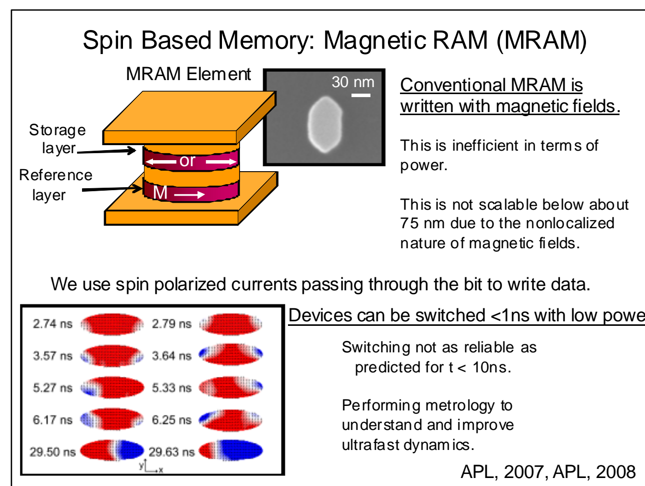

Figure 3. (top) Schematic of an MRAM device along with an SEM view of an indivual MRAM element (patterned at Hitachi Global Storage Technologies (HGST)). (bottom) Micromagnetic simulations (from a simulator developed at NIST (OOMMF)) suggest that the details of the reversal (switching) process are more complicated than typically assumed. Understanding the details of the switching process is expected to be crucial to the future development of MRAM.

Graphene can be thought of as a two dimensional structure composed of rings of six carbon atoms each. They are related to graphite, but graphite is a 3-dimensional structure that can be thought of as layers of graphene superimposed on one another. So, technically, graphene is a monolayer material, but bi-layers, tri-layers, etc. have been shown to have electrical properties similar to monolayer graphene. NIST is developing metrology techniques to measure accurately the properties of graphene.

Carbon nanotubes (CNTs) can be thought of as rolled sheets of graphene. CNT's can be either a single-walled (SWNT) or multi-walled nanotubes (MWNT). They have properties of great interest and measuring those properties has been a challenge because CNTs are usually prepared under which impurities and non-CNT's carbon compounds are included with the CNT's. Some NIST researchers have developed a laser cleaning system that is discussed in Figs. 4 through

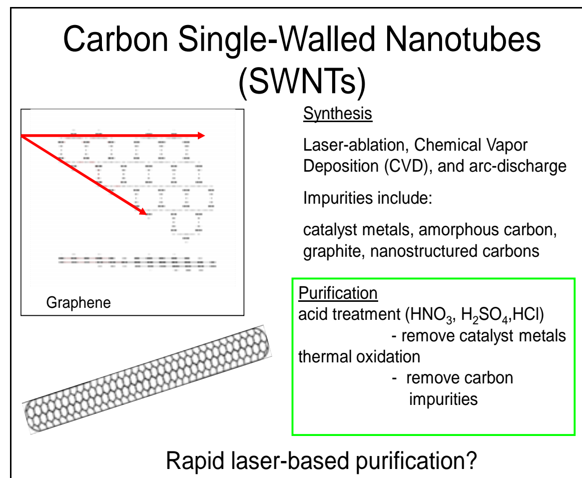

Figure 4. Description of the preparation and purification on single-walled carbon nanotubes.

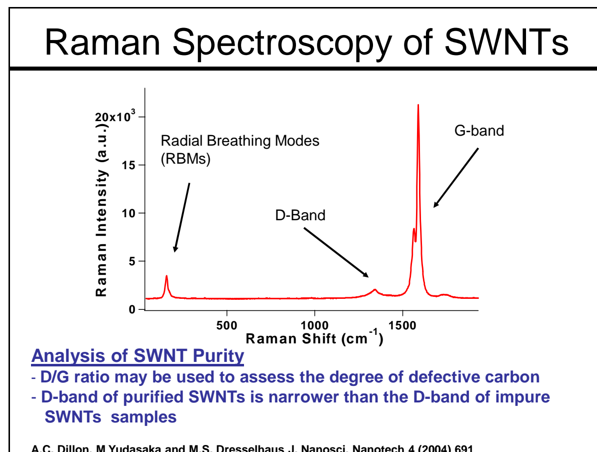

Figure 5. Raman spectrum of SWCNT

Other applications will be discussed during the presentation.

Conclusions

NIST's support has been and still is critical for the metrology needs of the semiconductor industry. Programs at NIST that are directed to this industry has provided needed techniques and methodologies that have allowed the industry to progress rapidly into areas

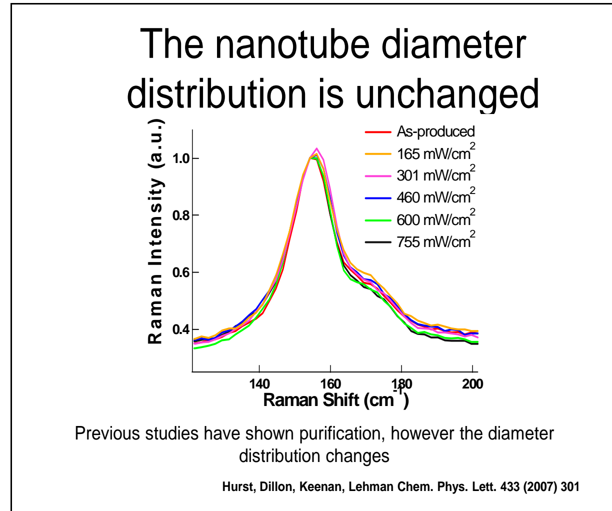

Figure 6. The CNT diameter is unaffected by the laser treatments.

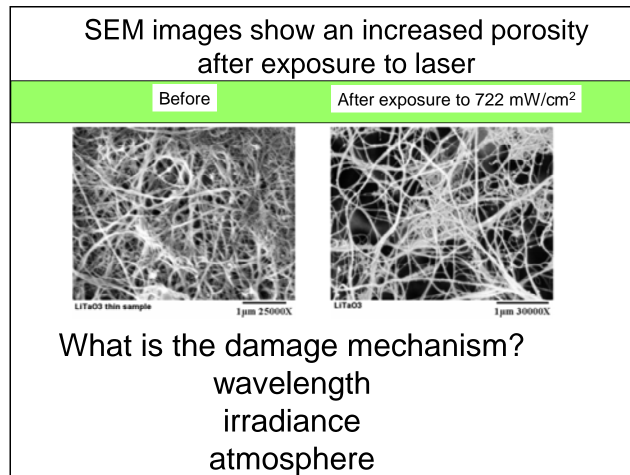

Figure 7. Laser exposure enhances the porosity of the matrix where the CNTs are embedded.

Acknowledgements

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References

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