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Channel Hot-Carrier Effect of 4H-SiC MOSFET

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Abstract. SiC MOSFET, as power device, can be expected to operate with high drain and high gate voltages, possibly leading to hot-carrier effect. However, hot-carrier degradation in a SiC MOSFET is difficult to detect because the as fabricated devices contain high level of defects. We report, for the first time, evidence of hot-carrier effect in 4H-SiC MOSFET. The result suggests that hot hole from impact ionization trapped in the oxide is the cause of the channel hot-carrier effect.

Introduction

Strong channel carrier heating, particularly at the drain end is expected for MOSFETs operating at high drain voltage. There will be a finite fraction of channel carriers at the Boltzmann tail energetic enough to surmount the energy barrier at the semiconductor/oxide interface, leading to the hot-carrier effect - a gradual degradation of device parameters [1]. For SiC power MOSFET during the transition from ON to OFF or vice versa, there will be transient periods where both the gate and the drain voltages are relatively high, possibly causing hot-carrier effect. However, for SiC, it is not easy to detect hot-carrier effect even if it exists, because the high density of defects already exist in the gate dielectric, the interface, and the channel region. To look for indications of hot-carrier effect, we must not rely on the conventional methods.

Experiments

For silicon nMOSEFT, the standard hot-carrier stress is the maximum substrate current condition ($V_G \sim ½\ V_D$). In a SiC MOSFET, a search for peak substrate current condition is not practical because of high junction leakage. Considering the stress condition that will most likely to occur in the operation of a power MOSFET, we decided to use the $V_G = V_D$ stress condition. Without making any assumption degradation, we monitor all terminals of the transistor to see what stands out.

Ring shaped 424 μm × 5 μm SiC nMOSFETs with 75 nm thick NO-annealed gate oxide were used. Two different drain bias were employed during stress for comparison (V_G = 20 V, V_D = 20 V and V_G = 20 V, V_D = 0.1 V). Transfer curves were measured before and after stress as a function of time (five curves per decade starting from 1 second after stress). Threshold voltages (V_{TH}) were extracted at I_D = 1 μA. All transistor measurements were done with V_D = 0.1 V and V_G sweeps from –1 V to 2 V.

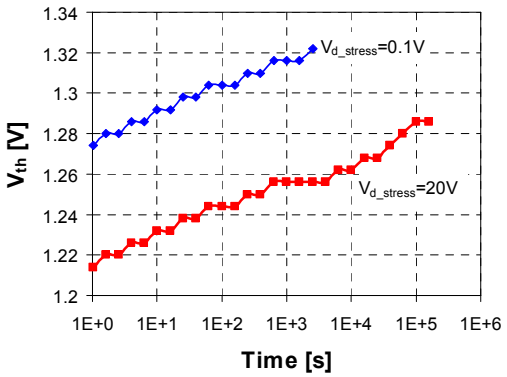

Fig. 1 V_{TH} shifts as stress time increases at two stress conditions. (V_G=20V, V_D=20V and V_G=20V, V_D=0.1V)

Results and Discussions. Fig. 1 shows the V_{TH} shift as a function of stress time for V_G = 20 V, and V_D = 20 V and 0.1 V (from two separate devices). Hot-carrier effect in silicon-based nMOSFET

typically increases interface state density, leading to V_{TH} shift and G_M degradation. For SiC, the interface state density is rather high to begin with. The observed V_{TH} shift may not be a consequence of interface state density increase. On the other hand, for nitrided gate oxide the high gate voltage alone can lead to bias-stress-induced threshold voltage instability [2] resulting from the trapping of electrons. The fact that V_{TH} shifts as a function of stress time is similar for both stress conditions clearly suggests that the electron trapping is due to bias instability, not channel hot-carrier effect.

Fig. 2 shows the drain current (in absolute value, thus the dip is where the current changes sign) in the region well below threshold as a function of stress time. Only the drain current before stress is positive all through the V_G sweep. For all post stress sweeps, an initial transient current that is dependent on stress time is clearly evidenced. Furthermore, the gate voltage at which the drain current starts rising (diffusion current) changes significantly with stress. In comparison, the evolution of transfer curve for the low-drain-voltage stress condition is shown in Fig. 3. The characteristic before stress is naturally similar to that in Fig. 2, while the behavior after stress is very different. There is no stress dependent initial transient current, and the sign of the drain current never change. Thus it is obvious that the transient current at the beginning of V_G sweep is due to high drain bias.

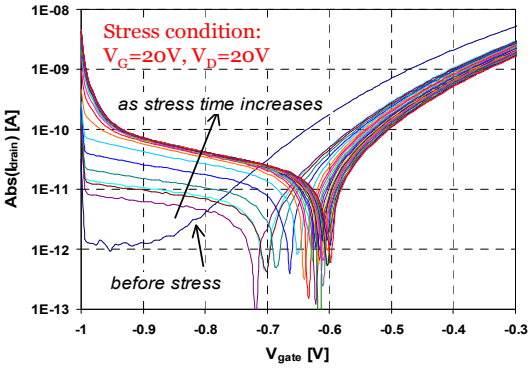

Fig. 2 I_D versus V_G before stress and after stress as time increases in log scale (five curves per decade starting from 1 sec). The stress condition is V_G = 20 V and V_D = 20 V. The dips correspond to the sign change of the drain current.

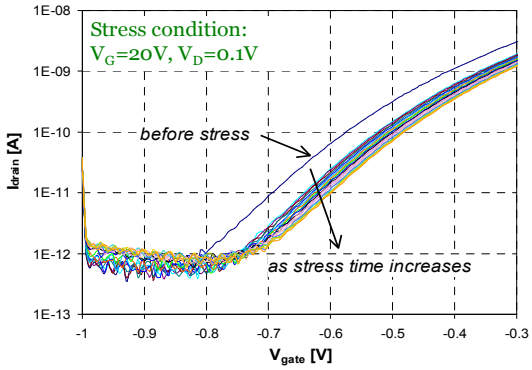

Fig. 3 I_D versus V_G before stress and after stress as time increases in log scale (five curves per decade starting from 1 second). The stress condition is V_G = 20 V and V_D = 0.1 V.

To clarify this transient behavior, we plot the currents from all four terminals plus the sum of all currents at the initial sweep of the gate voltage (- 1 V to - 0.9 V) for before stress, after a short stress, and after a long stress in Fig. 4a, 4b, and 4c respectively. An important point to note is the current sum. Since the wafer (and the wafer chuck) is isolated, the current sum should be zero except when the device serves as a source of charge. The before stress measurement shows a net out-flow of electrons from the device (Fig. 4a). Immediately after even a short stress, the current sum changes sign and become a net in-flow of electrons (Fig. 4b). The magnitude of this electron in-flow is much larger and grows with stress time (Fig. 4c). The initial out-flow of electrons is the characteristic of a very high density of interface states. When the gate voltage shifts from floating to negative, the Fermi level change forces many of the interface states to change from negative to positive, creating an excess of electrons. After stress, the net in-flow of electrons suggests large amount of trapped holes is being neutralized. Longer stress leads to more trapped holes.

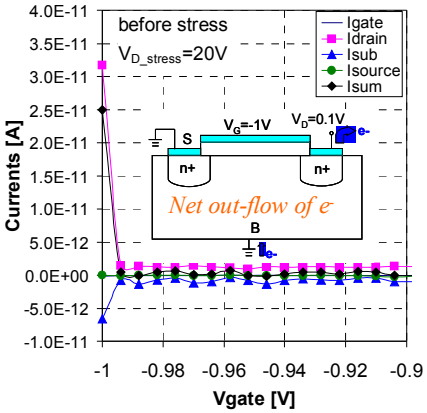

Fig. 4(a) Measurement of all the currents before stress for high-drain-voltage stress condition. The net current shows an out-flow of electrons.

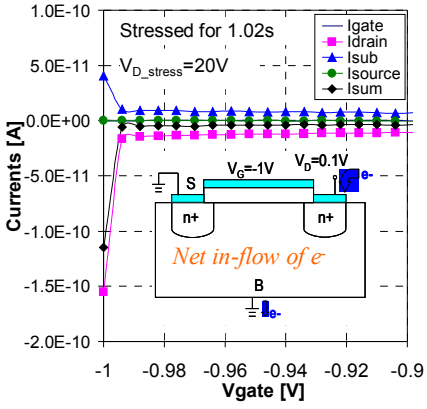

Fig. 4(b) Measurement of all the currents after short stress for high-drain-voltage stress condition. The net current shows an in-flow of electrons.

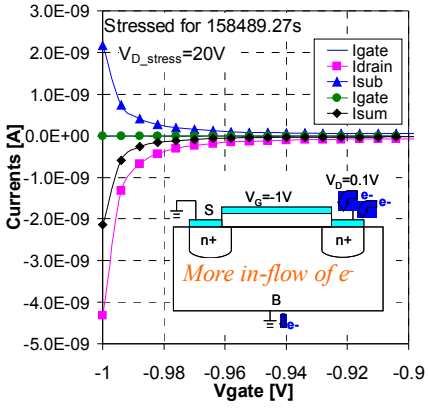

Fig. 4(c) Measurement of all the currents after long stress for high-drain-voltage stress condition. The net current shows more in-flow of electrons.

For comparison, Fig. 5a, 5b, and 5c shows the same before stress, after a short stress, and after a long stress cases for the condition of V_G = 20 V, V_D = 0.1 V. The behavior before stress is naturally the same. However, the after stress behaviors are quite different. The sign of net charge flow does not change and it does not grow with stress time. Clearly, without a high drain bias, the high density of trapped holes cannot build up. Thus we can conclude that the observed hole-trapping when the stress was with V_D = 20 V is due to channel hot-carrier effect.

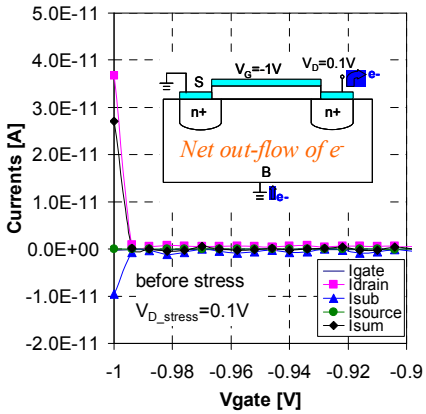

Fig. 5(a) Measurement of all the currents before stress for low-drain-voltage stress condition. The net current shows an out-flow of electrons.

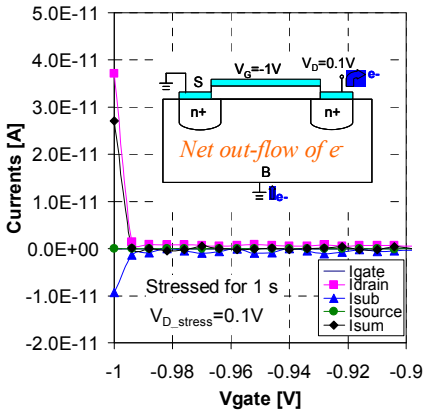

Fig. 5(b) Measurement of all the currents after short stress for low-drain-voltage stress condition. The net current shows an out-flow of electrons.

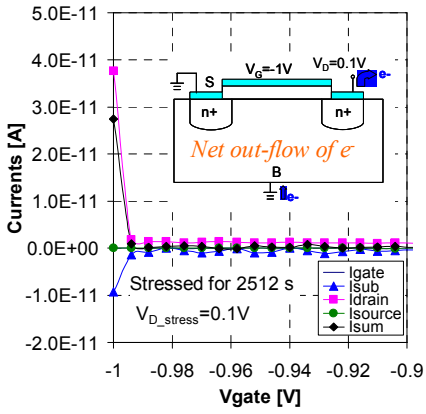

Fig. 5(c) Measurement of all the currents after long stress for low-drain-voltage stress condition. The net current shows an out-flow of electrons.

In Fig. 2, the drain current changes sign at higher gate voltage with longer stress time. The negative drain current indicates that trapped holes are being neutralized. The trapped holes near the drain end locally create a more positive electric field, and a wider depletion region. Due to the high density of defects, one would expect an increase in drain junction leakage current. This is indeed observed. The correlation between trapped holes density and junction leakage (measured as the I_{sub}) is plotted in Fig. 6 as a function of stress time. The gate voltage at which I_D = - 10 pA is employed as an indication of the trapped holes density. More trapped holes should shift the V_G @ I_D = - 10 pA to more positive. At each stress time, I_{sub} is extracted at V_G = - 1 V and - 0.9 V. They are plotted in Fig. 6 along with the V_G@I_D = - 10 pA. A clear correlation is obvious. Note that I_{sub} @ V_G = - 0.9 V is smaller because some of the holes are neutralized by the time the gate voltage is swept from - 1 V to - 0.9 V.

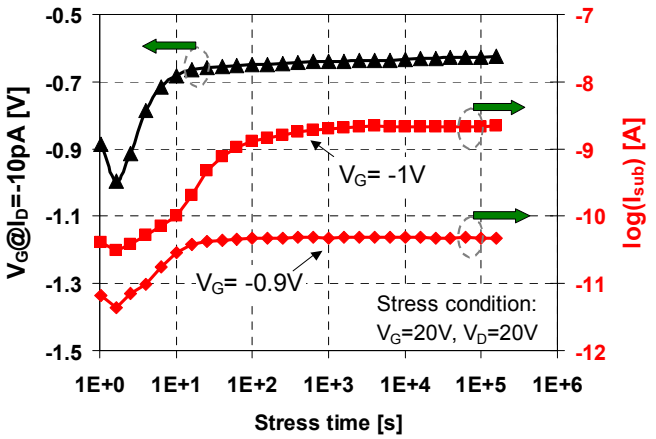

Fig. 6 Correlation, as a function of stress time, between the number of trapped holes, indicated by the gate voltage at which I_D = -10 pA, and the junction leakage current between the drain and substrate (I_{sub}). Stress condition used: V_G=20V and V_D=20V.

In hot-carrier stress on n-MOSFET, hot electrons are the problem. In our case, we are not using the common nMOSFET stress condition. Nevertheless, it is still fair to ask what the source of the trapped holes is during stress. One possible mechanism of hole-trapping is illustrated in Fig. 7. Channel electrons are heated up by the high electric field in the pinch-off region near the drain junction. The average electron energy (temperature) peaks at the drain junction and the thermalized electron population obeys the Maxwell-Boltzmann distribution. There will always be a fraction of the electrons at the distribution tail energetic enough to create electron-hole pairs through impact ionization. The hole generated will be swept backward to the channel. Falling backward through the depletion region, where the field is the highest, give these holes an energy kick substantial enough to overcome the oxide barrier. Since both V_D and V_G are 20 V, the vertical electric field near the drain is zero. Some of the energetic holes can be scattered towards the SiO_2 and be trapped in the oxide.

The phenomenon of holes gaining substantial energy by falling back through the depletion region is well established and has been employed to enhance the programming of floating gate based flash

memory through secondary impact ionization [3]. However, in our bias condition, there is no vertical field repelling the holes and secondary impact ionization is not necessary to result in hole-trapping.

Hole-trapping near the drain end can also explain the I_D-V_G characteristic measured after stress. With the MOSFET biased in the linear region (V_D = 0.1 V), the holes trapped near the drain will make that region change from accumulation to depletion earlier than the rest of the channel. This allows holes to detrap at gate bias below threshold, leading to the initial transient net in-flow of electrons as shown in Fig. 4. Since our I_D-V_G measurements scan from -1 V to 2 V and the scan rate is not fast, by the time when the threshold (I_D = 1 μA) is reached, all of the trapped holes at the drain end have been neutralized. This explains why the V_{TH} shifts shown in Fig. 1 are the same for both stress conditions.

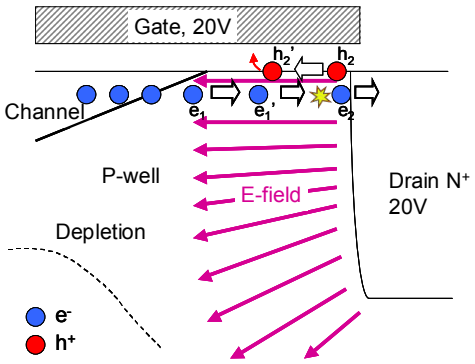

Fig. 7 Possible mechanism for hole trapping due to channel hot-electrons at high-drain-voltage stress condition.

Another factor that makes hole-trapping easier in SiC MOSFET is the smaller hole-injection barrier. The valence band offset of SiC is much smaller compared to that of Si (3.05 eV versus 4.75 eV) [4], therefore it is much easier for holes to be trapped in SiC MOSFET.

A natural question is that for the n-channel MOSFET with a large amount of hot channel electrons, why wouldn't the hot-electrons inject into the oxide and recombine with those trapped holes, especially when the conduction band offset in SiC is smaller than the valence band offset (2.7 eV compared with 3.05 eV)? The possibility of hot-electron injection increases exponentially in the pinch-off region. If there is any electron injection it should peak very close to the drain. On the other hand, the energy for holes traveling backward peaks in the pinch-off region near the channel. The two kinds of injection are therefore separated by a certain distance, and cannot easily recombine. However, in our measurements the electron trapping is not observed. This may be due to the way we measure the I_D-V_G characteristic. V_D = 0.1 V was applied before the V_G sweep with a time gap in the order of hundreds of microseconds. During this time gap, the trapped electrons may have been fully detrapped hence it is not recorded in the measurements. Careful thoughts on the experimental details are needed for future investigations.

Summary

In conclusion, we found evidence that channel hot-carrier effect does exist in SiC MOSFET operating at moderate (for power device) drain bias. The larger than expected effect is most likely due to impact ionization and hole-trapping. This effect manifest itself not in the traditional way usually associated with silicon MOSFET. As a result, exactly how the hot-carrier effect affects the reliability of the SiC MOSFET will require a new way of thinking.

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