FULL PAPER

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The Effect of Interfacial Roughness on the Thin Film Morphology and Charge Transport of High-Performance Polythiophenes**

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We control and vary the roughness of a dielectric upon which a high-performance polymer semiconductor, poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophene) (pBTTT) is cast, to determine the effects of roughness on thin-film microstructure and the performance of organic field-effect transistors (OFETs). pBTTT forms large, well-oriented terraced domains with high carrier mobility after it is cast upon flat, low-surface-energy substrates and heated to a mesophase. Upon dielectrics with root-mean square (RMS) roughness greater than 0.5 nm, we find significant morphological changes in the pBTTT active layer and significant reductions in its charge carrier mobility. The pBTTT films on rough dielectrics exhibit significantly less order than those on smooth dielectrics through characterization with atomic force microscopy and X-ray diffraction. This critical RMS roughness implies that there exists a condition at which the pBTTT domains no longer conform to the local nanometer-scale curvature of the substrate.

1. Introduction

Polymer semiconductors enable new modes of electronics fabrication because they can be deposited from solution[1–8] and patterned by printing on flexible substrates.[9–14] This advantage, however, makes the semiconductor microstructure dependent on many variables, including the chemistry and morphology of the dielectric upon which it is deposited. The roughness of the dielectric in particular is expected to strongly influence organic semiconductor microstructure because it influences the carrier mobility in organic field-effect transistors (OFETs),[15–20] which is strongly dependent on microstructure. Dielectric roughness may be a critical parameter for organic circuit fabrication because the solution-deposited dielectrics needed for flexible circuit applications are typically rougher than conventionally grown inorganic dielectrics. Understanding how dielectric roughness influences the microstructure and electrical performance of organic semiconductors is therefore a necessary first step towards the adoption of low-cost and flexible substrates, which are required to fully realize the benefits of organic semiconductors.[11–14,21,22]

Early studies on the impact of roughness on semiconductor morphology have generally focused on vapor-deposited small molecules such as pentacene. In these systems, the charge-carrier mobility generally decreases with increasing dielectric roughness, with a corresponding reduction of grain size.[17,19] This relationship is supported by demonstrations that carrier mobility can be increased by applying smoothing layers such as polystyrene[17] or poly(methyl methacrylate)[23] to rough oxide dielectrics. Recent work in solution-processable polymer semiconductors such as poly(9,9-dialkylfluorene-*alt*-triarylamine),[14,16] regioregular poly(3-hexylthiophene),[24] and poly(2,5-bis(3-tetradecylthiophen-2-yl)thieno[3,2-*b*]thiophene) (pBTTT)[15] has shown that charge-carrier mobility is reduced atop rougher dielectrics. The impact of dielectric roughness on film microstructure must be systematically established for highly crystalline, high-mobility polymer semiconductors such as polythiophene derivatives with regiosymmetric monomers.[25,26] Establishing these relationships will support the development of methods to repair or prevent the roughness-induced microstructure defects that can cause poor carrier mobility in these typically high-performing materials.

We evaluate the effect of dielectric roughness on the microstructure and field-effect hole mobility of thin films of solution-cast pBTTT. The molecular structure of pBTTT is shown in Figure 1.[25] pBTTT is one of a new class of polymer semiconductors that exhibit extensive 3D ordering in molec-

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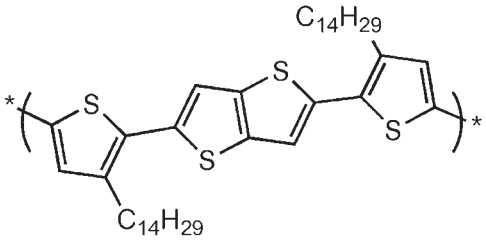

Figure 1. Chemical structure of poly(2,5-bis(3-tetradecylthiophen-2-yl) thieno[3,2-*b*]thiophene) (pBTTT-C_{14}), $M_n = 28$ kDa (1 Da $\approx 1.66 \times 10^{-24}$ g), polydispersity ≈ 2.

ular terraces,[27,28] making it an ideal material to assess the impact of dielectric roughness on the microstructure.

Dielectric roughness was controlled by exposing thermally grown silicon oxides to a reactive ion etch for various durations. The roughened dielectrics were then passivated with octyltrichlorosilane (OTS). This technique resulted in hydrophobic substrate chemistry with roughness varying from (0.3 to 3.0) nm. Atop these dielectrics of systematically controlled roughness, we cast and annealed thin films of pBTTT. We then evaluated how lateral domain size, intermolecular interactions, molecular orientation, and positional order depend on dielectric roughness. Changes in film microstructure are correlated to changes in the saturation hole mobility of OFETs fabricated atop the same dielectrics. A relatively small dielectric roughness (≈0.8 nm root-mean-square (RMS) roughness) can cause substantial disorder in pBTTT microstructure. The primary impact of increased roughness is a decrease in the lateral size of well-packed and well-aligned domains, which reduces carrier mobility by nearly three orders of magnitude. These results confirm that dielectric roughness is an important technical specification in flexible circuit design and fabrication.

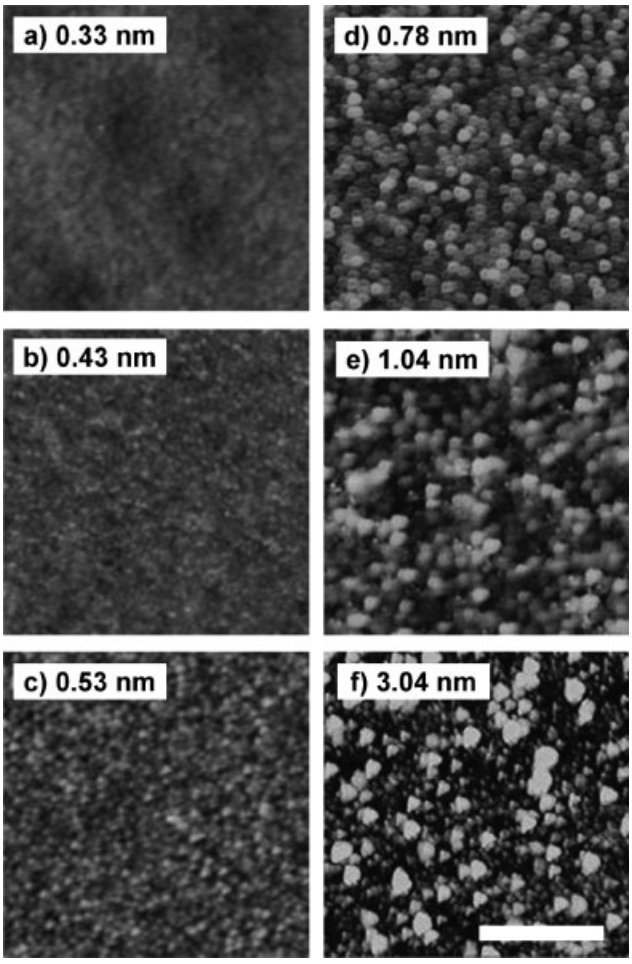

Figure 2. AFM height images of rough oxides after OTS passivation. All images have 10 nm vertical scales. Scale bar denotes 400 nm. Etching time of a) = 0; b) 10; c) 20; d) 40; e) 60; f) 120 s. RMS roughnesses are indicated on each image.

2. Results and Discussion

2.1. Substrate Characterization

To determine the impact of dielectric roughness on polymer semiconductor films, it is first important to characterize and quantify the dielectric roughness. RMS roughness is one of the useful metric used to quantify roughness on planar substrates. The RMS roughness is the square root of the averaged sum of height deviations taken from the mean data plane,

$$RMS = \sqrt{\frac{\sum (z_i - mean)^2}{n}} \quad (1)$$

where z_i is the height value at a certain point i and n is the number of points. A series of dielectrics with six different RMS roughness values were prepared by controlling the reactive ion etching time of 200 nm thick thermally grown silicon oxides. The oxides were initially quite flat, with RMS roughness ≈0.2 nm. Increasing etching time increases roughness. Figure 2 shows atomic force microscopy (AFM) images of the six oxide dielectrics after OTS passivation. The OTS passivation typically maintained or slightly increased the RMS roughness of the etched oxides.

The RMS roughness as defined above describes vertical variations in the rough surface. The lateral variations occur over a range length scale within the plane of the surfaces. The power spectral density (PSD) describes the contributions of different spatial frequencies to the RMS roughness.[16,20,29] PSD distributions of the OTS passivated, roughened oxides are shown in Figure 3. The overall power spectral density (PSD) increases with RMS roughness over the entire wavelength range from (15 to 1000) nm, indicating increasing fractal roughness. The RMS roughness at different length scales (Table 1) can be extracted by partial integration of the PSD.[30]

$$RMS = \sqrt{\int_{q=2\pi/\lambda}^{q} p(q)dq} \quad (2)$$

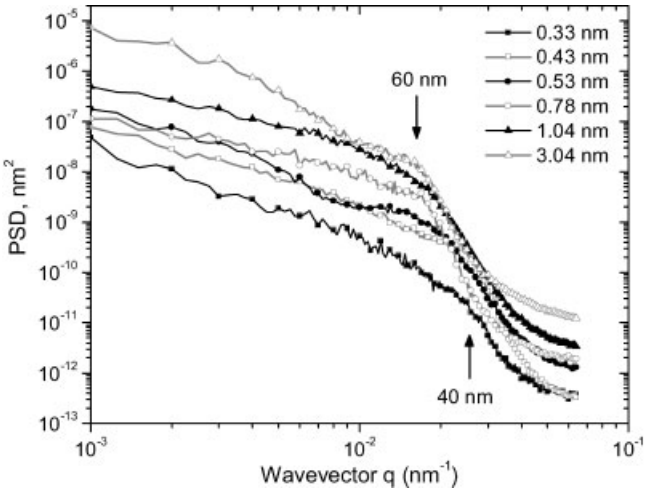

Figure 3. Power spectral density (PSD) curves versus wavevector q. PSD is calculated from AFM micrographs of rough surfaces. Prominent lateral length scales of 40 nm and 60 nm are indicated.

Where $q_0 = 6.4 \times 10^{-2}\ \mathrm{nm}^{-1}$, λ is the length scale, and $p(q)$ is the PSD as a function of q. We find for our dielectrics that the measured roughness at small length scales is directly dependent on that of the larger length scales, making it impossible to rigorously separate the effects of short-wavelength roughness from long-wavelength roughness as can be done for self-organized interfaces which are molecularly smooth but macroscopically rough.[16] For surfaces with RMS roughness less than 0.53 nm, this length scale is broadly distributed, about (30 to 50) nm. For surfaces with RMS roughness 0.78 nm or greater, the length scale sharpens to (55 to 60) nm. The features responsible for this length scale are visible as domains with circular boundaries in Figure 2d–f.

The etched and passivated silicon oxide dielectrics have characteristics appropriate to evaluate the impact of roughness on pBTTT microstructure and carrier mobility, because the length scales of the roughness variation are similar to the length scales of the pBTTT microstructure. When pBTTT is cast and annealed upon flat surfaces, it forms terraced domains of 2.1 nm in height that extend laterally hundreds of nanometers to micrometers.[27,28] It is reasonable to expect that pBTTT solidification atop (30 to 60) nm wide features with nanometer-scale height variation may substantially limit lateral terrace size and reduce carrier mobility.

Table 1. RMS roughness at different length scales.

Overall RMS roughness [nm]	Length scale		
	30 nm	60 nm	600 nm
0.33	0.008	0.04	0.26
0.43	0.009	0.08	0.39
0.53	0.013	0.09	0.44
0.78	0.014	0.13	0.72
1.04	0.016	0.14	0.97
3.04	0.026	0.17	2.50

2.2. Effect of Roughness on pBTTT Microstructure

Atomic force microscopy reveals that the micrometer-scale terraces of pBTTT films on flat surfaces can be entirely disrupted by solidification on the rough substrates. AFM images of pBTTT films cast on the roughened dielectrics are shown in Figure 4. The films were annealed by heating to a mesophase (≈180 °C) and then cooling. This mesophase annealing procedure increases the lateral domain size and improves order within domains.[27,28] Terraces atop the flattest dielectric (Fig. 4a) exhibit ≈ (100 to 400) nm lateral size (on the film surface) and ≈2.1 nm heights, consistent with previous reports and the X-ray diffraction (XRD) layer spacing.[27,28] As dielectric roughness increases, the domain size decreases, as shown in Figure 4b and c. Dielectrics with RMS roughness greater than 0.78 nm exhibit no terraces (Fig. 4d–f). There appears to be a critical RMS roughness between 0.53 nm and 0.78 nm where domain formation is disrupted. We note that the critical roughness for pBTTT domain disruption is similar to the threshold roughness required to decrease carrier mobility in amorphous poly(9,9-dialkyl-fluorene-*alt*-triarylamine),[14,16] evaluated at the 100 nm lateral length scale.

The critical RMS roughness may represent a condition at which the pBTTT domains can no longer conform to the local nanometer-scale curvature of the substrate without an interruption in packing. The AFM images of the substrates provide some information about the magnitude of local nanometer-scale curvature, although the radius of curvature might be overestimated owing to convolution with the AFM tip, especially for the roughest films where the tip shape appears to be present in the image. The substrates with 0.53 nm RMS roughness exhibit an ≈80 nm minimum radius of curvature, whereas those with 0.78 nm roughness exhibit a sharper ≈50 nm minimum radius of curvature. Higher-amplitude roughness at longer lateral length scales may not impact pBTTT microstructure provided that the radius of curvature is large. These considerations have important implications for dielectric selection and optimization, especially for solution-deposited dielectrics. Polymer dielectrics with longer-wavelength roughness[14,16] might prove to be more suitable than nanoparticle inks with particles in the (10 to 100) nm range[31] or chemical-vapor-deposited dielectrics.[32] However, we note that roughness at the 100 nm length scale does appear to influence the carrier mobility of amorphous poly(9,9-dialkylfluorene-*alt*-triarylamine),[14,16] even though no morphological impact is observed.

The chemical nature of the dielectric surface chemistry also influences the lateral crystal size of pBTTT.[28] The pBTTT domains after annealing typically have a smaller lateral size on clean oxide dielectrics than on hydrophobic OTS-passivated dielectrics. The difference in domain size is attributed to a greater nucleation density on the clean oxide. Importantly, sharp pBTTT terrace edges are observed atop flat clean oxide despite the smaller lateral domain size. It has also been shown that pentacene nucleates more densely on rough dielectrics to create a greater number of well-defined smaller domains.[17,19]

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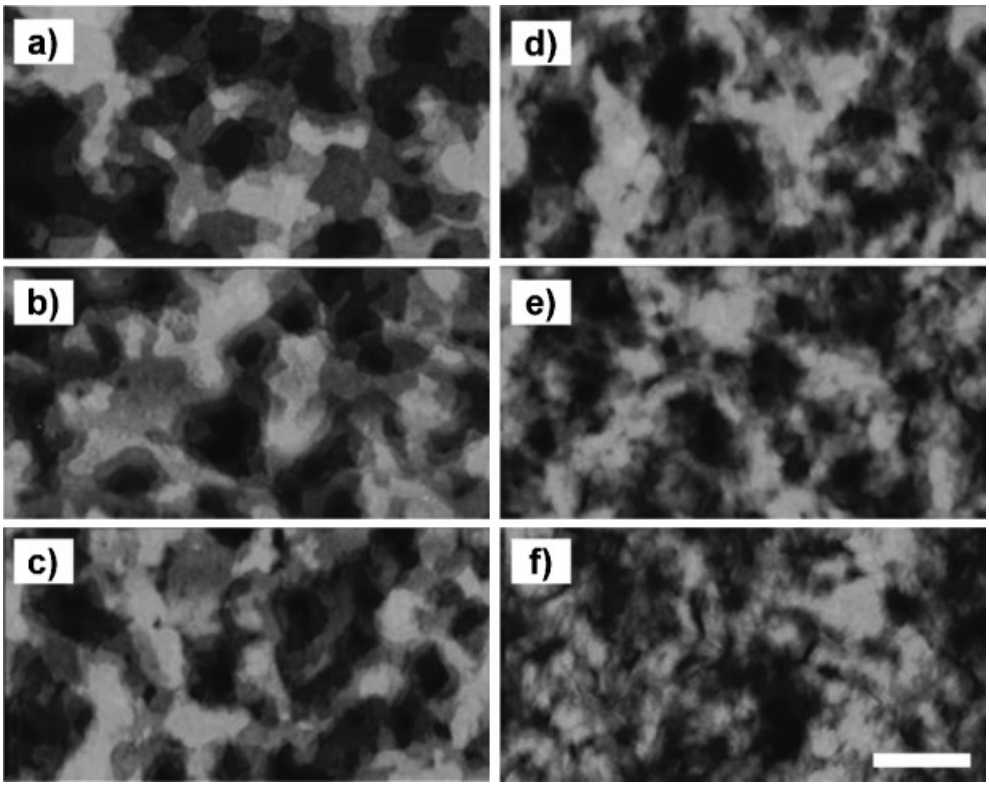

Figure 4. AFM images of pBTTT atop various rough surfaces after heating above the mesophase transition and then cooling. All images are 2 μm × 1 μm size and 20 nm height scale. Scale bar denotes 400 nm. The underlying silicon oxide layer roughnesses are a) 0.33; b) 0.43; c) 0.53; d) 0.78; e) 1.04; and f) 3.04 nm. Well-oriented terraces on a flat surface (a) become more nodulelike features as the bottom layer roughness increases.

In contrast, sharp pBTTT terrace edges are not observed atop roughened and OTS-passivated dielectrics. This comparison suggests that the mechanism of pBTTT terrace disruption on rough dielectrics is more complex than a simple increase in nucleation density. It is possible that conforming to a rough surface during terrace formation interrupts domain growth at especially sharp features on the dielectric, further limiting domain size and corrupting edge definition.

While microscopy shows that dielectric roughness disrupts the pBTTT microstructure at the lateral length scale of domains, additional characterization is required to determine whether molecular-scale packing within domains is affected. The quality of π-overlap within domains could influence carrier mobility more than the number or character of domain boundaries. Ultraviolet-visible (UV-Vis) absorption spectroscopy provides a means to evaluate intermolecular interactions at the molecular level, because the extent of intra- and intermolecular π-orbital delocalization are captured in the peak location and structure of the absorbance spectrum. As-cast films on quartz substrates with RMS roughness of (0.5, 0.8, 1.0, and 3.0) nm all exhibited similar spectra (not shown) with absorption maxima at 550 nm. After annealing, all spectra were red-shifted with nearly identical peak widths and absorption maxima at 563 nm (Fig. 5a and b). The lowest-energy shoulder of the absorbance spectrum (designated B

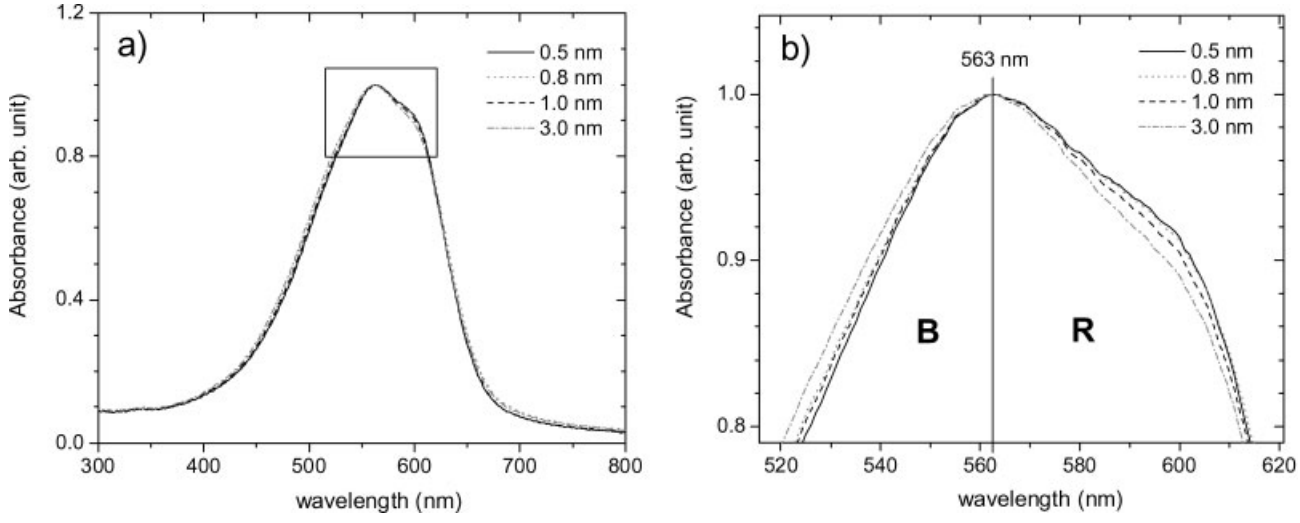

Figure 5. a) UV-Vis absorption spectra for thin films of annealed pBTTT on various rough quartz plates and b) enlargement of the marked area. B and R denote blue and red absorption region, respectively. Peaks are normalized by peak height to remove small variations due to film thickness.

on Fig. 5b) does decrease systematically by ≈0.8% as substrate roughness increases from 0.5 nm to 3.0 nm RMS. This indicates that π-orbital delocalization improves upon annealing to a similar extent regardless of roughness. Interfacial roughness therefore does not profoundly impact the molecular-scale packing or conformation of the pBTTT chains.

Although the molecular-scale packing of pBTTT is not influenced by dielectric roughness, it remains possible that roughness could influence molecular orientation because the dielectric surface is not flat at the molecular length scale. The orientation of pBTTT can be determined using near-edge X-ray absorption fine structure (NEXAFS) spectroscopy, which measures the absorption of polarized soft X-rays that excite electrons to molecular bound states. By collecting NEXAFS spectra at multiple incident angles, the surface-relative orientations of molecular resonances can be determined. The most strongly oriented resonance of the pBTTT system is the carbon K-edge $1s \rightarrow \pi^*$, which is a transition normal to the conjugated plane of the pBTTT backbone. The orientation of the π^* resonance is typically expressed as a dichroic ratio, R, which is greater than 0 for an edge-on conjugated plane, and is typically ≈0.4 for annealed pBTTT films on flat surfaces.[27] If the pBTTT molecules are assumed have a single surface-relative orientation, then $R \approx 0.4$ can be interpreted as a conjugated plane tilt within the pBTTT crystal of ≈21°, which is supported by first-principles modeling.[27] If pBTTT domains do tilt upon rougher dielectrics, then R will decrease with a lower bound of $R = 0$ for a random distribution of domain orientations. We note that R is more sensitive to domain tilts orthogonal to the pBTTT backbone than to tilts along it.

Carbon K-edge NEXAFS spectra of pBTTT films atop dielectrics of RMS roughnesses 0.33 nm and 1.04 nm are shown in Figure 6a. The intensity of the π^* resonance varies systematically with the angle of incidence, and can be fit to determine orientation,[33] as shown in Figure 6b. Both films exhibit R similar to that previously reported, as do films deposited on dielectrics with RMS roughness between 0.33 nm and 1.04 nm. The pBTTT film deposited atop the 3.04 nm roughness dielectric exhibited $R = 0.37 \pm 0.01$, which is lower than that of pBTTT films deposited on smoother dielectrics, but only by a small amount equally consistent with a ≈3° mis-tilt of domains or a ≈7% randomly oriented fraction. A red-shift of the π^* resonance location, which has been previously attributed to intermolecular packing differences in regioregular poly(3-hexylthiophene) P3HT,[34] is not observed regardless of roughness. In general, the NEXAFS analysis indicates that rough dielectrics do not substantially impact the pBTTT molecular orientation, although orientation may be modestly disturbed on very rough dielectrics.

The quality of long range positional order within pBTTT films can be evaluated with specular XRD.[35] The intensity and shape of the (200) Bragg peak collected as a two-dimensional pattern describes the extent of layer order, the thickness of domains of well-ordered layers, and whether there is layer tilt. Figure 7a shows example two-dimensional patterns

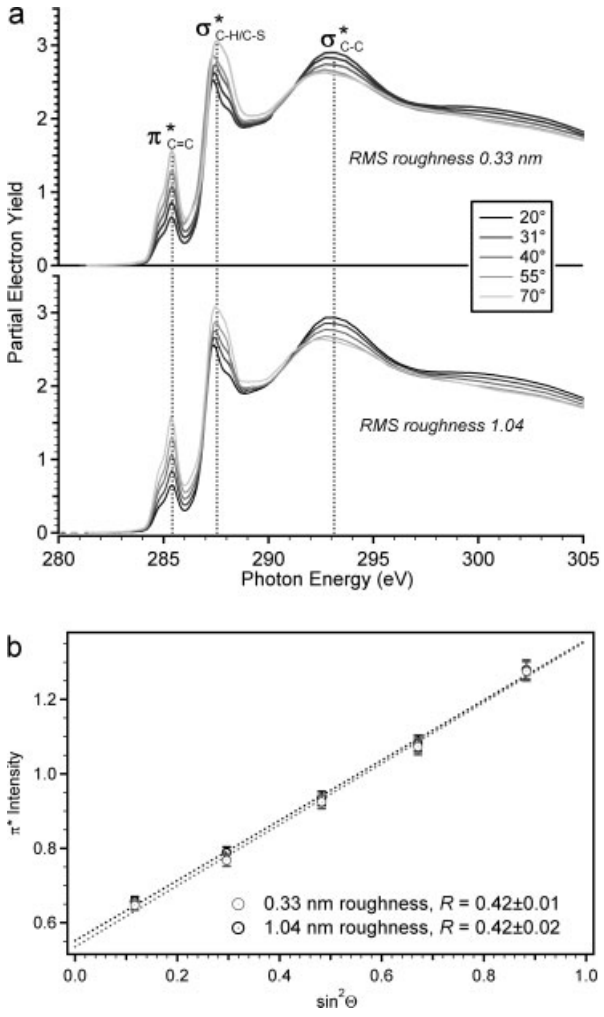

Figure 6. a) Carbon K-edge NEXAFS spectra of pBTTT films atop dielectrics of different roughness. b) Fit of π^* intensity vs. squared sine of incident angle used to determine molecular tilt.

for the cases of perfectly oriented crystals and for tilted crystals with a distribution of orientations. Perfectly oriented crystals result in an elliptical pattern where the vertical width (along q_z) of the ellipse is determined primarily by the thickness of the crystals perpendicular to the substrate and the horizontal width (along q_{xy}) is related to the lateral coherence of the (200) planes. The lateral coherence is determined by the degree of positional and orientational registration between the planes of neighboring domains. Defects such as dislocations will broaden the horizontal width.[36] Distributions of tilted crystals also will broaden the horizontal width, but will result in an arc pattern instead of an elliptical pattern.[35] The width of the arc will be determined by the tilt distribution, with an isotropic tilt distribution resulting in a ring. A rocking curve is a scan through reciprocal space along this arc. At small tilt angles, a rocking curve is essentially identical to a q_{xy} scan.

Figure 7b shows the (200) Bragg peaks of pBTTT films, from the scattered intensity along the q_z axis of the patterns in

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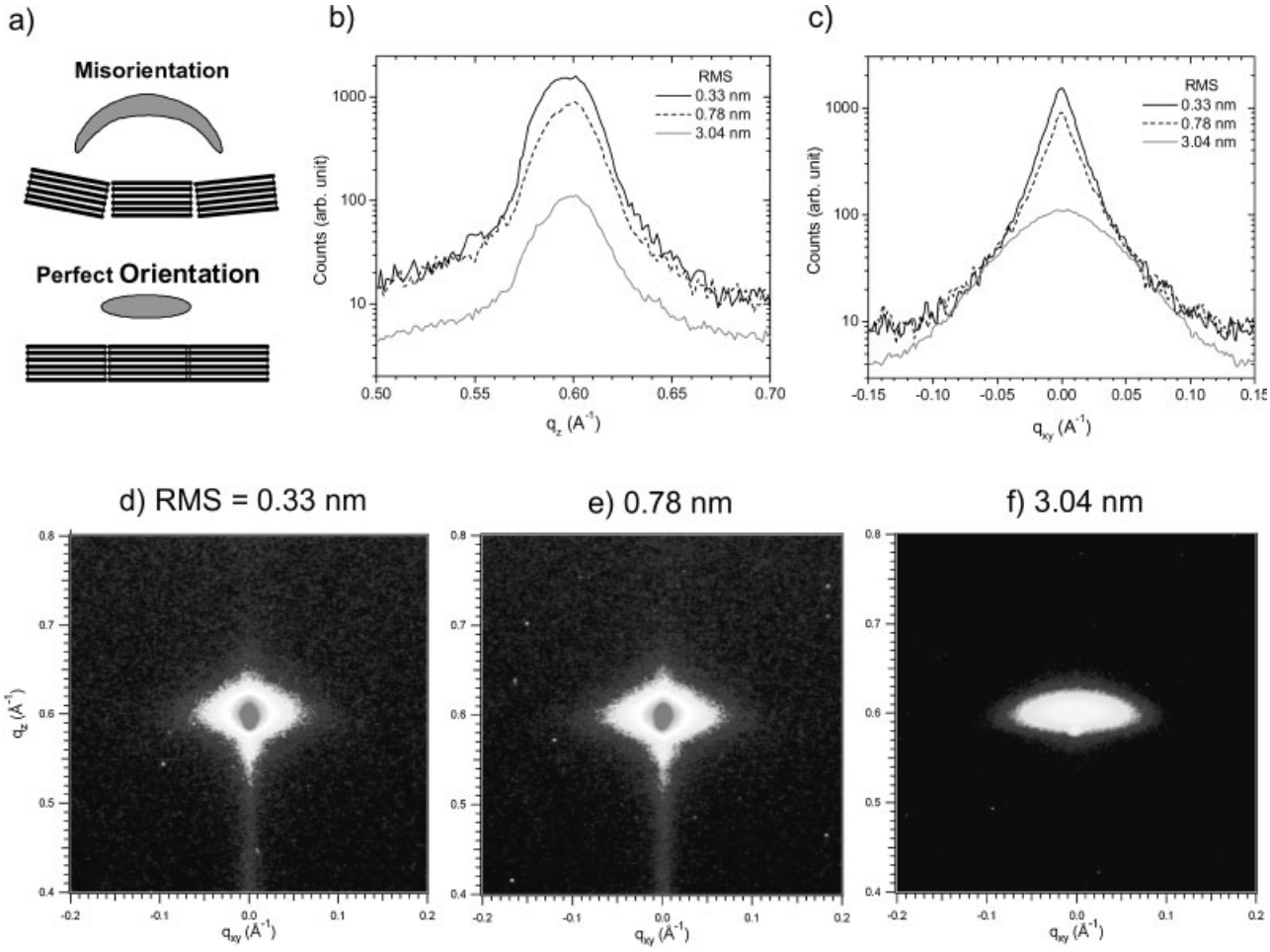

Figure 7. X-ray diffraction of annealed pBTTT on various roughness OTS treated substrates. a) shows expected diffraction spot shapes for cases of misoriented crystals and perfectly ordered crystals. b) q_z and c) q_{xy} of the (200) diffraction obtained from two-dimensional diffraction images near the Bragg condition. The reflected beam was subtracted from (b). d)–f) are two-dimensional X-ray diffraction images at the Bragg condition for each of the roughnesses plotted on the same intensity scale.

Figure 7d–f. Figure 7c shows rocking curves about the (200) Bragg peak, from the intensity along the q_{xy} axis of the patterns. The Bragg peak intensity decreases substantially for the pBTTT film on the roughest dielectric (3 nm), but the peak does not substantially broaden along the q_z or q_{xy} axes. The Bragg peak widths along q_z (Fig. 7b), which are similar for all three pBTTT films, indicates that diffracting layered domains extend vertically $2\pi/\Delta q_{FWHM} \approx 20$ nm (10 repeat units), which corresponds roughly to the entire pBTTT film thickness. The horizontal peak widths along q_{xy} indicate that the lateral coherence of the diffracting crystals is similar for all films and that the reduction in peak intensity is not due to a simple smearing of the diffracted beam into a larger region of reciprocal space.[37] Finally, all of the (200) peaks are elliptical patterns with no arc, indicating that there is not a significant population of tilted layers in the annealed pBTTT film on any of the substrate roughnesses investigated in this study. The lack of tilted layers becomes especially clear in comparison to as-cast pBTTT films on flat dielectrics, which have been shown to exhibit significant arcs in the (h00) Bragg peak series.[35]

The similar shapes of the Bragg peaks indicate that the diffracting domains have similar thicknesses and are well oriented, with no evidence for tilted crystals. The impact of dielectric roughness on pBTTT films is manifested in the XRD patterns primarily as a decrease in Bragg peak integrated intensity by a factor of ≈15 from the smoothest to roughest dielectric. This decreased peak intensity indicates that large portions of the roughest films do not have long-range order and therefore do not contribute to the diffraction. This result does not contradict the UV-Vis spectroscopy finding that roughness does not profoundly impact the molecular-scale packing or conformation of the pBTTT chains, because the UV-Vis absorption measurement evaluates interactions between neighboring chains within layers, whereas the XRD measurement evaluates longer-range order among multiple layers. Further, this result is quite consistent with the NEXAFS

analysis, which indicated negligible domain tilt regardless of dielectric roughness. Combining these results with those from AFM suggests a substantial decrease in the lateral size of the crystals on rough dielectrics and an increase in the number of areas with poor intermolecular interaction between domains.

The impact of dielectric roughness on the diffraction of pBTTT films observed here is larger than that of surface chemistry, where no decrease in Bragg peak intensity was observed.[28] This comparison further supports the hypothesis that the effect of dielectric roughness is not simply the enhancement of nucleation. Rather, the roughness may also substantially hinder the growth of well-ordered domains and result in the formation of defective crystals with paracrystalline order,[38] perhaps due to strain on rough substrates. A decrease in diffraction intensity has also been reported for pentacene films grown on rough dielectrics, which did not exhibit $h00$ Bragg reflections.[18]

2.3. Effect of Roughness on OFET Carrier Mobility

The disruption of pBTTT morphology by dielectric roughness should strongly impact OFET carrier mobility. Even though mobility will be influenced by carrier path and field distribution differences, the decreased lateral grain size atop rough dielectrics will exhibit a greater number of grain boundaries with poor π-overlap, which will limit carrier mobility. All the top contact OFETs exhibited saturation, and transfer curves showed a linear response of the square root of drain current to gate potential (Fig. 8). Saturation hole mobility was extracted from the linear slopes.

Typically, the hole mobility of pBTTT films increases by a factor of (1.5 to 2) after annealing, which involves heating above the mesophase transition and then cooling.[25,28] The hole mobility of as-cast films was similar for all dielectric roughnesses in the (0.002 to 0.02) $cm^2\ V^{-1}\ s^{-1}$ range, but exhibited a clear dependence on dielectric roughness after annealing, as shown in Figure 9. Increasing dielectric roughness causes a substantial reduction of the hole mobility of annealed devices. The hole mobility drops most remarkably at 0.78 nm RMS roughness where microscopy indicates that terraces are disrupted (Fig. 4) The hole mobility drops further by a factor of 400 from the smoothest to the roughest dielectric. The mechanism of mobility decrease in pBTTT on rough dielectrics is likely due to the combination of an increased number of lateral grain boundaries, which will limit transport between domains, and an increased number of packing defects which will limit transport within domains. The pBTTT hole mobility decrease on rough dielectrics is similar to that observed for pentacene (factor of 10)[17,19] and P3HT (factor of 100)[24] on rough dielectrics.

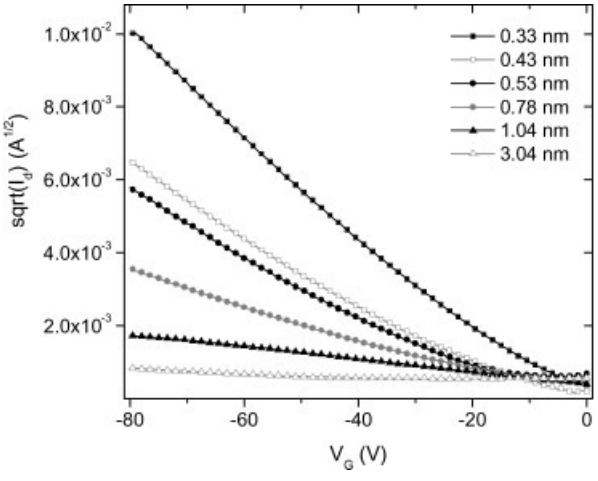

Figure 8. Representative transfer characteristics of bottom gate/top electrode OFET devices with annealed pBTTT semiconductors/rough oxide dielectrics. Linear regression between −80 V and −60 V was used to determine the saturation mobilities (μ).

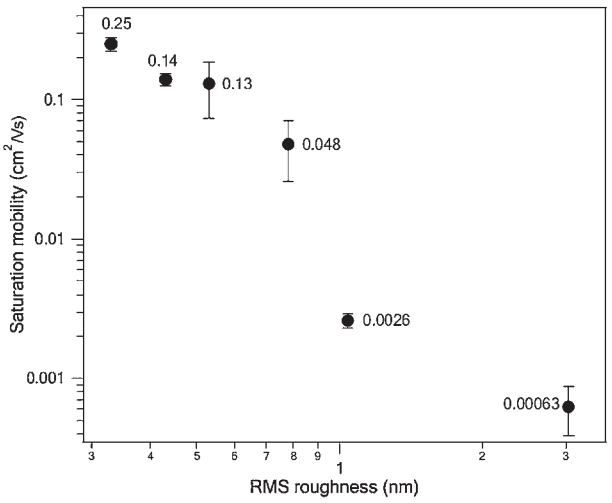

Figure 9. Charge carrier mobility (μ) plot for pBTTT thin film transistors after heating at mesophase for substrates of various dielectric roughness. Uncertainty for mobility is the standard deviation calculated from the distribution of saturation field effect mobilities.

3. Conclusion

We have shown that dielectric layer roughness strongly affects the morphology and charge transport properties of pBTTT. Because pBTTT forms highly oriented terraces on flat surfaces, changes in its microstructure atop rough dielectrics were especially clear. A critical value of roughness was observed between (0.5 and 0.8) nm where terraces were no longer observed in AFM and charge carrier mobility decreased substantially. Rough dielectrics alter the layered microstructure by reducing lateral domain size and decreasing the extent of long-range layer order, while the molecular conformation and the orientations of molecules and domains remain unchanged. These results provide fundamental evidence that roughness of dielectric interfaces is a critical

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parameter that must be addressed in the development of flexible electronics.

4. Experimental

To create rough gate dielectric layers, a series of rough oxides were prepared with a reactive ion etching (RIE) tool, Silicon RIE Unaxis-790 (Unaxis Wafer Processing, St. Petersburg, FL) located in the National Institute of Standards and Technology (NIST) nanofab facility.[39] For this, 200 nm thermally grown oxides (RMS roughness is ≈0.2 nm) on highly n-doped silicon wafers were used. During the etching process, CF_4 etching gas was supplied constantly at 40 sccm, the pressure inside the chamber was kept at 100 mTorr, and the power was 100 W which gives etching rate of 20 nm min^{-1}. By controlling the etching time, RMS roughnesses beween (0.3 and 2.9) nm could be obtained. After cleaning with Jelight ultraviolet-ozone cleaner for 10 min, the etched oxides were rinsed with water, dried thoroughly with nitrogen, and immersed in 0.002 mol L^{-1} OTS solution in hexadecane for 16 h. After OTS passivation, the substrates were cleaned by sonication with chloroform, isopropyl alcohol, and de-ionized water for 10 min in each solvent, then rinsed with isopropyl alcohol, and finally baked at 150 °C for 10 min. Hydrophobic surface with water contact angles of 108° to 115°, depending on roughness, were obtained. For UV-Vis measurements, quartz plates (initial roughness ≈0.5 nm) were etched following the same procedure used for the thermal oxide substrates. After passivation with OTS, a series of four quartz plates was obtained with (0.5, 0.8, 1.0, and 3.0) nm RMS roughness.

Semiconducting pBTTT (Fig. 1) was synthesized as reported previously. Films were cast from 75 °C, 0.4 mg mL^{-1} solutions in a solvent pair (chloroform:dicholorobenzene = 8:1) at (3000) 2π rad min^{-1} using a (100) 2π rad min^{-1} acceleration rate. All film processing was performed in a N_2 atmosphere. The polymer film thickness was ≈20 nm. The spun-cast films were heated to the pBTTT mesophase at 180 °C for 5 min, then cooled slowly to room temperature.

To obtain topographical images of the rough oxides and to examine terrace formation of pBTTT-C_{14} on rough oxides, an AFM (Dimension 3100, Veeco) was used in tapping mode. Fresh tips were used with each film. Scan size of images were obtained ranging from 1 μm to 10 μm to achieve a high lateral resolution and to detect feature length scales. With Nanoscope software, RMS values and the power spectral density (PSD) of the rough silicon oxide were analyzed over the complete scan area and the domain size on top of pBTTT was measured. NEXAFS spectroscopy was performed at NIST beamline U7A of the National Synchrotron Light Source (NSLS) of Brookhaven National Laboratory. Carbon K-edge collection was performed in partial electron yield (PEY) mode with a grid bias of −50 V. Spectra collected at the five incident angles, Θ, from 20° to 70° and were normalized with respect to carbon concentration by their intensity at 330 eV. XRD measurements were conducted using a laboratory-scale small-angle X-ray scattering instrument (Rigaku) with $MoK_{\alpha 1}$ radiation in conventional pinhole geometry. The incident beam, diffracted beam and sample chamber were under vacuum. An image plate (30 cm × 30 cm) was used to collect the two-dimensional scattering patterns. The sample was mounted in the specular geometry with the X-ray incidence angle set to the Bragg angle of the (200) peak (1.9°). A Perkin-Elmer Lambda 950 UV-Vis spectrometer was used to measure the absorption spectrum.

To measure carrier mobility, top contact source and drain gold electrodes were thermally evaporated on top of the pBTTT through a shadow mask. Pressure inside the chamber of the evaporator was maintained under 10^{-6} Torr and the electrodes were deposited to 60 nm with a deposition rate of 0.05 nm s^{-1}. On a sample size of 13 mm × 13 mm, 9 devices were deposited. The channel length (L) to width (W) ratios (W/L) of the devices were distributed as follows: 3 at 1000 μm/105 μm, 3 at 1000 μm/114 μm, and 3 at 2000 μm/122 μm. I–V measurements were performed in a Cascade Microtech probe station under N_2 atmosphere. Source, drain, and gate currents were monitored independently by two trigger-linked Keithley 6430 and one 2410 electrometers. In a plot of the square root of the drain current versus gate voltage, we fit the data in the saturation regime. According to the Equation 1, the average saturation mobility (μ) was calculated.

$$\sqrt{I_{ds}} = \sqrt{\frac{W\mu_{sat}C_{ox}}{2L}}(V_g - V_t) \quad (3)$$

Where, μ_{sat} is saturation mobility, C_{ox} is the capacitance of silicon oxide, and I_{ds}, V_g, and V_t are source-drain current, gate voltage, and threshold voltage, respectively. The mobility reported in this paper was the average from nine transistors as indicated above. The capacitance variation of oxide due to the different etching times was corrected for in this calculation.

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[39] Certain equipment, instruments or materials are identified in this paper in order to adequately specify the experimental details. Such identification does not imply recommendation by the National Institute of Standards and Technology nor does it imply the materials are necessarily the best available for the purpose.