$SiO_2/Si_3N_4/Al_2O_3$ stacks for scaled-down memory devices: Effects of interfaces and thermal annealing

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Effects of interfaces and thermal annealing on the electrical performance of the $SiO_2/Si_3N_4/Al_2O_3$ (ONA) stacks in nonvolatile memory devices were investigated. The results demonstrated the principal role of Si_3N_4/Al_2O_3 and Al_2O_3/metal-gate interfaces in controlling charge retention properties of memory cells. Memory devices that employ both electron and hole trappings were fabricated using a controlled oxidation of nitride surface prior to the Al_2O_3 growth, a high-temperature annealing of the ONA stack in the N_2+O_2 atmosphere, and a metal gate electrode having a high work function (Pt). These devices exhibited electrical performance superior to that of their existing $SiO_2/Si_3N_4/SiO_2$ analogs. © *2006 American Institute of Physics*.
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Silicon-oxide-nitride-oxide-silicon (SONOS) memory and its nitride read only memory (NROM) modification are attractive solutions for future high-density data storage applications.[1,2] In these devices the information is stored as charges in the silicon nitride layer. In contrast to traditional SONOS memories, where program/erase operations involve direct electron tunneling through a thin (~20 Å) bottom oxide (BOX), in NROM these operations are accomplished by hot carriers (electrons/holes) locally injected over a barrier of a relatively thick (40–70 Å) oxide into the nitride layer near the drain.[2,3] As a result, 2 bits of information can be reliably stored in a single memory transistor.

Scaling down the SONOS memory cell to sub-100-nm technology nodes necessitates ONO stacks with small effective oxide thicknesses (EOTs). Currently, the only viable solution for achieving a sub-100-Å EOTs involves replacement of a conventional SiO_2 in the top dielectric layer with a material having higher dielectric constant (k). The high-k top layer is expected to provide several additional advantages including effective blocking of electron injection from the gate electrode and improved program/erase efficiency with a possibility of a Fowler-Nordheim (FN) hole injection from the substrate. The FN hole injection could provide an erase mechanism alternative to the currently used "hot" holes, which are the principal cause of the BOX degradation in NROM cells.[3–5] Moreover, the FN hole injection could enable a refresh operation of the memory cell.[15]

Aluminum oxide, Al_2O_3, ($k=7–10$) (Ref. 6) is regarded as one of the best candidates for the top oxide layer in ONO stacks due to its high thermal and chemical stabilities, electrical strength, and compatibility with conventional materials used in the memory cell manufacturing.[7–10] Despite several promising results, a broad application of Al_2O_3 in the SONOS memory stacks is hindered by several technical problems, including inferior retention characteristics compared to traditional NROM devices,[8] pinning effects at the Al_2O_3/poly-Si interface,[9,11] and mechanical stresses in Al_2O_3 after the 900 °C annealing.[12]

The present letter reports a structural and electrical study of differently processed $SiO_2/Si_3N_4/Al_2O_3$ (ONA) stacks with a particular emphasis on the effects of (1) Si_3N_4 surface preparation, (2) postdeposition annealing of the entire ONA stack, and (3) type of metal top electrode on the electrical characteristics of the resulting ONA-based memory devices.

The ONA stacks used in this study incorporated a dry grown SiO_2 layer (68 Å) and a Si_3N_4 layer deposited by low-pressure chemical vapor deposition (CVD). The Al_2O_3 layer (150 Å) was grown on top of the Si_3N_4 layer using atomic layer CVD at $T=450$ °C. The Si_3N_4 surface was used either as deposited (A type) or intentionally oxidized (about 10 Å deep) prior to the growth of Al_2O_3 (B type).

The chemical structure of the alumina specimens was investigated by high-resolution transmission electron microscopy (HRTEM) and spatially resolved over the ONA thickness electron energy loss spectroscopy (EELS).[13]

Electrical characterization was performed using Si-ONA-metal (SONAM) capacitors with dimensions of 500×500 μm^2. Prior to capacitor fabrication, the samples were annealed at 850 °C for 30 min in three different gas environments (O_2, N_2, and a N_2+O_2 mixture).[14] Metal electrodes with large work function (Au and Pt) were used to increase the barrier height (~4 eV) for electron injection into Al_2O_3. The rear contact was fabricated using Al deposition.

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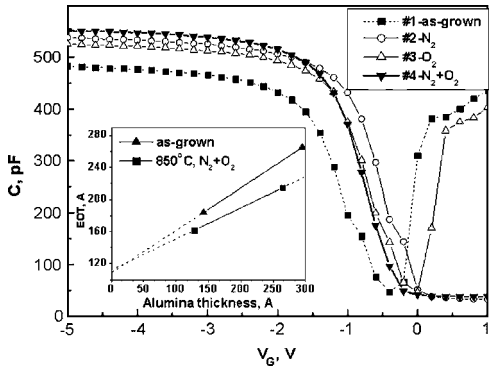

FIG. 1. *C-V* characteristics ($f=30$ Hz) of the *A*-type samples annealed in different gas environments. Similar effects were observed for the *B*-type stacks. An insert shows the EOT of the *B*-type stacks as a function of Al_2O_3 thickness (150 and 300 Å) in the samples as deposited and annealed at 850 °C in the N_2+O_2 mixture. The extrapolation to a zero thickness of Al_2O_3 yields the effective EOT of the ON bilayer. A small increase of the bilayer EOT after annealing is observed.

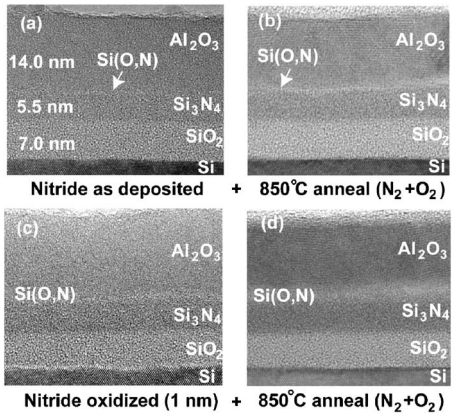

FIG. 3. HRTEM images of samples *A* [(a) and (b)] and *B* [(c) and (d)] before [(a) and (c)] and after [(b) and (d)] annealing at 850 °C in N_2+O_2. Crystallization of Al_2O_3 and the evolution of the SiON interfacial layer are observed.

Figure 1 shows the *C-V* characteristics of the *A*-type samples before and after annealing in different gas environments. The annealing significantly reduced both the EOT and the positive charge in the stack (compare curves 1 and 2–4). The positive charge in the as-grown stacks was attributed to the Si_3N layer[15] and correlates with the reduction of the hydrogen content in this layer upon annealing.[16] The heat treatment in the N_2+O_2 mixture yields the smallest EOT combined with a twofold reduction in the interfacial charges.

The *I-V* characteristics of similar samples before and after annealing are summarized in Fig. 2. The annealing decreased the FN current "threshold" voltage, which is consistent with the observed reduction of the EOT. The gas environment has a pronounced effect on the leakage (subthreshold) currents. We argue that oxygen annealing reduces the number of oxygen vacancies and improves alumina stoichiometry, thereby reducing the trap-assisted currents.

Cross-sectional HRTEM/EELS studies of the as-grown samples confirmed the amorphous nature of Al_2O_3 and revealed the presence of a partially oxidized nitride layer, hereafter denoted as SiON, at the Al_2O_3/Si_3N_4 interface even in the *A*-type sample (Fig. 3). These results are consistent with a partial oxidation of the nitride surface upon exposure to air reported previously.[16] The oxidized layer in the *A*-type stack is nonuniform with the average thickness of less than 1 nm. In contrast, controlled oxidation of the nitride surface in the *B*-type stacks generated a relatively uniform SiON layer of about 1 nm thick.

Annealing both *A*- and *B*-type stacks induced crystallization of Al_2O_3, regardless of the gas environment. Diffraction patterns and near-edge structure of the Al-$L_{2,3}$ and O-*K* EELS edges (Fig. 4) all suggest a γ-Al_2O_3-like polymorph as the crystalline phase.[17] A strong ⟨111⟩ texture was observed. The crystallization was accompanied by about 10% reduction in the thickness of Al_2O_3 layer, which is consistent with the 20% density increase commonly observed for the transformation from amorphous to γ-type Al_2O_3.[18]

In addition to crystallization of Al_2O_3, the annealing produced growth of the interfacial SiON layer. The resulting thickness of the SiON layer was about 2.5 nm in the *B*-type stack and about 1 nm in the *A*-type stack (annealing improved the uniformity of the SiON layer in the *A* type). The EELS suggested incorporation of Al into the SiON interfacial layer upon annealing, as evidenced by the characteristic change in the fine structure of the Al-$L_{2,3}$ edge on going from the crystalline Al_2O_3 to the amorphous interfacial (Si,Al)ON layer (Fig. 4). Furthermore, the secondary ion mass spectroscopy revealed that the amount of hydrogen in Al_2O_3 was reduced twice after the annealing. In parallel, the Al_2O_3 dielectric constant increases from $k\sim 7$ in the as-grown sample

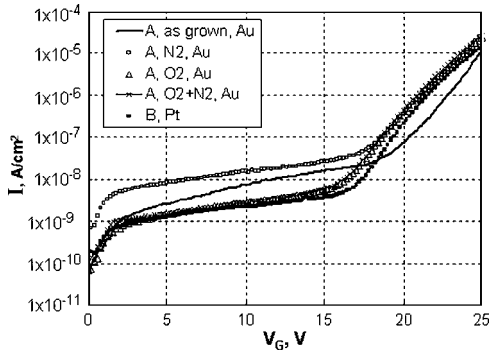

FIG. 2. *I-V* characteristics of *A*-type samples (Au electrode): as grown and annealed at 850 °C in N_2, O_2, and N_2+O_2 mixture. *I-V* curve for the *B*-type sample with the Pt electrode annealed at 850 °C in N_2+O_2 is shown for comparison (Pt electrode is advantageous for blocking of electron injection at high currents).

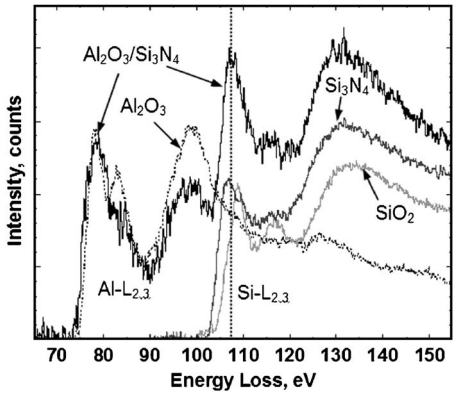

FIG. 4. Spatially resolved EELS spectra containing the Al-$L_{2,3}$ and Si-$L_{2,3}$ edges and recorded from the different layers in the *B*-type stack annealed at 850 °C in N_2+O_2. The spectra reveal clear changes in the near-edge structure of the Al-$L_{2,3}$ edge on going from γ-like Al_2O_3 to the amorphous interfacial layer. These changes are consistent with Al being present in the amorphous interfacial layer.

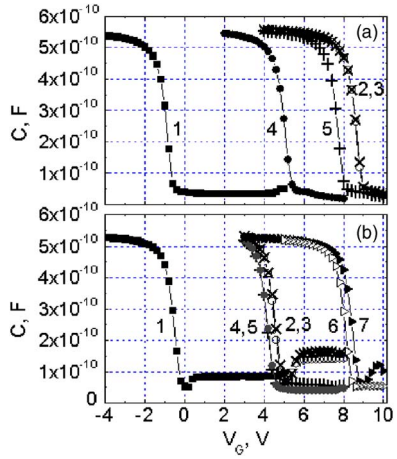

FIG. 5. (Color online) Charge loss effects observed in electron/hole-programmed capacitors (samples *A* and *B* annealed in N_2+O_2). (a) *C-V* curves for the *A*-type stacks with Au electrode: (1) initial; [(2) and (3)] *e* programmed (14 V) and biased positively and negatively, respectively, prior to the bake; and [(4) and (5)] biased positively and negatively, respectively, after bake. (b) *C-V* curves for the *A*- and *B*-type stacks with Pt electrode: (1) *A*-type initial; [(2) and (3)] *A*-type *e* programmed (14 V) and biased positively and negatively, respectively, prior to the bake; [(4) and (5)] *A*-type biased positively and negatively, respectively, after the bake; and [(6) and (7)] *B*-type *e* programmed (25 V) prior to and after the bake, respectively (program window ~9 V, ΔV_{fb}~300 mV).

to ~10 (insert of Fig. 1). Thus, the reduction of EOT (~10%) upon annealing can be attributed to crystallization of Al_2O_3. Extrapolation of the EOT dependence to the zero Al_2O_3 thickness (Fig. 1) indicates that the EOT of a bilayer ON stack increases upon annealing. It can be ascribed to the growth of a SiON layer (Fig. 3) having the *k* value lower than that of the nitride.

Figure 5 presents results of a charge loss in capacitors based on the *A*- and *B*-type ONA stacks. The charging was performed using a FN injection from the substrate. Subsequent baking at 150 °C for 1 h in the N_2 atmosphere caused a significant loss of the trapped carriers. No correlation between the retention loss and the leakage current was observed. The best retention characteristics were obtained after annealing in the N_2+O_2 mixture; however, the electron retention was still inferior to that of the standard NROM stacks (ΔV_{fb}~300 mV for program window ~3–3.5 V). The origin of the retention loss in the electron/hole-programed capacitors was determined by comparing standard baking and baking under a negative/positive voltage of 7 V applied to the gate. A complete suppression of charge loss when applying an appropriate voltage to the gate suggests that the loss occurs through the Al_2O_3 layer.

For the Al_2O_3-controlled electron loss, any charges present in the vicinity of the Al_2O_3/metal-gate interface should either enhance (positive charges) or suppress (negative charges) the electron flow. This effect was confirmed using the *C-V* test of the two capacitors. They were subjected to either positive or negative bias (5 V) which was applied to the gate electrode immediately prior to the bake. The electron loss in the capacitor having a positive charge at the Al_2O_3/Au interface was significantly higher than that in the capacitor with a negative charge [Fig. 5(a)]. A similar effect was observed for the hole-programed capacitors. The effect of the interfacial charges is more pronounced for larger program windows. The effect of a prebake bias polarity was much smaller for the Pt capacitors [Fig. 5(b)]. The hole-programed Pt-gated capacitors demonstrated the largest program window of 5.5 V, which is consistent with the best blocking of electron injection into alumina. Thus, the interfacial charge is not an intrinsic property of Al_2O_3 but is determined by the type of a metal electrode. Therefore, several other conventional materials having a high work function, such as TiN, TaN, and W, can be considered as potential candidates for a gate electrode.

Controlled oxidation of the nitride surface prior to Al_2O_3 growth (*B*-type samples) significantly reduced the level of electron loss in the SONAM stacks. The *B*-type ONA structures demonstrated retention characteristics that were either very close or superior to the conventional ONO. For example, the sample with a Pt electrode annealed in the N_2+O_2 mixture exhibited a retention loss of only 300 mV (for the 9 V program window) compared to 1 V in the *A*-type sample [see Figs. 5(a) and 5(b)]. This result suggests that a relatively thick (25 Å) interfacial (Si,Al)ON layer in the annealed B-type stack provides an efficient barrier for the electron escape into the metal electrode. We believe that the EOT of <100 Å can be achieved for ONA stacks by further reduction of all layer thicknesses, thus enabling operating voltages below 6 V in NROM- and 10–12 V in SONOS ONA-based memory devices.

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