Interconnection Continuity Test for Packaged Functional Modules

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We developed an electrical test to evaluate interconnections in packaged, electrostatic-discharge (ESD) protected modules. The ESD protection circuit, which in modern integrated circuits is present at every I/O as an inherent part of the chip structure, can be employed to create an electrical path through the interconnection without powering ON the internal circuitry of the chip. The technique utilizes a chip-specific voltage–current characteristic, and a model of the interconnection, from which the interconnection ohmic resistance can be directly obtained. The technique is applicable to a broad range of functional packages. Its sensitivity is comparable or better than the sensitivity of standard test techniques that utilize specialized test chips. This technique can also be used to test interconnections in failed IC's, since integrity of the internal circuitry is not required in this test.

INTRODUCTION

The testing of interconnection of chip carriers prior to chip assembly has become an increasingly difficult and expensive task. The small size of the chip joints and their complex top-surface metallurgy makes them susceptible to contamination and damage during handling and electrical probing. This has become a growing problem for the direct flip-chip packaging technologies that utilize microvias and organic carriers. To minimize the possibility of damaging the chip bonding pads, as can occur during continuity testing, this test has often been replaced with procedure that involves optical tracing of the nets at each circuitry level, followed by a single-node charge deposition or an open ended time-domain reflectometry. However, neither the optical tracing nor the single-node electrical probing can detect nets with defects such as insufficient thickness of the conductor, microcracking, or a buried contact resistance. Once the functional chip is assembled to the carrier the closed interconnection loop then contains nonlinear elements such as diodes, bipolar transistors, or FET transistors. These elements limit the applicability of direct input testing, making the test for most part impractical to perform. This paper describes a new electrical test that can be used to evaluate the interconnections continuity resistance in packaged modules by utilizing the electrostatic discharge protection circuit.

INTERCONECTION MODEL

In modern integrated circuits the ESD is built as an inherent p-n junction in the I/O cells, located in close proximity to the bonding pads (1). Figure 1 illustrates the diagram of a single interconnection which consists of the ball grid array contacts (BGA), carrier circuitry, the chip solder joints (C4s) and the ESD protection circuit. During normal operation of the integrated circuit, the ESD is reverse biased. When the ESD is forward biased its dynamic resistance drops and the junction channels electric charge away from the internal circuit. Thus, the ESD junction can be employed to create an electrical path through the interconnection without powering ON the internal circuitry of the chip.

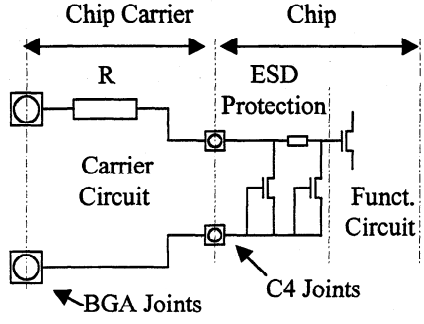

Fig. 1. Interconnection diagram.

The relationship between the current drained from the forward biased junction, I_j, and the resulting voltage at the testing pads, V_p, can be described by the following expression (1) (see ref. (2)).

$$I_j = I_o\left[\exp\left(\frac{q(V_p - I_j R)}{\eta kT}\right) - 1\right] \qquad (1)$$

where, k is the Boltzman's constant, η is the junction ideality factor, I_o is the saturation current, and R represents the equivalent resistance of the interconnection consisting of a junction resistance and the resistance of the wiring. Application of a current wave digitized as a set of n data points ΣI_j, results in the corresponding voltage wave ΣV_p. These experimental data can be used to obtain the interconnection ohmic resistance, the saturation current, and the ideality factor

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from equations (2-5). Equations (2-5) have been derived from expression (1) by using a general linear least squares method (3).

$$0 = \sum_{i=1}^{n} \frac{1}{\sigma_i^2} \left[\sum_{k=1}^{3} a_k X_k(I_{ji}) - V_{pi} \right] X_l \quad l = 1, 2, 3 \qquad (2)$$

where σ_i is the measurement error of the i^{th} data point, and the parameters a_1 ... a_3 and the basic functions $X_1(I_j)...X_3(I_j)$ of the model are given as follows:

$$a_1 = \eta kT/q \qquad X_1 = ln(I_j) \qquad (3)$$
$$a_2 = R \qquad X_2 = I_j \qquad (4)$$
$$a_3 = -\eta kT/q\ ln(Io) \qquad X_3 = 1 \qquad (5)$$

Substituting equations (3-5) into equation (2) yields a set of linear equations **XA** = **V** which can be solved directly. **A** is a vector of the interconnection parameters, **X** is a square matrix, which elements represent combination of the basic functions, and **V** is a vector that represents combination of the voltage wave with the basic functions.

EXPERIMENT AND RESULTS

Interconnection testing has been performed on a flip chip, plastic, ball-grid array package that carried a CMOS-6S chip. During testing, a forward biased current I_j, was drained by probing the BGA I/O pads. A Keithley[1] Model 2400 SourceMeter™ was used as a current source and a voltmeter. The instrument was programmed to perform a current sweep operation during which discrete current values were applied to the testing pads while the corresponding voltage drop was measured. The current values, the instrument delay time, and the number of readings taken at each current level were programmed individually for every I/O to minimize the testing time while maintaining measurement errors at a acceptably low level. Typically, the current wave and the resulting voltage wave consisted of 20 data points. A computer was used to control the SourceMeter™ and to carry out the data acquisition and calculation of the interconnection parameters.

Figure 2 shows the experimental current – voltage data for a single interconnection compared with the least squares fit to the model. The experimental data agree very well with the predicted values confirming the validity of the model and the calculation procedure. The equivalent continuity resistance of this interconnection obtained from the model is 4.845 Ω. This value corresponds well to the circuit resistance estimated from the geometrical details of the interconnection. The two remaining parameters i.e. substrate reverse current and the ideality factor, which are global for a given integrated circuit, are 7.1 nA and 1.78, respectively. The

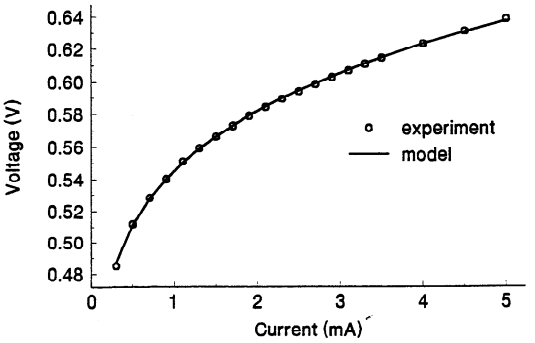

Fig. 2. The experimental and calculated current–voltage data for an interconnection path with ESD. R=4.845 Ω, η=1.78, Io=7.1 nA.

resolution of the resistance parameter, R, was determined experimentally to be about 5 mΩ by including a known standard, variable resistor in series with the interconnection.

There are several components, which contribute to the uncertainty of the estimated interconnection parameters R, η and Io. These include assumptions and simplifications of the model, computational as well as experimental errors. Experimental error includes error in making and maintaining reliable contacts as well as error introduced by variation of the junction temperature during the measurements. The interconnection model neglects contribution of the saturation current, Io, to the measured current. Since the saturation current is usually six orders of magnitude smaller than the measured current, this error was judged to be insignificant. Similarly, the computational errors were neglected since the number of significant figures in the computed solutions was >12. The number of significant figures in the computed solution was estimated by subtracting value of $\log(\|\mathbf{X}\|\ \|\mathbf{X}^{-1}\|)$ from the number of digits carried. From the instrument technical specification, the accuracy of voltage readings was better than 0.02 % with resolution of 50 μV, and the accuracy of the current readings was better than 0.05 % with resolution of 500 nA. Thus, the combined instrumental accuracy was expected to be in the range of about 0.07 %. However, the relative standard uncertainties of the interconnection parameters estimated as the diagonal elements of the covariance matrix were larger, in the range of 2.0 % for R, 1.5 % for η, and 1.7 % for Io. This corresponds to an error in R of about 100 mΩ. This error can be minimized further to about 80 mΩ by controlling and maintaining a constant temperature of the ESD junction.

1. Certain materials and equipment identified in his manuscript are solely for specifying the experimental procedures and do not imply endorsement by NIST or that they are necessary the best for these purposes.

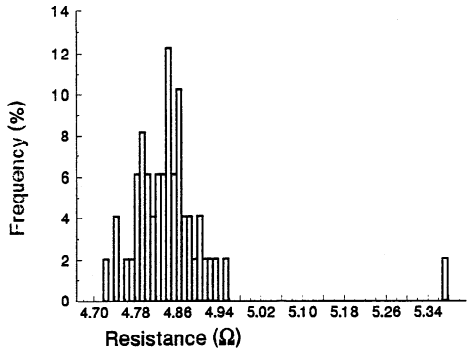

Fig.3. Histogram of the interconnection resistance.

Figure 3 shows a histogram of the interconnection resistance measurements for a batch of 36 modules. The distribution has a mean value of 4.836 Ω. The standard deviation of the distribution is 0.0514 Ω and the standard error of the mean is 8 mΩ. A measurement at 5.377 Ω falls outside of the distribution indicating an interconnection with questionable performance.

DISCUSSION AND CONCLUSION

It has been found experimentally that the test procedure described above can be used to determine the interconnection parameters, including the interconnection resistance, with considerable confidence and precision. For example, a current wave, digitized to 20 data points, is sufficient to determine the interconnection resistance, R, with resolution of 5 mΩ and relative standard uncertainty better than 2 %. A defective net will be distinctly separated from the entire population and easily detected on the histogram of the interconnection resistance. Likewise, statistical analysis of the other interconnection parameters, (the saturation current or the ideality factor) can be used to assess the quality and functionality of the chip. Unlike the results obtained by other techniques, which often produce unpredictable and unreliable results, the resistance values estimated with this method reflect the real continuity resistance of the interconnection circuit. This makes the method sensitive in the detection of defects caused by manufacture and environmental stressing. The computational algorithm is exceptionally stable and fast, while standard fitting procedures are usually computationally involved, subject to round off error affected by initial parameters, and often unable to meet the convergence criteria.

The testing time is a very important factor in assessing practical applicability of the test. A functional chip carrier having typically hundreds of input-output interconnections imposes rather demanding testing time requirements, which desirably, should not exceed a few tenths of a second per interconnection. In the presented laboratory set-up of the test, it takes about 200 ms to execute a suitable current wave for a single interconnection and to transfer the current-voltage data from the instrument buffer to the computing unit. In comparison, the computing time is negligible. The total testing time will also depend on the time it takes to make contacts to the test pads. Therefore, in a practical application, the testing time will most significantly depend on the speed of the hardware used and not on the model.

Although the above interconnection model emphasizes the electrical characteristic of the bipolar transistor, other types of the ESD protecting mechanisms, such as diode-connected FET transistors, can be employed and treated similarly. Thus, the presented test structure is of a general form, and therefore, is applicable to a broad range of functional packages. It can be used for process verification, non-destructive field failure analysis, and for interconnection reliability assessment with a comparable or better sensitivity than standard techniques that utilize specialized test chips. Even failed ICs can be tested using this technique since integrity of the internal circuitry is not required in this test.

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