A paradigm for interconnect geometry to reduce grain boundary resistance

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Interconnects with nonuniform width are proposed for control of grain boundary density; the grain boundaries will be driven toward the narrowest locations to reduce the free energy of the system. The positive impact on electrical transport of the reduced grain boundary density is weighed against the negative impact of local constrictions and reduced line packing, with practical geometrical parameters quantified through consideration of sidewall roughness. It is found that technologically relevant sub-100-nm interconnects could benefit from use of this line geometry.
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INTRODUCTION

Shrinkage of transistor dimensions on silicon computer chips has been accompanied by a similar reduction of the dimensions of the metal interconnects that join them. As copper interconnect widths have shrunk below 100 nm, their electrical resistivity has risen due to scattering of electrons on the interconnect surfaces as well as the boundaries between the discrete copper grains that comprise the interconnects.[1–3] This size effect increases *RC* time delays as well as Joule heating and is noted to be a key issue in manufacturability of future electronics.[4] The magnitude of the problem has motivated substantial research into the processing and properties of metallizations fabricated from alternative conductors such as silver.[5–13] However, experimental data indicate that the increased resistivity is due as much to electron scattering on the grain boundaries within the interconnects as to scattering on the interconnect surface,[1–3] and similar results have been obtained for silver interconnects.[13] It therefore appears that mitigation of size effects requires control of microstructure.

DIAMONDBACK GEOMETRY: BENEFIT AND COST

Grain boundary scattering in wires is modeled assuming a "bamboo" structure for the grain boundaries, i.e., all grain boundaries perpendicular to the wire axis. Reflection of a fraction of the electrons passing over the grain boundaries that span the conductor path is the origin of the increased electrical resistivity. A formula for the effective resistivity of a wire with regularly spaced grain boundaries has been published,[14]

$$\rho_{\mathrm{gb}} = \left[1 - \frac{3}{2}\xi + 3\xi^2 - 3\xi^3 \ln\left(1 + \frac{1}{\xi}\right)\right]^{-1} \rho, \tag{1}$$

where ρ is the intrinsic resistivity of the bulk conductor and ξ depends on the grain size (grain boundary spacing) δ, boundary reflectivity coefficient R, and electron mean free path in the bulk conductor λ according to

$$\xi = \frac{\lambda}{\delta}\frac{R}{1-R}. \tag{2}$$

The predicted grain boundary scattering increases as the grain boundary spacing decreases below the mean free path of the electrons λ (36 and 57 nm for high-purity copper and silver, respectively, at room temperature). Increasing the grain size of ultrasmall interconnects decreases the resistivity of the interconnect by decreasing the number of grain boundaries scattering electrons along a given length. Based on the results for Cu and Ag interconnects, entirely eliminating the grain boundaries would decrease by more than a factor of 2 the resistivity increase associated with reduction of interconnect size. However, processing of copper[1,2] (and silver[13]) interconnects results in a grain size similar to the smallest dimension of the interconnect (width or height). There are no known techniques to increase the grain size significantly.

Currently, recrystallization dynamics coupled with trench geometry limit the grain size in interconnects with uniform cross section. This paper suggests that the interconnect geometry therefore needs to be reconsidered; a geometry that would allow the grain boundary spacing to be controlled would be of some interest. Such a geometry is shown schematically in Fig. 1 where the interconnect has a modulated, rather than a uniform, width. In this case, the modulation resembles the pattern on the back of a diamondback rattlesnake. Such modulation of the interconnect width creates a driving force for attracting and pinning the grain boundaries at particular locations; reduction of the free energy of the system by minimization of grain boundary area

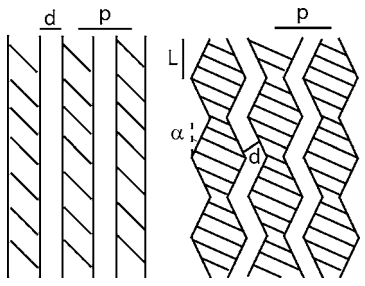

FIG. 1. Schematic arrays of straight and diamondback geometry interconnects, the latter configured for optimal packing with identical pitch and gap (plan view orientation, interconnect height *h* not indicated).

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drives grain boundaries toward the narrowest locations on the interconnect. These locations are defined by the lithography used to fabricate the damascene trench that will contain the interconnect; for the diamondback geometry in Fig. 1 they are spaced $2L$ apart. For any nonzero value of the splay angle α, the grain boundaries can reduce their area by moving to these internal corners of the modulation; the driving force for this motion increases with the angle α. In what follows it will be assumed that the diamondback geometry works perfectly so that grain boundary spacing equals $2L$. Conditions that might impede successful implementation are then explored, specifically the impact of sidewall roughness.

The paper calculates two resistance effects: (1) decreased resistance due to increased grain boundary spacing but unchanged interconnect width and (2) increased resistance due to varying interconnect width but unchanged grain boundary spacing. The terms are added together to estimate the total impact of the geometry change.

An estimate of the change of the interconnect resistance Δ_{gb} due to changed grain boundary spacing is obtained from the difference between ρ_{gb} in Eq. (1) evaluated using grain boundary spacing defined by the diamondback geometry ($\delta=2L$) and, as with traditional interconnects, by the interconnect width ($\delta=w\equiv p-d$),

$$\Delta_{gb} \approx \left.\frac{L}{wh}\rho_{gb}\right|_{\delta=w}^{\delta=2L} = \frac{L}{wh}\rho\left[1-\frac{3}{2}\xi+3\xi^2-3\xi^3\times\ln\left(1+\frac{1}{\xi}\right)\right]^{-1}\Bigg|_{\xi=(\lambda/w)R/(1-R)}^{\xi=[\lambda/(2L)]R/(1-R)}. \tag{3}$$

Use of the single width w to convert from resistivity to resistance for both geometries implicitly treats the grain boundary scattering as a fixed resistance localized at the interface, hence the noted approximation. Resistivity decreases, $\Delta_{gb}<0$, if the grain boundary spacing increases, here for $L>w/2$.

The diamondback geometry increases the resistance by introduction of constrictions along the length of the interconnect as well as through decreased packing efficiency for arrays of lines. In deriving expressions for these effects, it is presumed that interconnect resistance is proportional to the inverse of interconnect width integrated along the length of the interconnect. Integration over scattering paths,[13,15,16] while appropriate for the length scales of interest, is not practical for reasons that will be discussed later; also, the predictions of such models would depend on the specularity assumed for the surface.

Consider an optimized packing for an array of lines, such as is shown in Fig. 1, where the modulation along adjacent lines is displaced by L, one-half of the modulation wavelength. For comparison to interconnects of uniform width where $w=p-d$, demanding equivalent line pitch p and spacing d between the interconnect surfaces (i.e., along a path normal to the interconnect surface) leads to a value for the diamondback interconnect's average width $\bar{w}$ that is decreased below the value w according to

$$\bar{w} = w - d\left(\frac{1}{\cos(\alpha)}-1\right). \tag{4}$$

This reduced linewidth results from the additional area associated with the meander of the gap region between the conductors. The resistance of the diamondback line without grain boundaries (called here the "intrinsic" line resistance R_{int}) is obtained by integrating the resistance per length (resistivity divided by cross-sectional area) along one segment,

$$\begin{aligned} R_{int} &= \int_0^L \frac{\rho}{hw(x)}dx \\ &= \frac{\rho}{h}\int_0^L \frac{dx}{w_{min}+2x\tan(\alpha)} \\ &= \frac{\rho}{2h\tan(\alpha)}[\ln(w_{min}+2L\tan(\alpha))-\ln(w_{min})]. \end{aligned} \tag{5}$$

Then, noting that the average width of the diamondback line is related to the minimum width and splay angle α by $w_{min}=\bar{w}-L\tan(\alpha)$ and using the relationship between w and $\bar{w}$ for diamondback and straight interconnects with equal pitch and gap given in Eq. (4), Eq. (5) can be rewritten as

$$R_{int} = \frac{\rho}{2h\tan(\alpha)}\ln\left(\frac{w-d([1/\cos(\alpha)]-1)+L\tan(\alpha)}{w-d([1/\cos(\alpha)]-1)-L\tan(\alpha)}\right). \tag{6}$$

The numerator and denominator of the logarithm are the maximum and minimum widths of the diamondback interconnect. Using the resistance of the straight interconnect without grain boundaries,

$$R_0 = \frac{\rho L}{hw}, \tag{7}$$

and Eq. (6), the resistance change associated with using diamondback interconnects in place of straight interconnects of equivalent pitch and spacing (both without grain boundaries) can be written as

$$\begin{aligned} \Delta_{int} &\equiv R_{int}-R_0 \\ &= \frac{\rho}{2h\tan(\alpha)}\ln\left(\frac{w-d([1/\cos(\alpha)]-1)+L\tan(\alpha)}{w-d([1/\cos(\alpha)]-1)-L\tan(\alpha)}\right) \\ &\quad -\frac{\rho L}{hw}. \end{aligned} \tag{8}$$

Adding the changes of the grain boundary and the intrinsic resistances to obtain the net resistance change arising from use of the diamondback geometry over straight interconnects, scaled by the resistance of the straight interconnect without grain boundaries, yields

$$\frac{R_{diamondback}-R_0}{R_0} = \frac{\Delta_{int}+\Delta_{gb}}{R_0}. \tag{9}$$

This change is plotted as a function of the lithographically defined diamondback half-period L in Fig. 2 using the expressions for Δ_{gb} and Δ_{int} given in Eqs. (3) and (8), respectively. Parameters for these predictions are grain boundary reflectivity $R=0.3$, mean free path $\lambda=36$ nm, interconnect

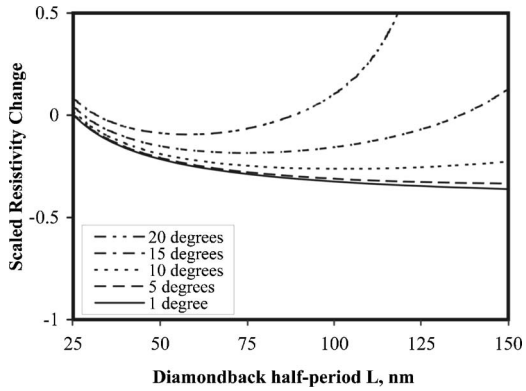

FIG. 2. Scaled resistance change as a function of the diamondback half-period L for $R=0.3$, $\lambda=36$ nm, $w=50$ nm, and $d=50$ nm. Splay angles α are indicated.

width $w=50$ nm, and gap $d=50$ nm (pitch $p=100$ nm). Results are shown for several values of splay angle α. Negative values indicate lower resistance than the straight interconnect with equivalent pitch and spacing. This difference exceeds $0.25R_0$ for $\alpha=10°$; the diamondback geometry thus eliminates more than two-thirds of the $0.44R_0$ resistance increase associated with grain boundary scattering in the straight interconnect. The improvement is larger if α is smaller; however, as will be discussed, line edge roughness precludes the use of arbitrarily small values of splay angle.

Figure 3 shows predictions for $w=30$ nm and $d=30$ nm ($p=60$ nm). The benefit of the diamondback geometry for this case reaches $0.48R_0$ for $\alpha=10°$, this is two-thirds of the grain boundary-induced resistance increase of $0.72R_0$ in the straight interconnect. For an intrinsic resistivity of 1.8 $\mu\Omega$ cm, similar to that of copper, this corresponds to a 0.86 $\mu\Omega$ cm decrease of the effective resisitivity of the diamondback interconnect as compared to that of the straight interconnect. Curves that terminate do so because their minimum width [$w_{\min}$ of Eq. (5)] reaches zero at that value of L.

The decrease of interconnect resistance that accompanies use of the diamondback geometry is greater for smaller splay angles. This is because the restrictions and packing loss associated with the diamondback are reduced so that the full benefit of the increased grain boundary spacing is realized. The diamondback geometry also yields improved resistance

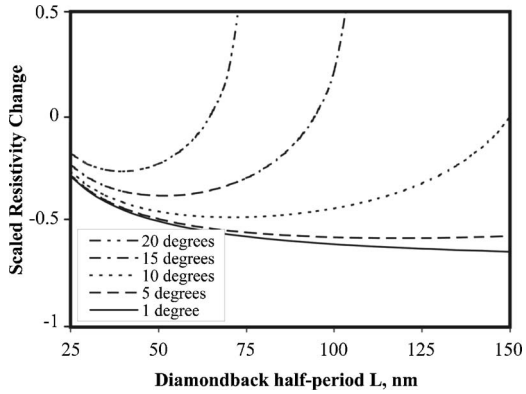

FIG. 3. Scaled resistance change as a function of the diamondback half-period L for $R=0.3$, $\lambda=36$ nm, $w=30$ nm, and $d=30$ nm. Splay angles α are indicated.

as L increases, but only to a point; as L increases sufficiently beyond the mean free path, the benefit saturates while the detrimental aspects of the splay begin to increase the resistance of the interconnect. The value of L at which optimum behavior is obtained depends on the splay angle.

THE IMPACT OF SIDEWALL ROUGHNESS

Successful implementation of the diamondback geometry for reduction of grain boundary density requires motion of the grain boundaries toward the narrowest regions of the interconnect so that multiple grain boundaries can be replaced by only one. The motion is driven by reduction of grain boundary area and energy through the monotonic decrease of the interconnect width; sufficiently large sidewall roughness could create local minima in the linewidth that would impede the requisite grain boundary migration. As an example, consider a sinusoidal variation of amplitude η and wave number ω on the interconnect width (assumed invariant through the height of the interconnect). In this case the width of a given segment can be written as a function of position x (defined along the centerline),

$$w_{\text{rough}}(x) = |x|\tan(\alpha) + \eta \sin(\omega x), \tag{10}$$

where the constant term has not been written. Taking $dw_{\text{rough}}/dx=0$ to find the positions x^* of local energy minima yields

$$x^* = \frac{1}{\omega}\cos^{-1}\left(\frac{\tan(\alpha)}{\eta\omega}\right), \tag{11}$$

which has no solution, and thus no local minima, for $|\tan(\alpha)| \geqslant \eta\omega$. For linewidth variation with a wave number $\omega=0.126$ nm^{-1},[17] this result indicates that η greater than 1.4 nm will lead to trapping for a 10° splay angle. The ITRS roadmap already calls for lithography with 3σ dimensional control of 1.8 nm before the end of this decade and 1.0 nm by the middle of the next.[18]

DISCUSSION

The effectiveness of the diamondback geometry for controlling the grain boundary density in real materials and structures will depend on the kinetics of grain boundary motion as well as pinning of such motion as might occur on the sidewalls, the energetics of which have been explored above. Significantly, grain boundary migration over micrometer lengths is typical in the field over filled features during the recrystallization that accompanies postdeposition processing of Cu interconnects.[19] Given sufficient impetus through the sidewall splay, it should be possible to direct this motion within the features. Interestingly, sharp cusps on straight lines have been used to trap magnetic domain walls; in that case, however, applied magnetic field drives the domain wall to the pinning site.[20]

Surface scattering might also be impacted by the varying width. An exact integral expression like that for straight interconnects[13,15,16] cannot be derived because the bounding surfaces cannot be written using a finite number of functions. Numerical and approximate analytical solutions have not been attempted. Capacitance, approximately scaling with in-

terconnect perimeter as $1/\cos(\alpha)$, will be lowest for the smallest splay angle compatible with the requisite grain boundary motion. Interestingly, similar modulation of the interconnect height would yield a driving force for directed grain boundary migration without the packing problems inherent in width modulation at fixed pitch.

CONCLUSIONS

In summary, the positive impact on electrical transport of reduced grain boundary density that might arise from the use of an interconnect geometry of nonuniform width was weighed against the negative impact of local constrictions and reduced line packing associated with the same geometry. It was found that the electrical resistance of technologically relevant sub-100-nm interconnects could be reduced through the proposed modulated line geometry. The parameters used to evaluate the impact of the modified geometry, though not particularly aggressive, eliminated approximately two-thirds of the detrimental grain boundary contribution to the interconnect resistance (within the approximations used for the analysis). The same geometrical parameters yielded energetics favorable for directed grain boundary migration even when existing expectations for the sidewall roughness of future interconnects were considered; kinetics are not generally believed to be a limiting factor. The success of analogous experiments with magnetic domain walls is highly suggestive.

ACKNOWLEDGMENT

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