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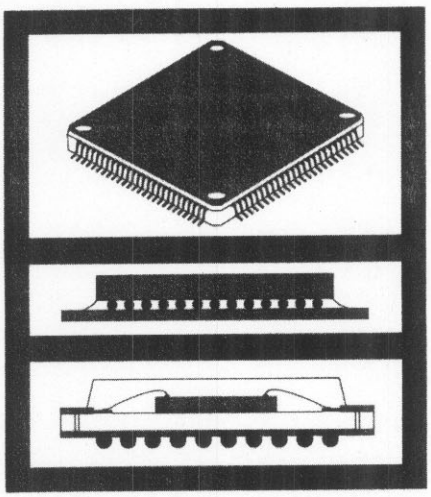

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PLASTIC FLIP-CHIP-BGA CARRIER WITH MICROVIAS FOR CHIP SCALE PACKAGING

Jan Obrzut, Polymers Division, NIST, Gaithersburg, MD 20899
Miguel Jimarez, IBM Microelectronics, Endicott, NY 13760

We evaluated a near-chip-scale package, that utilizes the flip-chip, plastic-ball-grid-array technology with microvias. The microvias were photolithographically patterned in built-up dielectric layers. We verified optimal conditions for photo-exposure and thermal cure process of the SLC, phtoimageable dielectric layer, using dielectric relaxation spectroscopy measurements. The resulting composite material exhibited aging resistance and satisfactory dielectric properties. We also investigated several fiber-glass-epoxy laminates using dielectric spectroscopy, and identified a laminate material of low moisture absorption and exceptional immunity to the plated-fiber-defects. The phtoimageable dielectric layer and the fiber-glass-epoxy laminates were selected to build the near-Chip Scale Package. The package was successfully fabricated using the flip-chip, plastic-ball-grid-array-microvia technology. The 4S2P structure with 256 BGA connections accommodated a chip with 700 C4 joints. Measurements of stress concentration and thermal expansiveness during thermal loading indicated that the mechanical construction of the package was optimally designed. The predictions of the materials dielectric evaluation and of mechanical modeling were verified by executing a series of standard reliability tests. It has been determined that this plastic, Flip-Chip-BGA carrier with microvias is manufacturable and can satisfy the standard reliability requirements.

Keywords: plastic chip carrier, chip scale packaging, microvias, photoimageable dielectric, interfacial moisture, flip chip, ball grid array, reliability, stress testing

INTRODUCTION

Chip Scale Packages (CSPs) take advantage of massive connectivity and improved electrical performance of the flip-chip packaging technology. These improvements result from the application of an additional dielectric layer between the chip and the carrier. The presence of microvias and built-up circuitry such as the Surface Laminar Circuitry (SLC)[1] in this additional layer, allows the utilization of chip-scale ground rules to packages that were traditionally considered as printed wiring board designs. Currently available CSP applications consist of about 50-150 I/O's, with pitches in the range of 500 to 1270 μm. In this article we evaluate a Flip-Chip Plastic Ball-Grid-Array package (FC/PBGA) that carried a 12 x 14 mm die with 700 controlled collapse chip connections (C4). The tightest pitch between the C4 joints was 230 μm. The carrier dimensions were standard 21 mm x 21 mm, 1.27mm pitch, with 255 BGA interconnections. According to the technical benchmark of the chip scale packages [2], a package can be defined as a CSP if either the package-die perimeter ratio is smaller than 1.2, or the package-die area ratio is smaller than 1.5. The perimeter and area ratios of our package were 1.4 and 2.6 respectively. Thus, our package did not exactly meet the CSP definitions. Nevertheless, we consider it capable of further scaling and the results obtained here can serve as an important step in the development of the CSP technology and the corresponding scaling rules. In the following sections we will discuss the characterization of the dielectric layers, the package construction and assembly process, the results of bumping of the FC pattern, the out of plane expansiveness measurements, and the reliability assessment of the package.

EXPERIMENTAL

Dielectric Materials

The negatively acting, photoimageable dielectric material for microvias (Surface Laminar Circuit, SLC™) was based on a formulation obtained by swelling an epoxy resin with a second epoxy monomer. These were mixed with photoinitiator and cross-linking activation constituents. During photo patterning, the material was selectively cross-linked by photo-initiated polycondensation of the epoxy monomer. After the development of the microvias, the dielectric was finally cured using a thermal bake. The effect of accelerated environmental stress on the dielectric properties of the SLC layer was evaluated by dielectric relaxation spectroscopy [3]. A Similar dielectric technique was employed to characterize interfacial moisture in an epoxy resin-fiber glass laminate, which was used as a core for the chip carrier construction [4].

Substrate Construction and Assembly

The cross-section of the chip carrier consisted of four signal and two power planes, (4S2P), arranged in the following order:
(S2){SLC}(S1){laminate}(P){laminate}(P){laminate}(S1') {SLC}(S2'). The 2S2P portion of the laminate i.e. (S1){laminate}(P){laminate}(P){laminate}(S1') was produced using standard sequential drilling and full-panel-copper-plate processes. The plated through-holes (PTHs), with a diameter of 250 μm, were completely filled with a CTE-matching copper-particles-epoxy-resin paste. The filling process was designed and implemented specifically for this construction in order to increase the surface area over the filled PTHs available for the SLC layer. The panels with filled PTHs were planarized, and were again full-

panel-copper-plated. The two S1/S1' signal circuitry layers consisted of 75 μm wide lines and 125 μm spacing. They were made by a subtractive etch process. After surface preparation, the photoimegeable dielectric material was applied, exposed, developed and cured to form the outer, nominally 50 μm thick SLC layers. This unique design allowed direct landing of microvias onto filled, plated-through-holes without the necessity of implementing the dog-bone connections. Consequently, this enabled a very high density of flip chip interconnections on a single SLC layer. The nominal diameter of the developed microvias in the SLC layer before plating was about 100 μm. The S2/S2' circuitry on the SLC layer was made using an additive copper plating process to form 50 μm wide lines, spaced by 122 μm. After circuitizing the SLC layer, a solder mask was applied and the parts went through the finishing metal preparation process. The C4 pads and the BGA pads were either electroplated with an eutectic Sn/Pb, or finished by electroless-nickel deposition and subsequent immersion gold plating. The finished, electroless Ni-Au C4 pads and microvias were bumped by screen printing of an experimental, water soluble solder paste and a laser cut stencil. In contrast to the Sn/Pb plating, the screen printing resulted in a better yield and a much higher quality of C4 joints.

The chips were attached to the carriers on an assembly line using mechanical placement and no-clean flux. After the reflow, the volume of solder joints and their electrical continuity were inspected. The assemblies were encapsulated with an underfill and inspected for voids and adhesion defects by using acoustic microscopy. The eutectic BGA balls (750 μm in diameter) were attached to the BGA pads using a graphite mold.

Table 1. Test nets, their attributes and the number of the risk sites in the net per module

Attributes	Number of the risk sites per module
C4-S2	290
C4-μVia-S1	158
S1-FPTH-S1'	45
S2-μVia-FPTH-S2'-BGA	43
S1'-μVia-BGA	80
S2'-BGA	120
C4-μVia-FPTH-μVia-BGA-(card)	26
S2-(X-Y) nets	4
S1-(X-Y) nets	4
S2-S1(Z) nets	8
FPTH-Power Planes	42
Voltage-Ground (Z) net	1

C4 chip-carrier joints
μVia microvias in the SLC dielectric
S2 signal layer at chip-SLC interface
S1 signal layer at SLC-laminate interface
FPTH filled, plated through holes in the laminate

Thermo-Mechanical Characterization

The relative mechanical compliance and thermal mismatch between the silicon chip, the underfill material, and the laminate carrier were analyzed using both Shadow Moiré and Moiré interferometry techniques [5, 6]. The bending deformation was also studied by measuring the deflection of the module at various temperatures.

Reliability Testing

The circuitry of the chip, the carrier, and the card for 2nd level assembly were carefully designed for ease of monitoring during environmental stress testing. Specifically, we were concerned with the electrical continuity of the interconnections and the electro-migration along the interfaces and across the dielectrics. The attributes of the test nets and the number of the risk sites per module are listed in table 1.

Description of the Risk Sites

C4-S2; The C4 joints of the chip were attached directly to the SLC circuitry. The nets were arranged as daisy-chain-stitches between the chip and the carrier. Fatigue life of the C4-to-S2 connections was determined based on electrical continuity measurements during accelerated temperature cycling. In order to detect electro-migration within the underfill and at the chip-S2 interface, adjacent nets were biased against the C4-S2-μVia-S1 nets while being exposed to heat and humidity.

C4-μVia-S1; The chip C4s were connected to the S1 circuitry through microvias. The risk sites were combined into daisy chains stitches to test integrity of the microvias, and of the C4-to- microvia and microvia-to S1 connections.

FPTH-S1; This net was designed to test the robustness of the filled-plated-through-holes. The net consisted of a single stitch arranged around the entire laminate, outside the chip perimeter.

FPTH-μVia-BGA; This net has been designed to test the fatigue life of the interconnections of microvia joined to the filled-plated-through-hole on the BGA side of the carrier. The continuity-resistance of the nets was monitored during the accelerated thermal cycling.

S1'-μVia-BGA; The S1' circuitry of the laminate was connected to microvias and BGA joints. After 2nd assembly the carrier BGAs were connected to a complementary stitch pattern on the card. Therefore, this net was used to evaluate the 2nd level assembly interconnections.

S2'-BGA; These nets consisted of BGA joints attached directly to the bottom-most S2', SLC circuitry. The BGA joints could be connected to the complementary, daisy chain stitches on the surface circuitry of the card. The S2'-BGA nets were used to determine fatigue life of the BGA to SLC and the BGA to card interconnections. In addition these nets were utilized to investigate electromigration at the S2"-BGA interface and at the BGA-card circuitry interface by biasing the adjacent nets against each other.

C4-MV-FPTH-MV-BGA-Card; This was the most complex interconnection that exhibited all the novel attributes of the entire structure, including the connections within the near chip scale size FC/PBGA package and the BGA connection of the package to the card. The crossection of the risk site is shown in figure 9.

S2-(XY) and S1 (XY) nets consisted of comb patterns outside the chip area that matched the ground-rules of the S2 and S1 circuitry. They were used to evaluate in-plane electromigration between adjacent signal lines at the solder mask-SLC interface and at the SLC-laminate interface respectively.

S2-S1(Z); These were the same (XY) nets, but biased in the Z-direction, across the SLC layer to determine the dielectric integrity of the SLC material.

FPTH-Power Planes; The FPTHs were connected together and biased against the two power planes inside the laminate. Each FPTH-Clearance-Hole interface represented a risk site designed to characterize the carrier immunity against formation of anodic filaments along the glass-fiber surface.

Voltage-Ground (Z) net was used to evaluate the dielectric integrity of the carrier laminate material.

Table 2 summarizes the reliability and sample quantities used in each test.

Table 2. Reliability Test matrix.

No	Test	Conditions	Duration	Sample size	Ref.
1	ATC	-55 +125 °C	5000 c.	29 mod. 1)	[7,15]
2	ATC	-25 +115 °C	5000 c.	25 mod. 2)	[8,15]
3	ATC	-55 +125 °C	2350 c.	43 mod. 3)	[7,15]
4	ATC	0 to +125 °C	4000 c.	25 mod. 4)	[9]
5	PwC	25 to +110 °C	13400 c.	10 mod. 4)	[10]
6	PwC	25 to +125 °C	13400 c.	9 mod. 4)	[10]
7	HAST	110 °C 85 % RH 5.5 V	200 hrs.	10 mod. 4)	[11]
8	THB	85°C 85 %RH 5.5 V	1077 hrs	20 mod. 4)	[12]
9	PCT	121 °C 100 % RH	96 hrs	14 mod. 1)	[13,15]
10	HTS	150 °C	1240 hrs.	10 mod. 1)	[14]

[1] Modules tested as a component in a socket

[2] Modules assembled to cards, simulated rework performed on 5 modules.

[3] Modules tested as a component in a socket, simulated rework performed on 5 modules.

[4] Modules assembled to cards.

Hardware subjected to tests 1-3 and 9 was preconditioned according to test method [15] for class 3 and 2 moisture sensitivity.

RESULTS and DISCUSSION

Dielectric evaluation of the SLC and the laminate materials.

The dielectric properties of the SLC layer and the fiber-glass reinforced laminate were studied in detail in order to gain a fundamental understanding of the aging processes related to the manufacturing conditions and to the environmental stresses. Fig. 1 shows dielectric loss tangent of the SLC layer as a function of temperature, first, after UV exposure, and second, following complete photo / thermal cure. The low-temperature relaxation in the glassy state (β-relaxation) is associated with the local motion of the side-groups and limited motion within the backbone. The

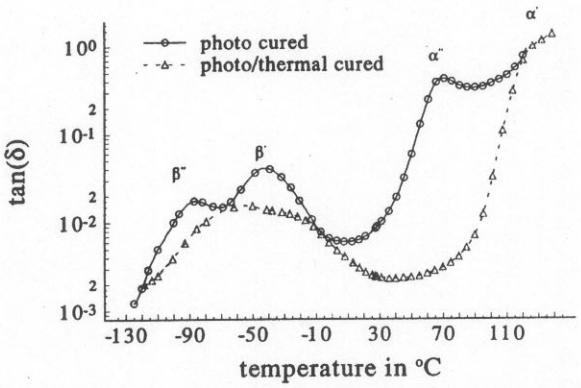


Fig. 1. Dielectric loss tangent of the SLC material as a function of temperature at 100 Hz.

high-temperature, glass-rubber relaxation (α-relaxation), resulted from a large-scale conformational rearrangement of the polymer backbone. The multiple relaxations seen in the photo-cured material (Fig. 1a) indicate that some incompatibility existed between components of the photo-cured polyblend. This resulted in phase separation with phase dimensions on the order of 0.1 μm. After thermal baking, the extent of molecular mixing in the final composite material appears to be considerably higher. The dielectric spectrum of the composite obtained from the photo and thermal crosslinking process shows that the two transitions broadened and merged into a single, broad relaxation peak. This indicates that there was substantial interpenetration between components of the polymer networks. Moreover, it shows that the curing process has been sufficiently optimized to produce a composite material with desirable dielectric properties. Heat and moisture treatment, however, reduced interpenetration. Figure 2 shows that the broad, single loss peak of the composite splits into subcomponents in HAST. It is seen that the phase

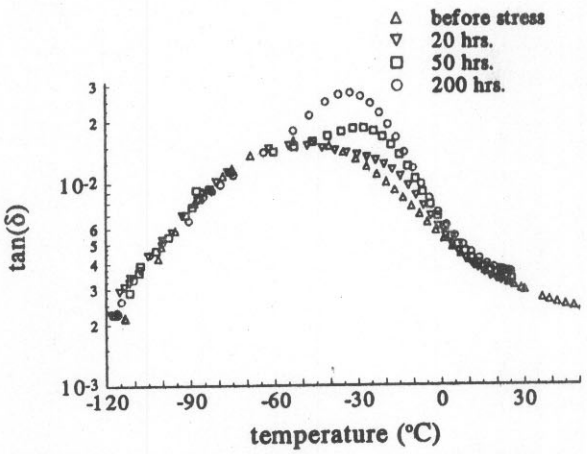


Fig.2. Effect of environmental stress (110°C, 85 % RH) on dielectric relaxation of the SLC material.

separation advances with duration of the stress. During environmental stressing at temperatures below the lowest glass-rubber transition temperature (T_G = 115 °C), the components of the polymer-network remain intimately mixed (Figure 2) and the failure rate decreases in time. On the other hand, environmental stressing at temperatures above the lowest glass-rubber transition reduced interpenetration considerably, and accelerated the failure rate due to moisture accumulation at the interphase. Such accumulation of moisture can create water paths, which may lead to a drop of insulation resistance below the failure criteria (1 MΩ). Based on these results, we decided to perform the HAST test at 110 °C for 200 hours. This was in contrast to common industrial practice which perscribes testing at 130 °C for 50 hours.

In contrast to the SLC dielectric layer, loss of insulation resistance in fiber-glass epoxy-resin laminates during environmental stressing can primarily be attributed to the

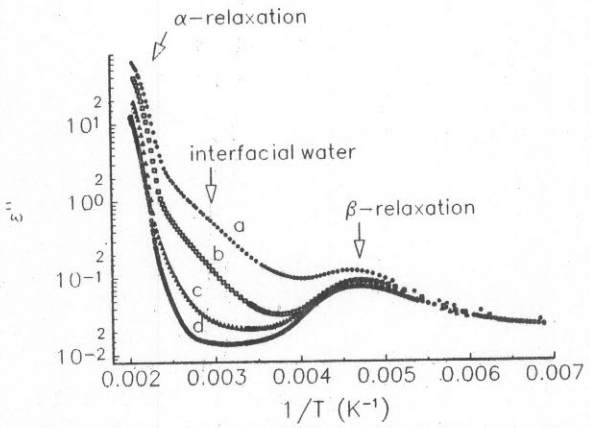


Fig.3. Dielectric loss of fiber-glass epoxy-resin laminates as a function of 1/T at 100 Hz after HAST (130 °C, 85% RH, 100 hours). Moisture concentration: (a) 1.2 %, (b) 0.8 %, c 03 % and (d) is a dry reference

creation of conducting filaments of copper along the glass fiber [16]. Metallic electro-migration along the glass fiber epoxy-resin interface can take place in the presence of interfacial water, which facilitates transport of interfacial charge carriers. The dielectric spectra of several fiber-glass-epoxy-resin laminates considered for this FC-PBGA carrier are shown in figure 3. All laminates are based on the same epoxy resin, but reinforced with three glass-fabric finishes. Each finish contains the same amino-functional-silane-vinyl-benzyl coupling agent. Only the glass surface is treated to enhance cleanness and improve the silane coverage. By ranking the finish from (a) to (c), we qualitatively described increasing cleanness of the glass surface for the silane application. Moisture that accumulated as interfacial water at the phase boundary between the glass and the resin gives rise to an additional peak on the dielectric relaxation spectrum. This interfacial water peak is located in Fig. 3 between the α and β relaxations. The area of this peak increases proportionally with the content of the absorbed water, and corresponds to the relaxation strength due to water. Thus, it is seen that the amount of interfacial water that accumulated during 100 hours of stressing at 130 °C, 85% RH was largest for laminate (a) (1.2 %), which received the standard finish. The amount of water that intruded the interphase in laminates (b) and (c) with enhanced finishes was considerably smaller, in the range of 0.8 % and 0.3 % respectively. It is worthy to note that the character and position of the α and the β peaks remains essentially unchanged after the HAST, indicating that moisture did not penetrate the backbone of the resin.

The data shown in Fig. 3 provide clear evidence that this resin remained dry during the environmental stress and that moisture collected mostly at the glass-resin interface. Moreover, the concentration of the interfacial water depended mostly on the bond-strength between the glass surface and the coupler, as long as the bonding between the coupler and the resin was optimally strong. In finish (c) the fabric received a special cleaning treatment to enhance condensation of silanol groups with silicates of the glass. Consequently, after 100 hours of HAST at 130 °C, 85% RH, laminate (c) absorbed only 0.3% of moisture and exhibited substantially improved insulation resistance performance. Therefore, this material was chosen as the core dielectric for the FC/PBGA carrier.

Discussion of the Chip Carrier Structure

Figure 4 shows the front (flip-chip-side) and the back (BGA side) of the complete carrier extracted from the manufacturing panel. As it has already been mentioned, the 21 mm x 21 mm size carrier contained four levels of circuitry and two voltage, reference planes. It had 700 controlled-collapse-chip-connections (C4) for flip-chip attachment of a 12 mm x 14 mm die, and 255 BGA connections for 2nd level assembly. We assembled a test chip to this carrier which had the same foot-print as the target functional chip. The test chip contained several specialized electrical nets that allowed us to detect chip

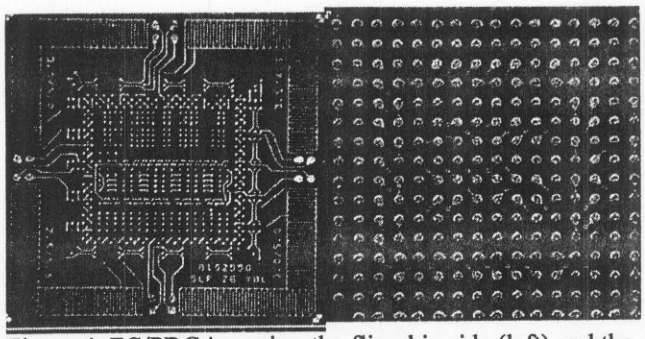


Figure 4. FC/PBGA carrier; the flip-chip side (left) and the corresponding BGA side (right).

cracking and electromigration at the interlevel dielectrics. These nets were utilized in addition to the test nets described already in table 1. The chip also had temperature sensors, and heating devices for the power-cycling test.

One serious challenge in the building of the carrier was the development of an adequate registration procedure that could be employed in the panel manufacturing environment. To register the 150 μm (6 mil) diameter capture pads of the 100 μm (4 mil) SLC microvias over the 49.5 cm x 58.8 cm (19.5" x 24") panel size, the resolution of an optical exposure-registration system had to be better than 5 μm. To achieve acceptable yield, significant effort was spent studying the effect of various processes on the dimensional stability of the panels. Through this effort we determined several new process control parameters. These proved especially useful in the surface preparation and planarization of the laminate before application and after cure of the SLC dielectric layer.

Other challenges included controlling the width of the 75 μm signal lines at the S2/S2' level as well as the photoresist removal step from the microvias prior to the SLC additive circuitization. We also identified that the eutectic Sn/Pb plating did not provide adequate quality of

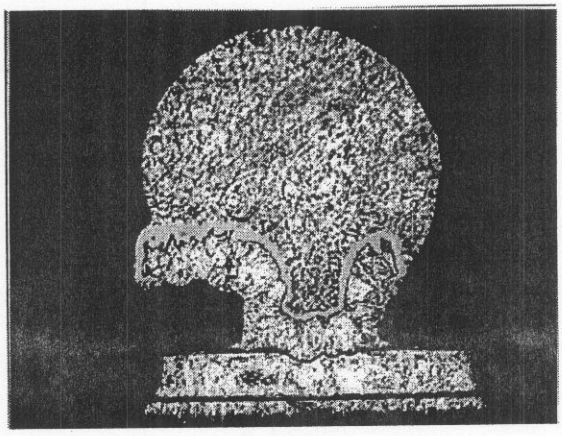


Figure 5. C4 Screen Printed Microvia

the C4 bumps. Therefore we investigated and employed screen-printing as the alternative bumping technique. Recently, several companies and packaging consortia started investigating this technology for bumping FC products such as wafers, ceramic and organic carriers, and printed wiring boards [16,17].

Figure 5 shows a crossection of a typical screen-printed C4 ball over a microvia. Using this technique we were able to control the volume of the solder deposit with required precision and eliminate voids that were discovered inside the Sn/Pb plated C4 joints.

Thermo-Mechanical Characteristic of the Module

Important factors in optimizing the construction of the package were the relative mechanical compliance and mismatch between thermal-expansiveness of the silicon chip, the underfill material, and the chip carrier. We

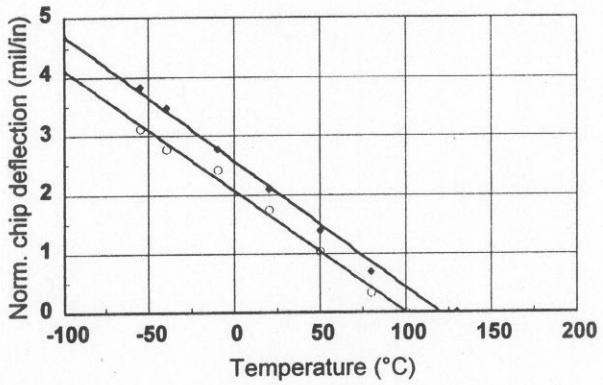
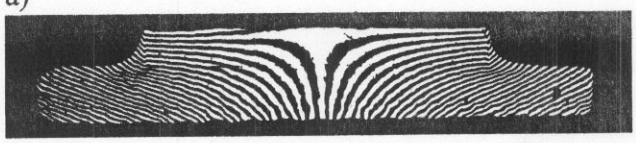


Fig.6. Maximum chip deflection measured for two underfills: (a) T_G =130 °C, and (b) T_G =100 °C

analyzed the thermally induced deformations and the corresponding local shear deformation modes by using Moire interferometry. Figure 6 represents an example of the maximum chip deflection for two assembled modules, measured by the Shadow Moire method. The deflection was measured at temperatures from –55 °C to 160 °C and normalized to the chip length. Module A was underfilled using a commercial, thermosetting resin with a glass-rubber transition temperature of about 130 °C. The underfill material in module B had a glass-rubber transition temperature of about 100 °C. It is seen that the maximum deflection of the chip assembled to the carrier decreases with increasing temperature, until the package becomes flat. The temperature at which the package is flat can be defined as the stress-free temperature. At this temperature, the chip becomes mechanically de-coupled from the carrier. According to the results shown in Fig. 6 the stress-free temperature for module A is about 130 °C and about 100 °C for module B. These temperatures coincide with the glass-rubber temperature of the corresponding underfill materials. This indicates that the deformation of the package is primarily dependent on the coupling between the chip and the carrier through the underfill material. Figure 7 shows the horizontal and vertical displacement fields obtained for module A by Moiré interferometry. The relative displacement between the chip and the carrier was induced

a)



(b)

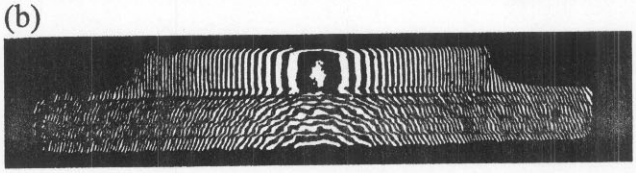


Fig. 7. Moiré fringe pattern for FC/PBGA assembly under thermal loading of $\Delta T = -60°C$. (a) - horizontal displacement; (b) vertical displacement.

by thermal loading of $\Delta T = -60°C$. The fringe patterns indicate rather significant bending of the assembly. The horizontal field shown in Fig. 7 a. corresponds to compressive strains at the BGA side (bottom) of the assembly and to a relatively small strain at the top of the chip. The vertical field shows deflection of the chip and bending of the carrier due to a larger coefficient of thermal expansion of the chip carrier compared to that of the chip. The curvature greatly exceeds that of thermally balanced ceramic packages, but it is typical for plastic assemblies.

The thermo-machanical analysis confirmed that the package has been properly designed and constructed. The analysis also helped to select appropriate materials for the laminate, the SLC layer and for the underfill in order to secure its reliable performance. Finally, it provided quantitative information on how these materials affected the thermo-mechanical response of the assembled module under various conditions.

Stress testing results

The reliability stress tests were performed in two steps. In the first step, we evaluated a small number (about fifty), of assembled modules. These results were used to eliminate weak points in the chip carrier construction, and to assess the development effort and the effectiveness of the quality controls. These data were also used as feedback to fine-tune the manufacturing process. This early reliability assessment was based on the Unbiased Autoclave Test (PCT, 121 °C, 100 %RH, 96 hours) and on the Deep Thermal Cycling (ATC, JEDEC A104-A condition C, 1020X –65 °C to 150 °C). During the stress tests, the modules were periodically evaluated using acoustic microscopy and visual inspection. Comparison of acoustic images obtained before the stress tests with images that were obtained during and after the stress, indicated that the risk sites were rather stable during stressing and did not develop areas of delamination or defects that could grow with the stress duration. The failure analysis was concluded using the acoustic imaging results, cross-sectioning and microscopic examination of the stressed parts. These results helped to make the final selection of the underfill material and the soldermask. They also prompted our decision to replace the Sn/Pb bumping by the screen-printing method.

In the second step, we increased the sample size to qualify the manufacturing line. Hardware that met the engineering specification was preconditioned and tested according to the reliability test matrix outlined in Tab. 2. In several tasks, we substantially exceeded the test duration and the number of stress cycles that are recommended in the technical literature. Below we report the stress testing results with emphasis on performance of the most novel and challenging elements of this carrier.

The SLC dielectric layer

Extensive cross sectional analysis did not reveal any symptoms of delamination between the SLC dielectric and the solder mask, nor between the SLC and the corresponding laminate carrier. Neither the PCT stress nor the DTC stress generated any particular type of defect within the SLC. Although initiation of cracking of the SLC layer has been sporadically observed on a number of cross-sections, it resulted from stresses initiated during manufacturing. Similarly, the dielectric performance of the SLC layer has been confirmed. Specifically, its immunity to electromigration across and along the interfaces has been verified up to temperatures determined earlier from the fundamental dielectric study.

Filled-Plated-Through-Holes

Filled-Plated-Through-Holes (FPTHs) represent a relatively new feature in the chip carrier packaging, for which reliability data is rather limited. Used in combination with microvias, the FPTHs maximize the density of the C4 joints

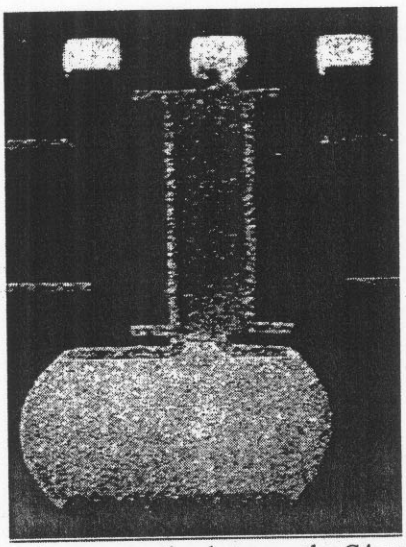


Fig. 8. Direct interconnection between the C4 and the BGA joints, which utilizes FPTH and microvias

while minimizing the number of the circuitry layers. Such connectivity structure simplifies the manufacturing process and relaxes tolerances of the process controls. Figure 8

shows an example of the direct interconnection between a C4 joint and a BGA joint, utilizing FPTHs and microvias. It was our expectation that under the severe conditions of the PCT stress test and the ATC stress test, even a minor deficiency in the FPTH construction would be revealed. According to the analysis of the test results, the performance of most of the PTHs was quite satisfactory through the stress conditions. Some defects, such as loss of adhesion between the filler and the copper barrel were observed. These did not, however, result in electrical failures.

Microvias

The near chip scale size FC/PBGA package contained 158 microvias connected directly to C4s and 88 microvias plated over the FPTHs. Therefore, the reliability of a wiring net with microvias can be a complex function, dependent on several risk factors. The failure analysis showed that the vast majority of the examined microvias were able to withstand all the stress conditions (Tab. 2) without compromising the integrity of the interconnection. In a few instances however, the microvias showed cracks or partial separation. These resulted from thermal expansion of either large voids in the plated BGA solder, or FPTHs covered with copper that was too thin. For example, figure 9 shows that expansion of the filler during thermal cycling led to

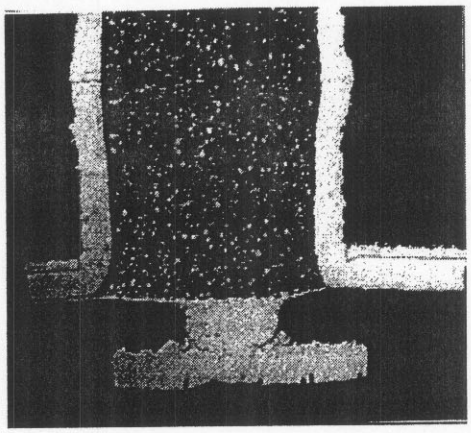


Fig. 9. Microvia connected directly to the FPTH after the temperature cycling test.

partial separation of the filler from the PTH barrel which initiated a crack in the consecutive microvia.

It is worthy to note that after over several thousand ATC cycles, the FPTH-microvia interconnections maintained electrical continuity within passing criteria.

Unerfill Delamination

Some symptoms of limited loss of adhesion between the chip and the underfill were detected in the PCT stressed modules. The defect was typically observed as a 5μm-15μm thick separation, spanning between the bottom of the die and the low Tg underfill B. The separation initiated typically at the chip edge and propagated a limited distance, affecting only few C4 joints. Thus, the majority of the C4 joints appeared to adhere well to the underfill material. It was observed during the first step of this evaluation, however, that the filler of the encapsulant B settled during curing, causing the bottom of the die-to-underfill-interface to separate. In contrast, little or no separation was observed with underfill A, in which the filler was relatively uniformly dispersed. The PTC stress seemed to have little effect on the die-underfill adhesion, which suggests that accelerated moisture adsorption remains the primary driving force responsible for the chip separation defect described above. The acoustic images indicated that some modules were assembled with a certain degree of voiding present within the underfill. During stressing, the voided areas showed a non essential enlargement without indication of a catastrophic delamination or loss of electrical continuity of the C4 test nets involved. Typically, the voids formed small bubbles, the size of the C4 ball, which did not cause any secondary defect.

Stress Test Electrical Failures

The defective sites were identified after detection of a stress-related drop in insulation resistance (IR) of the IR nets, or an increase in continuity resistance (ΔCR) of the interconnection nets. The failure criteria were as follows: IR < 1 MΩ (< 10 MΩ 2^{nd} level) for the insulation resistance and $\Delta CR > 10$ mΩ or 10% of time zero for the continuity resistance. Most of the tests performed in accelerated stress conditions are fairly well known and commonly used in engineering practice. The Power Cycling test (PX), however, is rather new and was designed to gain a better understanding of the interconnection fatigue in simulated field conditions. This test does not involve any significant acceleration. Rather, it relies on a large number of cycles in relatively short time. During the test, the heaters of the chip were activated periodically to simulate the chip ON/OFF thermal conditions as it is indicated in table 2. Most of the hardware that we tested performed without any failures. A small numbers of failures that resulted from the ATC testing and the PX testing were attributed to manufacturing process defects that escaped the quality controls. For example, the thickness of the cap over the failed FPTH shown in figure 9 was too small, violating the conductor thickness specification. The PCT test, the THB test and HTS test concluded without failures. We expected and detected, however, a growth of anodic filaments over the glass fiber surface in certain type of laminates (Fig. 3a and b). This led to a number of late-shorts during HAST testing.

CONCLUSION

Based on the detailed dielectric-relaxation-spectroscopy measurements, we determined optimal conditions for photo-exposure and thermal cure process of the SLC, phtoimageable dielectric layer. The resulting composite material showed satisfactory dielectric properties and improved aging resistance during environmental stressing. Similar work performed on several fiber-glass-epoxy laminates let us identify a laminate material of low moisture absorption and exceptional immunity to the plated-fiber-

defects. We selected these materials as a foundation for the near-Chip Scale Package. The package was successfully fabricated using the flip-chip, plastic-ball-grid-array-microvia technology. The 4S2P structure with 256 BGA connections accommodated a chip with 700 C4s. Measurements of stress concentration and thermal expansiveness during thermal loading indicated that the mechanical construction of the package was optimally designed and should withstand accelerated stress conditions at an acceptably low failure rate. The predictions of the dielectric evaluation of the materials, and the results of mechanical modeling were verified through a series of systematic standard reliability tests. The circuitry of the test chip, the carrier and the card for the 2nd level assembly was carefully designed. The reliability test vehicle was equipped with a large number of risk sites that included all-essential interconnection and interfacial attributes of this novel construction. It has been determined that this plastic, Flip-Chip-BGA carrier with microvias, is manufacturable, and can satisfy the standard reliability requirements of chip-scale packaging.

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