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Embedded Capacitance Materials and Their Application in High Speed Designs

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Abstract
Discrete decoupling capacitors become ineffective in higher speed systems due to inductance associated with interconnection. Decoupling can be achieved using embedded capacitance materials that make use of the capacitance of closely spaced power and ground planes. The approach improves electrical performance, frees surface real estate, and eliminates solder connections, which can lead to improved reliability. In this paper, we review three material options for embedded capacitors: thin FR4 epoxy-glass laminate, adhesiveless copper on polyimide substrate, and unsupported epoxy filled with high dielectric constant ceramic powder. Characteristics including material components and construction, dielectric constant and loss, and topography at metal-dielectric interfaces are compared. Attention is given to frequency dependence of the different material properties. Effects of the material characteristics on electrical performance, including capacitance and power and ground plane impedance, are examined. Finally, processing and fabrication issues are discussed.

Introduction
Trends for electronic devices include higher frequencies, lower voltages, and larger currents. At the same time, end users require increased functionality, smaller form factors and lower cost. Embedded distributed capacitance is a technology developed to address some of these needs. The technology involves using the capacitance of closely spaced power and ground planes as a local source of charge for decoupling purposes. The technology can reduce the number of discrete capacitors on the board, and advantages can include improved electrical performance, reduced board size, and potential improvements in reliability through the elimination of solder joints.

The use of conventional laminate with closely spaced power and ground planes to replace discrete capacitors on a multilayer printed circuit board has been known for years.[3] More recently, there have been efforts to develop thin laminate with ceramic powder filled dielectric in order to increase dielectric constant and capacitance.[4-5] These organic-ceramic hybrid materials have shown promise for embedded power-ground decoupling planes with desirable low impedance.[6] Properties,[7] performance,[8] and processing[9] of a number of embedded capacitance materials were studied in an Embedded Decoupling Capacitance Project supported by the National Center for Manufacturing Sciences.

From the viewpoint of decoupling, a power-ground plane capacitor can source the charge as long as its impedance is lower than the device input impedance. The best performance would be indicated by an impedance response that is close to zero at all frequencies. The power-ground planes made of typical dielectric materials exhibit undesired multiple resonance that can be mitigated by adding discrete decoupling capacitors. This approach introduces inductive components, which contribute to the equivalent inductance of the power plane and eventually limit the usable bandwidth.[10-11] Application of thin power-ground plane dielectric layers can suppress fluctuations in impedance by damping the resonance, which extends the usable bandwidth to higher frequencies. It has been suggested that in thin layers of low loss dielectrics the resonant damping can be due to conductive losses of the metal cladding[12] and a decreased dielectric thickness.[13]

Gould Electronics has introduced a distributed embedded capacitance material called TCC™ foil (T-foil). The material is an adhesiveless flexible laminate having a thin, unfilled polyimide dielectric.

The purpose of this paper is review the new material and compare it to thin conventional FR4 laminate and laminate with ceramic powder filled dielectric. Characteristics including material construction, dielectric constant and loss, and topography at metal-dielectric interfaces are compared. Effects of the material characteristics on capacitance and power and ground plane impedance are examined. Finally, processing and fabrication considerations are discussed.

Material Overview

The basic constituents of the three embedded capacitance materials are given in Table 1.

Table 1 - Constituent Materials

Material	Dielectric Resin	Support/ Filler	Copper Type
T-foil[14]	Polyimide film	None	ED: Direct Deposited
BC2000 or BC [15]	FR4 Epoxy	Woven Glass	ED Foil: DT, RTC
C-Ply or FE[16]	Epoxy	$BaTiO_3$ Powder	Rolled Foil

In the table, *ED* refers to electrodeposited copper while *DT* and *RTC* refer to double-treat and reverse-treat copper, respectively.

Resin type and filler determine dielectric constant (Dk) and loss, which are compared in Table 2.

Table 2 - Dielectric Properties

Material	Dielectric Constant (1 MHz)	Dissipation Factor (1 MHz)
T-foil	3.1	0.003
BC[17]	4.1	0.015
FE[5]	14 - 18[18]	0.005[18]

T-foil Dk is determined solely by the Kapton[19]-E base film. It is comparable to the Dk of epoxy resin without filler, which is about 3.45.[20] The Dk of glass is about 6.2,[20] and that of barium titanate can be as great as 5000.[21] The large Dk of the fillers increase Dk of FE and BC above that of the epoxy matrix alone. Dielectric constant increases with filler volume fraction.[7] The dependence on volume fraction explains the ranges of values given in the table for FE. The BC material Dk also exhibits dependence on filler (glass) content, but to a lesser degree than FE[7] .

All three materials have thin dielectrics to increase capacitance density. TCC dielectric thickness is determined by the availability of thin polyimide films. It is typically 25 µm thick, although polyimide films as thin as 12.5 µm are available. FE dielectric thickness is determined by the ability to solution coat a continuous film. Dielectrics as thin as 4 µm have been described in the literature.[5] Commercial thickness between 8 and 16 µm is expected to be typical. BC dielectric thickness is determined by the availability of thin core pre-preg. A thickness of 50 µm is commercially available in volume. Thickness of 25 µm is under development.

Copper thickness of each of the three materials is typically 35 µm. Thick copper is used to reduce voltage drop across the power distribution system.

Copper type has implications to the metal - dielectric interface topography. T-foil copper is mostly electrodeposited; it is built-up on top of a sputter deposited seed layer. The interface topography is very smooth, closely matching that of the base polyimide film. Average roughness (Ra) is less than 40 Å and peak-to-valley roughness (Rtm) is less than 100 Å, as measured in a 1 µm x 1 µm scan by atomic force microscope.[22] BC and FE use free standing copper foils in their manufacturing. The interface topography of BC is determined by the roughness of the treated shiny-side surface of double-treat copper. Typical roughness is about 0.4 µm Ra and 3.5 µm Rtm. Similarly, topography for FE is defined by the roughness of treated, rolled copper. Typical roughness for treated rolled copper can be about 0.1 - 0.2 µm Ra and 1 - 1.5 µm Rtm depending on treatments. The foil-based materials have significantly rougher interface. This can have implications with respect to skin effect and conductor losses as will be discussed below. Too large roughness could result in localized dielectric thickness variation and increase high potential dielectric breakdown (hipot) failures.

Capacitance

The capacitance, *C*, available from an embedded capacitor material is given by the equation for a parallel plate capacitor, Equation 1:

$$C = \varepsilon_0 \varepsilon_r A / h \qquad (1)$$

where ε_0 is permittivity of free space, ε_r relative dielectric constant, A is area and h is dielectric thickness. Capacitance per unit area was calculated using Equation (1) and Dk and thickness values typical for the three materials. Results are given in Table 3.

Table 3 - Calculated Capacitance Density

Material	Dielectric Constant (1 MHz)	Thickness (Microns)	Capacitance Density (pF/cm^2)
T-foil	3.1	12.5	216
		25	108
BC	4.1	25	143
		50	71
FE	18[18]	8	1962
		16	981

FE has the largest capacitance density because it is thinnest and has the highest dielectric constant among the materials listed. T-foil can have higher capacitance density than BC because it is thinner, even though Dk is lightly lower. For a given board size, higher capacitance density implies greater total capacitance and the possibility of replacing more discrete components. Additional embedded capacitor layers can be connected in parallel in a multilayer printed circuit board (MLB) to increase effective capacitance.

Capacitance is frequency and temperature dependent based on properties of the dielectric. Frequency dependence of T-foil dielectric constant and loss are given in Figures 1 and 2.

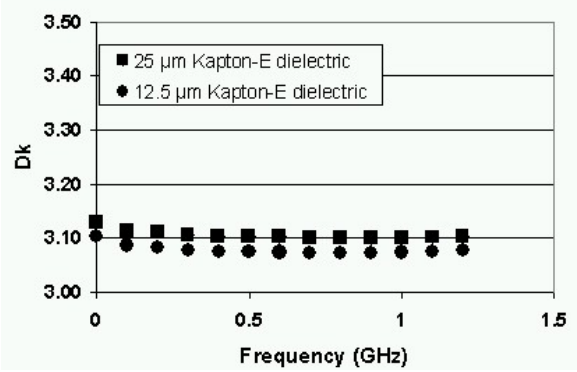

Figure 1 - Dielectric Constant of T-foil

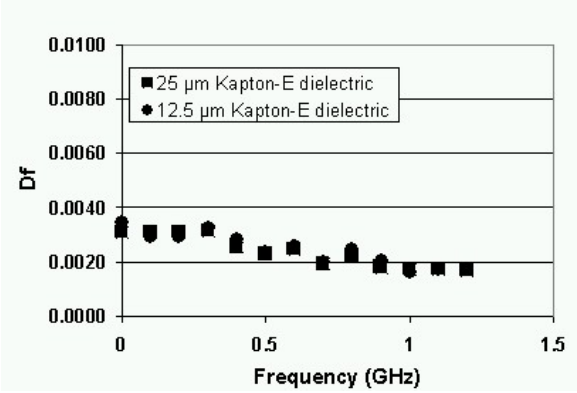

Figure 2 - Dissipation Factor of T-foil

The data were obtained by a certified independent laboratory and measured in accordance with IPC-TM-650 Method 2.5.5.9. Dielectric constant, and capacitance, change little (~ 1 %) between 1 MHz and 1 GHz. A decrease in loss is observed over the same frequency range, although increases are observed at frequencies above 1 GHz.. Slightly larger changes in Dk are observed for BC and FE. For BC, dielectric constant decreases to 3.94 at 1 GHz from 4.13 at 1 MHz[17] (~ 4.6 %) For FE, about 5 % reduction was reported between 1 KHz and 1 GHz[4]. Decreases in capacitance in accordance with to those of the Dk changes of each material might be expected over the same frequency ranges.

Temperature dependence of T-foil capacitance was determined over a range of temperatures between 25 and 150 °C. Capacitance was determined from impedance measurements that were made over a range of frequencies less than 10 KHz. T-foil capacitance is very stable with temperature, exhibiting less than 3 % change over the temperature range. This surpasses a ± 15 % specification. Capacitance of BC was determined over the same temperature range using the same technique. A variation of 9 % was observed. FE temperature variation is reported to be less than 15 % over a temperature range between -40 °C and 125 °C[5].

When used as power and ground plane, the interplane capacitance of embedded materials will provide most of the initial current to fast switching devices[23]. For CMOS devices, current is typically drawn as a burst immediately after a clock edge.[24] These ideas imply that the amount of capacitance in a small fixed time interval is of interest in high frequency designs.

A simple extension of Equation (1) can provide insight. At a fixed location on a MLB, the maximum distance a signal can propagate in the fixed time interval can be thought of as defining the maximum area of the embedded capacitor. Propagation velocity, v_p, is related to dielectric constant by Equation (2),

$$v_p = c / (\varepsilon_r)^{0.5} \qquad (2)$$

where c is speed of light. Substituting a circular area defined by v_p into Equation (1) yields an expression for maximum available capacitance, C_t, in a fixed time interval, t:

$$C_t = \pi \varepsilon_0 c^2 t^2 / h \qquad (3)$$

Maximum available capacitance in a fixed time interval is independent of dielectric constant. Increasing dielectric constant does increase capacitance density. However, lower dielectric

constant increases velocity and effective area, and the effects on capacitance may cancel out. This concept is illustrated in Table 4. A one nanosecond time interval and 25 µm thickness are assumed.

Table 4 - Capacitance in Fixed Time Interval

Quantity	T-foil	BC	FE
Dielectric Constant (1 MHz)	3.1	4.1	18[18]
Velocity (cm/ns)	17	14.8	7.1
Area (cm^2)	912	690	157
Capacitance Density (pF/cm^2)	108	143	627
Capacitance (nF)	98.5	98.5	98.5

The analysis suggests a device would draw similar burst current in a fixed time interval whether high or low dielectric constant materials are used as embedded capacitor materials. For the low Dk material, a greater proportion of board area would be utilized. Board size and location of device on the board could become constraints. Also, multiple devices drawing current simultaneously could be more likely to compete for available charge.

Reduced dielectric thickness increases capacitance in a fixed time interval as well as capacitance density. The thinner constructions of FE and T-foil are advantageous.

Power-Ground Plane Impedance

In order to analyze the effect of the dielectric thickness, dielectric constant, loss and conductive loss on the impedance characteristics, we performed a full wave numerical analysis of several power planes using a High Frequency Structure Simulator from Ansoft Corporation (Ansoft HFSS™). The power plane model was formulated based on the geometry and materials properties, without any prior assumption about the nature of the network equivalent circuit. The scattering parameters S_{11} and the input impedance have been obtained in the frequency range of 100 MHz to about 5 GHz for 5 cm x 8 cm power planes with 12.5 µm to 100 µm thick dielectric. The dielectric constant and the dielectric loss were chosen to represent the embedded capacitance materials. The dielectric materials were clad with 35 µm conducting planes having conductivity of copper, 5.8 10^7 S/m.

Figure 3 shows the input impedance calculated for 5 cm x 8 cm power planes 50 µm, 25 µm and 12.5 µm thick having the dielectric constant, ε′, of 3.8 and the dielectric loss tangent of 0.015 at 1 GHz. For the largest thickness, this model may be representative of a thin FR-4 laminate such as BC. The result for plane (a) shows a well-known undesired resonant behavior. A series resonance at about 480 MHz is followed by a first cavity resonance at about 930 MHz. At higher frequencies, the layer (a) exhibits several resonant oscillations, due to excitation of higher order modes. The frequency dependent input impedance characteristics calculated for the 25 µm thick plane (b) and the 12.5 µm thick plane (c) are similar to that of the 50 µm thick plane (a). It is seen that decreasing the dielectric thickness shifts the series and cavity resonance slightly towards lower frequencies, while the amplitude of the cavity resonance decreases.

The results of theoretical calculations shown in curve (a) in Figure 3 and curve (a) in Figure 6 below were evaluated experimentally and described previously[25]. The experimental results agree well with the calculated data, except that the measured input impedance increases with frequency. This effect results from uncompensated inductance of the testing probe, which is a common source of systematic errors in high frequency measurements.[25]

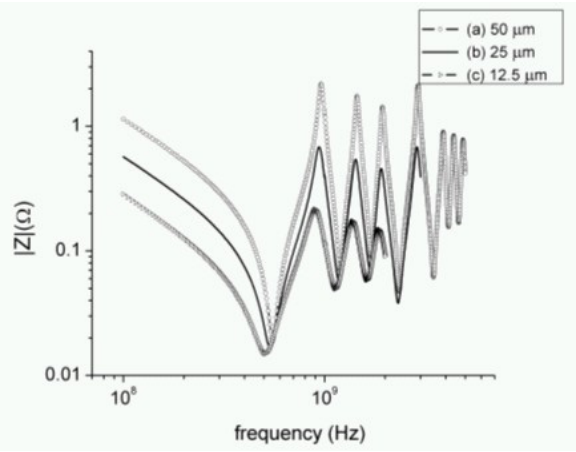

Figure 3 - Input impedance calculated for 5 cm x 8 cm power planes, Dk=3.8, tan(δ) = 0.015

Impedance characteristic for a 25 µm and 12.5 µm thick power planes having the dielectric constant of 3.2 and the dielectric loss tangent of 0.002 are shown in Figure 4. This model represents a T-foil dielectric material. As expected, the resonant frequencies are slightly higher than those in Figure 3, due to lower dielectric constant. In the case of 25 µm thick plane (a) the series resonance is at about 600 MHz, followed by the first cavity resonance at about 1.05 GHz. In the case of the 12.5 µm thick plane (b), the series LC resonance is at about 570 MHz, while the first cavity resonance is located at 1.01 GHz. The curves indicate that the material exhibits primarily capacitive character and can easily approach

impedances below one ohm. The resonant oscillations are clearly suppressed in the thinner dielectric leading to the lowest impedance values. Compared to FR4 type laminate, lower impedances are possible because thinner constructions are available.

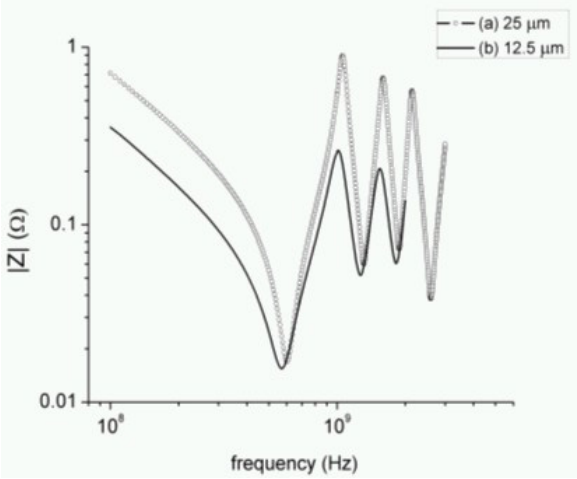

Figure 4 - Input impedance calculated for 5 cm x 8 cm power planes, Dk=3.2, tan(δ) =0.002

Figure 5 shows the impedance characteristic for a plane with dielectric constant of 18 and dielectric loss tangent of 0.02. The dielectric thickness is 25 µm in plot (a) and 16 µm in plot (b). Plot (b) may be representative of a 16 µm thick FE laminate. For the 16 µm plane, the LC resonance results in a minimum of impedance at about 235 MHz, while the first cavity resonance is located at about 415 MHz.

In comparison to the results shown in Figure 3 and 4, the FE type laminate exhibits series resonance and cavity resonance oscillations beginning at significantly lower frequencies. The oscillations are shifted to the lower frequencies due to the higher Dk, which decreases the velocity of the propagating wave in the dielectric.

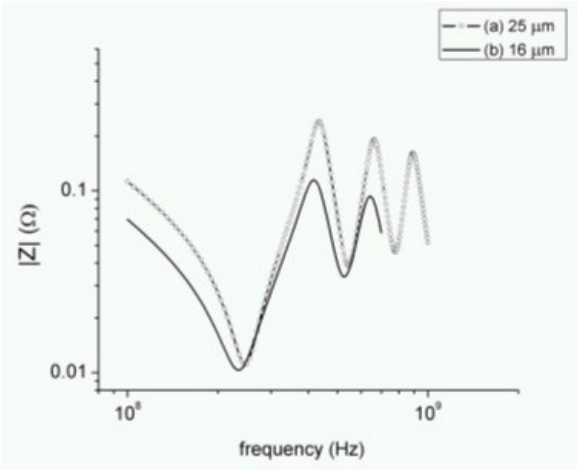

Figure 5 - Input impedance calculated for 5 cm x 8 cm power planes, Dk=18, tan(δ) =0.02

Referring again to Figure 5, the amplitude of the oscillations of the input impedance resulting from resonance is considerably suppressed compared to those in Figures 3 and 4. Furthermore, the magnitude of impedance remains consistently below 0.1 ohm at all frequencies for plot (b) in Figure 5. Thus, combination of smaller dielectric thickness (16 µm) and higher dielectric constant (Dk = 18) results in significant lowering of the impedance and suppression of the resonant behavior.

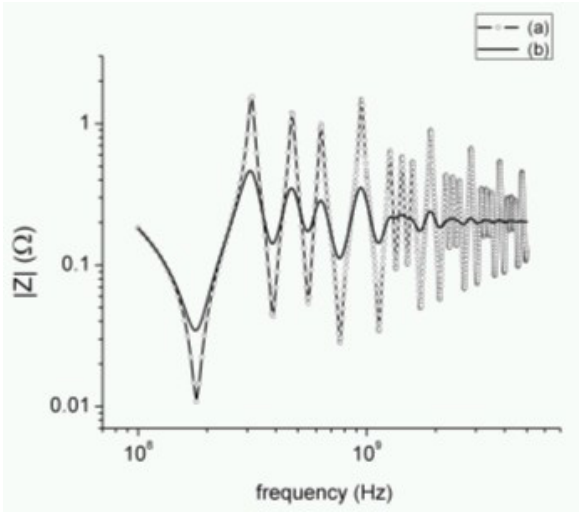

Figure 6 - Input impedance calculated for 5 cm x 8 cm, 100 µm thick power planes, Dk=38, (a) tan(δ) = 0.015, (b) tan(δ) = 0.15

The magnitude of the oscillations in curve (a) in Figure 5 (t = 25 µm, Dk = 18) are comparable to those in curve (b) in Fig. 5 (t = 12.5 µm, Dk = 3.2). This suggests that reducing thickness is more effective than increasing Dk in damping impedance oscillations. This observation is consistent with other analyses based on equivalent circuit models[13].

To further investigate effects of dielectric constant, impedance calculations were performed for a 100 µm thick plane with a dielectric constant of 38 and a dielectric loss tangent of 0.015. Results are shown in curve (a) in Figure 6. The first minimum in impedance is seen at about 180 MHz, while the first cavity resonance is located at about 315 MHz.

Again, resonances are shifted to the lower frequencies as a result of reduced velocity of the propagating waves in the dielectric. The magnitudes of impedance and the resonance oscillations are comparable to those observed in Figures 3 and 4. The order of magnitude larger dielectric constant is not sufficiently effective in reducing oscillations to offset the 4X greater thickness of the laminate.

Two mechanisms for suppressing resonance oscillations are conductor losses and dielectric losses. An expression for loss factor, α, for a low loss transmission line is given by Equation 4,[13]

$$\alpha = R/2Z_0 + GZ_0/2 \qquad (4)$$

where R is resistance of conductor, G is parallel dielectric loss, and Z_0 is characteristic impedance. The equation can provide insight to power plane behavior because the planes can be modeled as an array of lossy transmission lines[13]. The second term on the right in Eq. 4 describes contribution due to dielectric loss. Based in part on this equation, increasing dielectric loss should help to damp resonance behavior. Referring to Figure 6b, our calculations show that increasing the dielectric loss tangent to 0.15 suppresses resonant oscillations considerably. The resulting impedance characteristics are exceptionally flat over a broad frequency range. Our present calculation and earlier experimental evidence[25] suggest dielectric loss can be sufficient to suppress resonance oscillations.

We were unable to complete simulations of the effect of skin effect and conductor loss on impedance characteristics. However, the first term on the right of Equation 4 describes contribution due to conductor loss. As frequency increases, conductor loss contribution increases due to higher R arising from reduced skin depth. Furthermore, characteristic impedance in the first term is proportional to thickness making the first term inversely proportional to thickness. Hence, attenuation due to conductor losses is enhanced as dielectric thickness decreases. Our calculations, which show effective suppression of resonant oscillations with decreasing dielectric thickness, could be consistent with increasing conductor loss contribution.

It has been suggested that conductor loss in thin power and ground planes may be sufficient to damp resonance oscillations when skin depth is the same order as dielectric thickness.[8] At 1 GHz, skin depth in copper is a little greater than 2 µm. Dielectric thicknesses we considered were not that thin, and incomplete suppression of resonance oscillations in our calculations is understandable. However, skin effect losses can be magnified if root-mean-square (RMS) roughness is comparable to skin depth.[26-27]

Based on values presented earlier, Rtm roughness of electrodeposited DT and rolled copper foils are comparable to skin depth at 1 GHz. While Ra roughness is clearly lower for the two foils, the added interface roughness could contribute to higher conductor losses for the two foil based materials. More work is needed to characterize the effects of conductor loss on the performance of thin power planes.

Processing/Fabrication

The T-foil material is flexible, free-standing and non-brittle. There are no issues with innerlayer circuit images singulating from the core during processing. Materials like the BC and FE have inherent handling challenges because they are thin and brittle. BC and FE typically require the standard copper borders to be replaced with full copper border to the panel edge to minimize material cracking and part singulation. These materials may also require a design modification to provide overlapping features on the power and ground layer in order to maximize strength and minimize part singulation. This typically means the finished PCB will have the copper on the ground layer out to the edge of the board[9]. This modification would require acceptance by the customer prior to the board manufacturing. Another approach to addressing brittleness issue is to use a sequential build-up lamination strategy. T-foil requires no such design changes for successful handling.

All of the materials are very thin and typically require leaders or frames through the image, etch, and strip processes unless the PCB fabricator has equipment specifically designed to handle thin laminates. Cut sheet or postage stamp photoresist application to the BC and FE may need modification.

The materials can require a pre-bake before etching for dimensional stabilization and moisture removal. It is recommended for the T-foil material to be pre-baked prior to lamination to ensure moisture removal.

Desmear processing of these thin materials must be evaluated to ensure compatibility with the dielectrics and proper cleanliness of the copper post of the layer. For T-foil, the process cycle is typically in the low end to eliminate undercut at the copper-polyimide interface. BC and FE can have similar process modifications for acceptable hole quality.

Summary and Conclusions

Characteristics of three embedded capacitance materials have been reviewed. The three materials are a flexible, adhesiveless polyimide-based laminate (T-foil), a thin conventional FR4 laminate (BC), and an epoxy-ceramic powder composite (FE). All three materials are thin, with the T-foil and FE having the thinner constructions and therefore greater capacitance density. The FE material exhibits highest capacitance density as it is thinnest and has the highest dielectric constant. Capacitance in a fixed time interval is independent of dielectric constant.

Added capacitance due to larger dielectric constant may be offset by increased effective area from higher propagation velocity for lower Dk material. Capacitance in a fixed time interval can be increased by reducing dielectric thickness.

The high frequency impedance of dielectric power planes characteristic of the three materials has been modeled using a full wave numerical analysis without equivalent circuit assumptions. The response was found to be consistent with a capacitive load, without significant contribution from the circuit inductance that typically causes a series LC resonance and dominates the high frequency response. Impedance oscillations due to resonance were observed at high frequencies. However, impedances well below 1 ohm were obtained with thinner constructions.

Increased dielectric constant reduces the frequencies at which resonances begin and suppresses the magnitude of impedance oscillations. Thin dielectric is more effective at suppressing oscillations than higher dielectric constant. Our results may be consistent with conductor loss contributing to suppression of impedance oscillations. The simulation indicates that the material dielectric loss could play a significant role in suppressing the resonant behavior of power-ground planes.

All of the materials have a certain process uniqueness that must be accommodated in order to ensure successful addition into an MLB. For the thin, brittle, epoxy-based materials, effort is necessary to minimize cracking and innerlayer circuit singulation. For the polyimide based material, low end desmear process cycle is recommended to eliminate undercut. Elimination of moisture should be ensured for all three materials.

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