IMAPS International

Advanced Technology Workshop on

March 12-14, 1999

Chateau Elan, Braselton, Georgia

Flip Chip technology

Abstracts and Final Program

General Chair:
Daniel F. Baldwin, *Georgia Tech*

Technical Chair:
R. Wayne Johnson, *Auburn University*

SUNDAY, MARCH 14

BREAKFAST: 7 AM - 8 AM

SESSION 5: BUMPING

8 AM - 10:30 AM

Chair: Curt Erickson, *IC Interconnect*

22. Flip-Chip with MMICs off the Shelves
C. Drevon, S. George and A. Coello Vera, *Alcatel Space Industries*

23. Electroless Ni Bumped Flip Chip Interconnections on an Organic Substrate using Anisotropic Conductive Adhesives/Films (ACAs/ACFs)
Kyung-Wook Paik, Myung-Jin Yim and Young-Doo Jeon, *Korea Advanced Institutes Science and Technology*

24. A New Process for Solder Bump Fabrication
Ruoh-Huey Uang, Szu-Wei Lu, Ling-Chen Kung, Hsu-Tien Hu, Hsin-Chien Huang, Tsung-Yao Chu, *ITRI*

25. Electroless Wafer Metallization Processes for Flip Chip
A. Ostmann, *Technical University of Berlin*; Ch. Dombrowski, J. Kloeser, R. Aschenbrenner, H. Reichl, *Fraunhofer Institute for Reliability and Microintegration (IZM)*

26. Commercialization of a Low Cost Wafer Bumping Process for Flip Chip Applications
Andrew J.G. Strandjord, Scott F. Popelar, Curtis A. Erickson, *IC Interconnect*

SNACK BREAK: 10:30 AM - 11 AM

SESSION 6: RELIABILITY

11 AM - 2 PM

Chair: Andreas Schubert, *Fraunhofer Institute for Reliability and Microintegration (IZM)*

27. Flip Chip Reliability: Failure Mechanisms involving the under Bump Metallurgy
Frank Stepniak, *Delphi Delco Electronics*

28. Compensation of Thermal Expansiveness in Plastic DCA-Flip-Chip Assemblies using Mechanically Compliant Dielectric
J. Obrzut, *NIST*

29. microDAC Deformation Measurements on Flip Chip Structures
D. Vogel, A. Gollhardt, A. Schubert, B.Michel, *Fraunhofer Institute for Reliability and Microintegration (IZM)*

30. Flip Chip Interconnection using Redistribution Technology
M. Töpper, P. Coskina, K.-F. Becker, O. Ehrmann, H. Reichl, *Technical University of Berlin*

31. Effect of Nonlinear Material Models on the Reliability Assessment of Flip-chip Packages
Wei Ren, Zhengfang Qian, Minfu Lu, Sheng Liu, *Wayne State University*

32. Effects of Bonding Force on ACA Flip-Chip Joining
Zonghe Lai, Johan Liu, *IFV*

LUNCH: 2 PM

Compensation of Thermal Expansiveness in Plastic DCA-Flip-Chip Assemblies using a Mechanically Compliant Dielectric

by
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Differences in thermal expansiveness of the chip and the substrate increase probability of failure of the solder joints. The situation is especially critical for large integrated circuits directly attached to organic substrates using flip-chip and controlled-collapse-chip-connection (C4) technology.

Organic substrates, which consist of alternate dielectric layers of polymeric composites and metallic circuitry, typically exhibit coefficient of thermal expansion (CTE) of 30 x 10^{-6} $°C^{-1}$ to 60 x 10^{-6} $°C^{-1}$. In contrast, coefficient of thermal expansion of chip materials such as silicon, germanium or gallium arsenide, is only about 3 x 10^{-6} $°C^{-1}$ to 6 x 10^{-6} $°C^{-1}$. After attaching the chip to the substrate, the strain from the unequal expansion is absorbed primarily by the C4 solder joints, which are likely to fail when the assembly is thermally cycled. Application of a high modulus underfill, known as encapsulation, can reduce the strain on the solder joints and improve their fatigue life. However, this approach restricts the differential expansion by creating a strong mechanical coupling between the chip and the carrier. Loads acting normally to the substrate surface increase and, consequently, warp both the chip and the carrier. Such deformation can lead to chip cracking during 2^{nd} level assembly and premature failure of the ball grid array joints. Numerous solutions have been proposed to mitigate these problems. Mechanical stiffeners with desirable CTE, embedded as planes inside the laminate structure, can minimize the thermally induced vertical deformation (bending). However, electrical design and manufacturing of organic carriers with mechanical stiffeners is substantially more complicated than the standard laminates.

Alternatively, application of a compliant, low modulus dielectric layer between the chip joints (C4) and the carrier can decrease the thermally induced bending. The use of a compliant dielectric layer as a mechanical decoupler of the chip from the associated substrate is especially attractive for microvia technology. However, formulation of a material with suitable thermal and mechanical properties, process compatibility and satisfactory dielectric performance present a great material and process development challenge.

Model analysis indicates that the optimal thickness of the decoupling layer should range from ¼ to ½ of the C4-underfil gap. The desirable range of the Young's Moduli is approximated between 1.4 x 10^8 N/m^2 (20,000 psi) to 2.8 x 10^8 N/m^2 (40,000 psi). Rubbery, mechanically compliant polymer resins exhibit Young's Moduli well below 10^8 N/m^2, with the glass transition temperature (T_G) below room temperature. Such materials are unsuitable for the decoupling dielectric layer due to substantial shear deformation of microvias and poor dielectric properties at service temperatures, above T_G. On the other hand, epoxy resins with Young's Modulus above 3 10^8 N/m^2 and brittle-elastic behavior would extend coupling of the underfill. In contrast, dielectric and mechanical properties of polymer interpenetrating networks may be tailored in a broad range to achieve a viscoelastic characteristic between the brittle-elastic of epoxy glasses and the rubbery-elastic of elastomers. Interpenetrating polymer networks (IPN's) are a unique type of organic polyblends. They are synthesized by swelling a crosslinked resin with a second monomer (normal IPN) or a plastic resin with a crosslinking monomer (inverse IPN), which then is polymerized in situ. The polymerization reaction can be

induced by UV radiation, thus the material may be selectively patterned by photolithohraphy. The resulting morphology typically consists of a fine, phase separated cellular structure.

To verify these predictions we have investigated thermally induced deformations in assembled plastic FC-BGA packages that carried a 12 mm x 14 mm die with 700 C4 connections. The carrier dimensions were standard 21 mm x 21 mm, 1.27 mm pitch, with 255 BGA joints. The cross-section of the chip carrier consisted of four signal and two power planes (4S2P). The 2S2P portion of the carrier was made of a high glass transition temperature epoxy-laminate ($T_G \approx 180$ °C) using standard sequential drilling and full-panel-copper-plate process. The plated through-holes (PTHs) were completely filled with a CTE-matching copper-particles-epoxy-resin paste. The panels with filled PTHs were planarized, copper plated, circuitized and coated on both sides with a 50 μm thick compliant dielectric layer for microvias, and the die surface circuitry. The compliant, decoupling layer was based on a formulation obtained by swelling a linear-epoxy resin with a multifunctional epoxy monomer. These were mixed with photoinitiator and cross-linking activation constituents to obtain a negatively acting, photoimageable dielectric[1].

The dielectric relaxation spectroscopy data of the photo-cured material showed multiple relaxations, indicating some degree of incompatibility between components of the photo-cured polyblend. The dimension of the corresponding separate phases were in the vicinity of 100 nm. After thermal cure, the extent of molecular mixing in the final composite was considerably higher. The dielectric spectrum of the composite after photo and thermally induced crosslinking indicated that the individual transitions broadened and merged into a single relaxation peak. Similarly, two glass-rubber transitions, one at 135 °C and the other at 115 °C merged into a single transition ranging from 95 °C to 125 °C.

The relative mechanical compliance and thermal mismatch between the die and the carrier were analyzed using Moire′ interferometry[2]. The bending deformation was also studied by measuring deflection of the module as a function of temperature. According to the experimental data, the relative bending of the assembled packages with the compliant layer is smaller than that of the conventional laminate at all temperatures, and approaches zero at about 110 °C. At this temperature the interpenetrating polymer network is in its semi-rubbery state, and therefore, it can simultaneously conform to different thermal expansion rates of the chip and the laminate carrier. This decouples the chip expansion from that of the carrier, which minimize the warping of the assembly at temperatures well below the glass transition of the laminate. In addition, the compliant layer decreases the chip locking temperature, decreasing the stress that is thermally induced or locked during cure of the underfill. The results of the dielectric and mechanical evaluation were verified by executing a series of standard reliability tests. It has been determined that FC assemblies with the compliant dielectric layer can satisfy the standard reliability requirements, and that the construction is suitable for a variety of packaging configurations including the chip scale packaging.

References:

1. J. Obrzut and J. Lauffer, " Effect of Accelerated Environmental Stress on Dielectric properties of UV Cured Epoxy-Resin Films"; MRS Fall Meeting November 27-December 1, (1995), Boston, MA, Symposium on Long Term Performance Issues in Polymers.

2. Y. Guo, "Applications of Shadow Moiré Method in Determinations of Thermal Deformations in Electronic Packaging," the Society for Experimental Mechanics (SEM) Spring Conference, Grand Rapids, MI. (1995)