Determination of Work Functions in the $Ta_{1-x}Al_xN_y/HfO_2$ Advanced Gate Stack Using Combinatorial Methodology

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***Abstract*—Combinatorial methodology enables the generation of comprehensive and consistent data sets, compared with the "one-composition-at-a-time" approach. We demonstrate, for the first time, the combinatorial methodology applied to the work function (Φ_m) extraction for $Ta_{1-x}Al_xN_y$ alloys as metal gates on HfO_2, for complementary metal–oxide–semiconductor applications, by automated measurement of over 2000 capacitor devices. Scanning X-ray microdiffraction indicates that a solid solution exists for the $Ta_{1-x}Al_xN_y$ libraries for $0.05 \leq x \leq 0.50$. The equivalent oxide thickness maps offer a snapshot of gate stack thermal stability, which show that $Ta_{1-x}Al_xN_y$ alloys are stable up to 950 °C. The Φ_m of the $Ta_{1-x}Al_xN_y$ libraries can be tuned as a function of gate metal composition over a wide ($0.05 \leq x \leq 0.50$) composition range, as well as by annealing. We suggest that $Ta_{0.9}Al_{0.1}N_{1.24}$ gate metal electrodes may be useful for p-channel metal–oxide–semiconductor applications.**

***Index Terms*—Combinatorial methodology, complementary metal–oxide–semiconductor (CMOS), equivalent oxide thickness (EOT), flatband voltage, $Ta_{1-x}Al_xN_y$, work function.**

I. Introduction

Aggressive scaling of complementary metal–oxide–semiconductor (CMOS) transistors to meet the requirement of the International Technology Roadmap for Semiconductors has made the traditional gate stack, SiO_2 gate dielectric and polycrystalline Si (poly-Si) gate electrode, unsuitable for future integrated circuits [1]. High leakage current density (J_L), poly-Si depletion, and boron dopant diffusion are the most urgent gate stack problems to be solved [2]–[4]. In the past decade, high-κ gate dielectrics compatible with poly-Si gate processing have been studied extensively, and HfO_2, Hf–Si–O, and Hf–Si–O–N, among others, have been identified as promising replacements for SiO_2 [2], [4]–[6]. However, the selection of metal gate substitutes for poly-Si, which are compatible with the new high-κ gate dielectrics, is not as advanced. For high-performance CMOS applications, the metal gate electrodes must have work functions (Φ_m) aligned with the conduction (4.05 ± 0.2 eV) and valence (5.17 ± 0.2 eV) bands of Si for n-channel metal–oxide–semiconductor (NMOS) and p-channel metal–oxide–semiconductor (PMOS) applications, respectively [7]. This can be achieved with either two metals or one metal processed in two different ways. Among the many metal gate candidates, TaN has shown very useful Φ_m tunability by alloying with various elements [8]–[12]. In particular, $Ta_{1-x}Al_xN_y$ alloys are easily formed with very good electrical and chemical properties [13].

The systematic measurement of Φ_m across the wide composition range of $Ta_{1-x}Al_xN_y$ alloys is not trivial, since capacitor fabrication and characterization based on a "one-composition-at-a-time" approach are extremely time consuming. As a result, to date, only sparse data are available for this metal gate alloy system [14]. Combinatorial methodology enables the generation of a much more comprehensive and uniform data set, since it allows high throughput measurements on a "library" film that contains the entire compositional variation [15]–[17]. The goal of this research is to demonstrate the efficiency of combinatorial techniques for the rapid determination of Φ_m of $Ta_{1-x}Al_xN_y$ metal gate alloys through the deposition of a binary composition spread [18]. We have, for the first time, systematically extracted Φ_m as a function of composition for the $Ta_{1-x}Al_xN_y/HfO_2$ advanced gate stack, using capacitance–voltage (C–V) characterization analysis.

II. Experimental Procedure

$Ta_{1-x}Al_xN_y$ libraries (composition spread films) were fabricated at room temperature in a radio-frequency reactive magnetron sputtering system. Ta and Al targets were mounted in two separate guns and reactively sputtered in Ar/N_2 at a pressure of 0.6 Pa. The chamber is equipped with a moving shutter system, which allows one to reactively sputter wedges of TaN and AlN. The wedge heights can be as small as 0.4 nm.

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The substrate is rotated by 180° between the deposition of alternate TaN and AlN wedges; thus, the library is intimately mixed at the atomic level, even in the as-deposited state. The final library film thickness of 50 nm results from more than a hundred wedge-pair depositions [19]. In this way, the library film is almost pure TaN on one end, and AlN on the other. The library film is about 15 mm × 15 mm in size. To calibrate the wedge profile, and therefore the composition variation across the library, 3-nm-high TaN wedges were deposited with multiple passes of the shutter (≈0.4 nm for each pass). Rutherford backscattering spectroscopy (RBS) was used to determine the Ta areal density (Ta/cm^2) as a function of position on the wedge, which turned out to be linear with the position [19]. The AlN wedges were calibrated by atomic force microscopy profilometry, since they could not be calibrated by RBS due to the similar atomic number of Al and Si. Wavelength dispersive spectroscopy (WDS) was used to verify the composition spread of the library films. Nitrogen stoichiometry was also determined by RBS for a pure TaN_y film; y was found to be equal to 1.24. A scanning X-ray microdiffractometer (D8 DISCOVER with GADDS by Bruker-AXS) was used to study the structure of the $Ta_{1-x}Al_xN_y$ libraries.

Identical $Ta_{1-x}Al_xN_y$ libraries were deposited on four different dielectric stack thicknesses. SiO_2 films, either 4, 5, 6, or 10 nm thick, were grown by steam oxidation on 300-mm-diameter p-type (resistivity of 15 to 25 $\Omega \cdot$ cm) wafers. A 3-nm atomic layer deposited (ALD) HfO_2 film was grown on top of each of these SiO_2 films. Thus, from the C–V analysis of the four libraries [$Ta_{1-x}Al_xN_y/HfO_2(3\ nm)/SiO_2$ (4, 5, 6, or 10 nm)], we could systematically extract Φ_m as a function of gate electrode composition.

III. Results and Discussion

Fig. 1(a) schematically shows the library film, where each dot represents a capacitor. The composition is systematically changing from TaN-rich to AlN-rich along the y-direction. The resulting average composition variation is shown in Fig. 1(b). A wide range of average compositions $x = 0.05$ (±1% atomic ratio) to 0.85 (±1% atomic ratio) was achieved in the library films. Pure TaN and AlN regions are not achievable on the library film because both targets must be sputtered continuously, and there is a small gap between the shutter and the substrate, which allows the introduction of a small amount of material from the Al target, for example, when the Ta target is depositing a wedge. The slight composition shift in the x-direction is due to a small deposition rate variation across the sample area. In order to take this variation into account, we averaged the capacitor data along the isocompositional stepwise rows (example marked in the figure).

Fig. 2(a) shows the diffraction pattern plot of the $Ta_{1-x}Al_xN_y$ libraries taken with a 0.5-mm-diameter X-ray beam. The diffraction was taken with the ω-scan mode, and intensities are integrated in the χ direction for each 2θ angle. As shown in the figure, the intensity of the (111) peak of face centered cubic (FCC) $Ta_{1-x}Al_xN_y$ systematically decreases from $x = 0.05$ toward $x = 0.45$. This tracks the evolution of the $Ta_{1-x}Al_xN_y$ composition spreads. No AlN or other intermetallic compounds were observed. Fig. 2(b) shows the top view of the plot in a smaller 2θ range (30° to 40°). The (111) peak was observed systematically shifting toward higher 2θ values, which is consistent with the fact that the smaller lattice parameters of $Ta_{1-x}Al_xN_y$ are formed with the increasing Al ratio [(Ta) $r = 0.209$ nm, and (Al) $r = 0.182$ nm]. This suggests a solid solution of $Ta_{1-x}Al_xN_y$ throughout the range $0.05 \leq x \leq 0.50$.

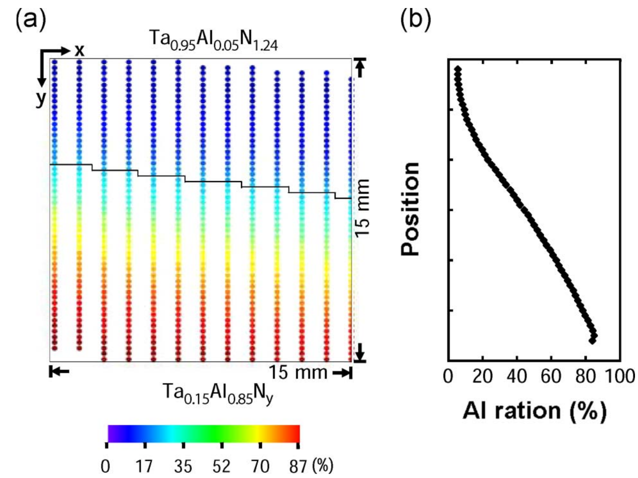

Fig. 1. Characterization of the compositions for the $Ta_{1-x}Al_xN_y$ library. (a) Composition map of the $Ta_{1-x}Al_xN_y$ composition spread, as determined by WDS. The dimension of the library is 15 mm × 15 mm. Each dot represents a MOSCAP. (b) Plot of the compositional variation across the sample. Each point was derived by averaging the compositions along isocompositional stepwise rows. A wide range of average compositions $x = 0.05$ to 0.85 was achieved.

A side view of a typical $Ta_{1-x}Al_xN_y/HfO_2/SiO_2$ capacitor structure is shown in Fig. 3(a). These metal–oxide–semiconductor capacitors (MOSCAPS) were directly formed by deposition of the $Ta_{1-x}Al_xN_y$ library film on top of the wafer through a stainless steel shadow mask with hundreds of nominal 150-μm-diameter openings. We have measured the diameters of 50 MOSCAPS at random across a typical library and found the average diameter to be 146.7 μm with a standard deviation of 1.9 μm. The configuration of the mask is shown in Fig. 3(b). After the deposition of the metal gate libraries, they were given a forming gas anneal [(FGA), 90% N_2/10% H_2] at 500 °C for 30 min. C–V curves were measured at 1 kHz to avoid series resistance. An inductance–capacitance–resistance (LCR) meter with a parallel resistance–capacitance circuit mode was used to measure capacitance with the modulation signal level set at 50 mV. The C–V curves were automatically measured on more than 2000 MOSCAPS on the four library samples. A standard program [20] was used to fit the measured C–V curves, from which equivalent oxide thickness (EOT) and flatband voltage (V_{fb}) were extracted. Φ_m was extracted by extrapolating V_{fb} as a function of EOT. After analyzing the C–V data of the FGA library samples, they were given rapid thermal anneals (RTAs) at 900 °C, 950 °C, and 1000 °C for 5 s. The C–V curves were again measured after each of these anneals to assess the thermal stability of the $Ta_{1-x}Al_xN_y/HfO_2/SiO_2$ gate stacks.

EOT, readily extracted from the C–V analysis, offers a snapshot of gate stack thermal stability. Fig. 4 shows the typical EOT maps, in this case, for the $Ta_{1-x}Al_xN_y/HfO_2(3\ nm)/SiO_2$ (6 nm) gate stack after FGA, 900 °C, 950 °C, and 1000 °C

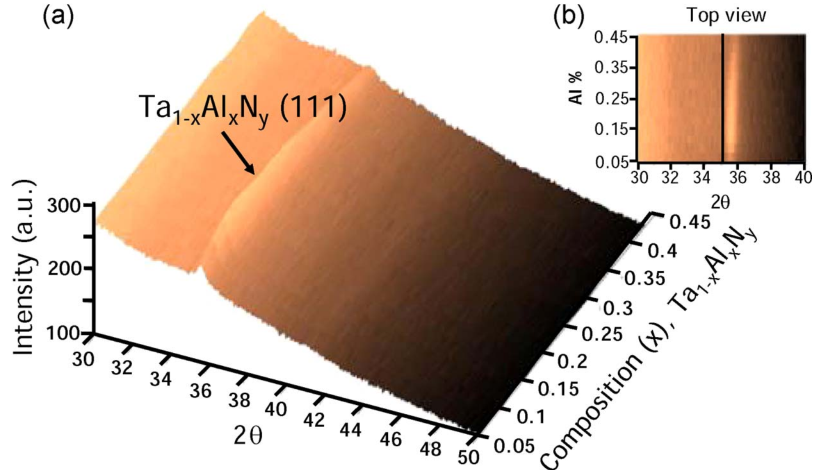

Fig. 2. Characterization of the structures of the $Ta_{1-x}Al_xN_y$ library. (a) Three-dimensional plot of the $Ta_{1-x}Al_xN_y$ composition spread, as determined by the scanning X-ray microdiffraction. (b) Top view of the plot from $2\theta = 30^\circ$ to $2\theta = 40^\circ$.

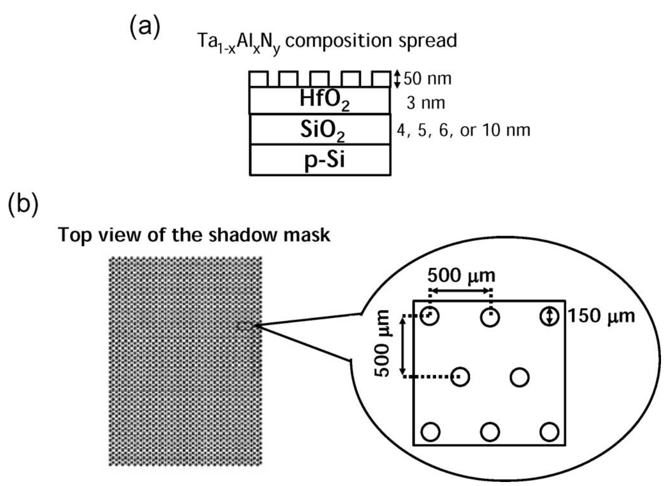

Fig. 3. Schematic drawing of the design of the library. (a) Side view of a typical $Ta_{1-x}Al_xN_y/HfO_2/SiO_2$ gate stack (not to scale). (b) Layout of the shadow mask.

RTAs. Only the data for metal gates with $x \leq 0.5$ are shown; higher Al contents show decreasing conductivity, since AlN is a wide bandgap semiconductor. The missing dots are indicative of capacitors that failed (i.e., these devices did not exhibit well-behaved C–V characteristics and could not be automatically fitted) as a result of the thermal treatment. As can be seen in the figure, more MOSCAPS degrade with increasing anneal temperature for gates with $x < 0.35$; very few failures are seen for higher Al content gates $(x > 0.35)$. Generally, the average EOT is as predicted from the $HfO_2(3\ \text{nm})/SiO_2$ (6 nm) stack (EOT $\cong$ 6.7 nm) for anneals up to 950 °C, except for the values close to the Al-rich end, where the EOT deviations (about 0.5 nm) might be due to increased series resistance due to the decreased conductivity of $Ta_{1-x}Al_xN_y$ alloys with high Al content. Such agreement is a qualitative indication of the thermal stability of the gate stack, i.e., that no extensive reaction has occurred between the gate metal electrode and HfO_2. However, deviations from the expected EOT value were observed after the 1000 °C anneal. Hafnium silicate might be formed over the whole discussed composition range, particularly for $x \leq 0.25$ (note the yellow and orange points). Higher EOTs are observed, which is an indicative of the formation of a lower dielectric constant material (HfSiO) in the HfO_2 layer [21]–[23]. For $0.3 \leq x \leq 0.5$, more Al atoms might diffuse into HfO_2, thus forming higher k dielectrics (hafnium aluminate) which lower EOTs (note the dark blue points). This has been observed by others [24].

Leakage current density (J_L) is also a measure of thermal stability of the gate stacks. Statistically reliable J_L values were obtained by averaging ten consecutive measurements at an applied dc gate bias of 1 V on hundreds of MOSCAPS. The J_L map is shown in Fig. 5. We found that J_L varied between 10^{-9} to 10^{-10} A/cm^2 for our thinnest gate stack $[HfO_2(3\ \text{nm})/SiO_2(4\ \text{nm})/Si]$ even after the 1000 °C anneal. These low leakages are consistent with a 4.6 EOT gate stack that was subjected to a high thermal budget [25].

Fig. 6 shows a plot of V_{fb} as a function of Al content for the four different gate stacks $Ta_{1-x}Al_xN_y/HfO_2(3\ \text{nm})/SiO_2$ (4, 5, 6, or 10 nm) after FGA. A systematic decrease of V_{fb} with increasing Al content is observed for the four gate stacks, which implies a decrease of Φ_m. This will be discussed later. All four curves in Fig. 6 show the same decreasing trend of V_{fb} with Al concentration. This can be attributed to the fact that the same $Ta_{1-x}Al_xN_y/HfO_2/SiO_2$ interface exists for each samples. A $\approx$50 mV deviation is observed for the thinnest SiO_2 underlayer, most probably due to more HfO_2 defects formed on the thinner SiO_2 buffer layer, to cause more fixed oxide charge $(\approx 2 \times 10^{11}/\text{cm}^2)$, which shifts V_{fb} to a more negative value. The inset in Fig. 6 is an example of how V_{fb} can change with annealing, in this case, for the $Ta_{1-x}Al_xN_y/HfO_2(3\ \text{nm})/SiO_2$ (6 nm) gate stack. V_{fb} is seen to change dramatically with annealing, indicating a change in Φ_m. For the 1000 °C RTA, the data for $x \leq 0.3$ are missing because most of the devices failed.

The Φ_m of the metal gate electrode is one of the most important CMOS transistor design parameters. We can extract Φ_m from an extrapolation of V_{fb} versus EOT [26]

$$V_{\text{fb}} = \left(\frac{\Phi_m - \Phi_s}{q}\right) - \frac{\rho_1}{\varepsilon_{\text{ox}}}\text{EOT}_1^2 - \frac{Q_1}{\varepsilon_{\text{ox}}}\text{EOT}_1 - \frac{Q_2}{\varepsilon_{\text{ox}}}\text{EOT} \qquad (1)$$

where Φ_m and Φ_s are the work functions of the metal gate electrode and Si; q is the electronic charge; ρ_1 is the bulk charge in HfO_2; EOT_1 is the EOT of the HfO_2 layer; ε_{ox} is the static

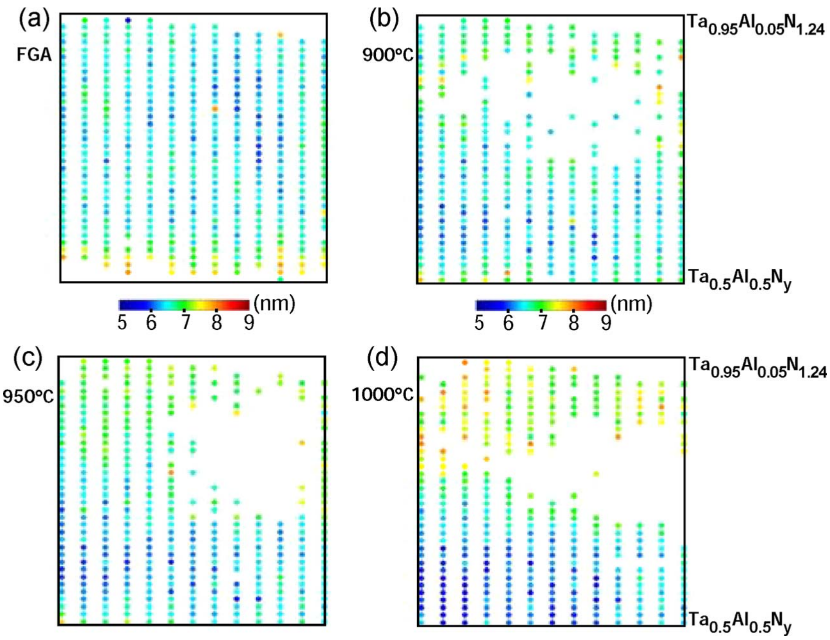

Fig. 4. Maps of the extracted EOT for the $Ta_{1-x}Al_xN_y/HfO_2(3\ \mathrm{nm})/SiO_2$ (6 nm) gate stack. The maps under different thermal budgets are shown. (a) FGA. (b) 900 °C. (c) 950 °C. (d) 1000 °C. The missing points are bad devices. The nominal EOT is ≈6.7 nm. Only compositions with $x = 0.05$ to 0.5 in the $Ta_{1-x}Al_xN_y$ composition spread are shown.

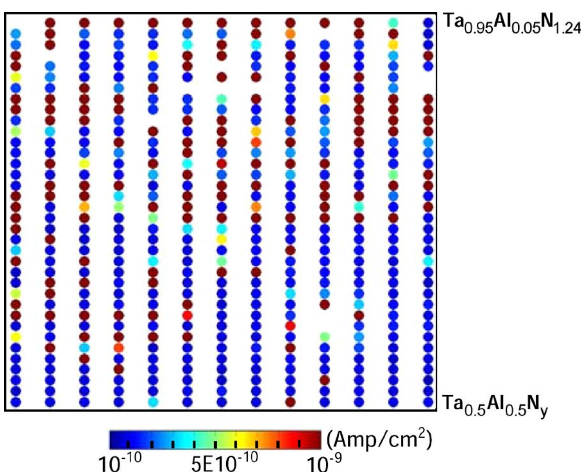

Fig. 5. Map of the leakage current density (J_L) measured at an applied dc gate bias of 1 V for the $Ta_{1-x}Al_xN_y/HfO_2(3\ \mathrm{nm})/SiO_2$ (4 nm) gate stack.

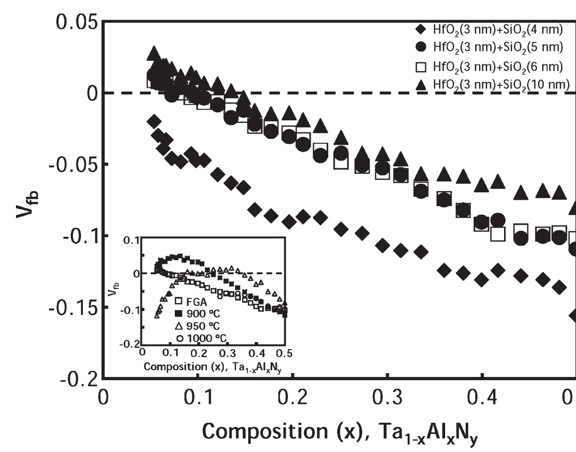

Fig. 6. Plot of the extracted flatband voltage (V_{fb}) for the $Ta_{1-x}Al_xN_y$ composition spreads. V_{fb} was observed systematically decreasing with increasing Al ratio for the four $HfO_2(3\ \mathrm{nm})/SiO_2$ (4, 5, 6, or 10 nm) gate stacks after FGA. The inset is an example of how V_{fb} can change with annealing (FGA, 900 °C, 950 °C, and 1000 °C), in this case, for the $Ta_{1-x}Al_xN_y/HfO_2(3\ \mathrm{nm})/SiO_2$ (6 nm) gate stack.

dielectric constant of SiO_2; Q_1 and Q_2 are the fixed oxide charges at the HfO_2/SiO_2 and SiO_2/Si interfaces, respectively; and EOT is the total EOT (SiO_2 plus HfO_2). The intercept of the extrapolation of (1) I is equal to

$$\left(\frac{\Phi_m - \Phi_s}{q}\right) - \frac{\rho_1}{\varepsilon_{\mathrm{ox}}}\mathrm{EOT}_1^2 - \frac{Q_1}{\varepsilon_{\mathrm{ox}}}\mathrm{EOT}_1. \qquad (2)$$

For negligible reactions in the gate stacks such as FGA and after 900 °C, this can be reduced to

$$\Phi_m = q^* I + \Phi_s \qquad (3)$$

since it can be assumed that ρ_1 and Q_1 are small. I and Φ_s are known quantities; thus, Φ_m can be readily determined. For extensive reactions in the gate stacks such as after 950 °C or higher, interactions have occurred at the various gate stack interfaces and that ρ_1 and Q_1 are no longer insignificant. Thus

$$\Phi_m = q^*\left(I + \frac{\rho_1}{\varepsilon_{\mathrm{ox}}}\mathrm{EOT}_1^2 + \frac{Q_1}{\varepsilon_{\mathrm{ox}}}\mathrm{EOT}_1\right) + \Phi_s. \qquad (4)$$

In Fig. 7, for the FGA data, Φ_m is derived through (3). One can observe that Φ_m systematically decreases with increasing incorporation of Al, which is consistent with the empirical relationship between Pauling electronegativity and the effective Φ_m, which states that elements with smaller electronegativities tend to lower Φ_m [27]. The geometric mean electronegativities for TaN and Al are 2.14 and 1.61, respectively. The Φ_m values decrease from ≈4.9 eV$(x = 0.05)$ to ≈4.75 eV$(x = 0.5)$, which are higher than the few values reported in the literature

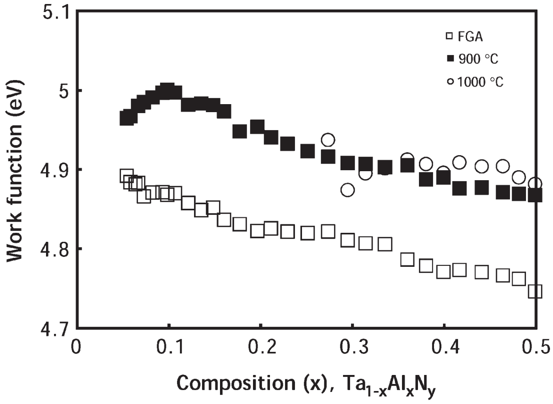

Fig. 7. Plot of the extracted work functions (Φ_m) for the $Ta_{1-x}Al_xN_y$ composition spreads. Φ_m was extracted after FGA, 900 °C, and 1000 °C as a function of Al content. Φ_m with $x < 0.3$ after 1000 °C could not be mapped due to the degradation of the capacitor characteristics.

[14], possibly for the following reasons: 1) in the present case, no capping layers were deposited on top of the $Ta_{1-x}Al_xN_y$ composition spread to minimize oxidation. Oxidation may cause the electronegative O atoms to form negative dipoles in the interfaces of $Ta_{1-x}Al_xN_y/HfO_2$, thereby increasing Φ_m [28], [29]; 2) the N/Ta ratio ($\approx$1.24) is significantly higher than the literature values. It has been reported that higher N ratio in metal nitrides can result in higher Φ_m [30].

After 900 °C RTA, ρ_1 and Q_1 might be still small, as discussed earlier. The extracted Φ_m shows a systematic increase in the FGA value of Φ_m ($\approx$0.1 eV) over most of the composition range, due to further oxidation of the $Ta_{1-x}Al_xN_y$ metal gates. This suggests similar amount of interfacial negative dipoles created in the interfaces of $Ta_{1-x}Al_xN_y/HfO_2$. Compared with the $Ta_{0.67}Al_{0.33}N/SiO_2/Si$ gate stack in the literature [31], we find our value, with the same Al content, to be $\approx$0.12 eV lower. This might be due to a different degree of Fermi level pinning for HfO_2/SiO_2 dielectrics [32], as compared to SiO_2. In general, the 900 °C Φ_m values show an almost parallel decreasing trend with Al content as the FGA case, except for Al values of ≤ 0.1. Φ_m peaks and then decreases. A similar peaking trend was also observed by Alshareef *et al.* [14]. A possible mechanism might involve the relatively easier oxidation tendency and interdiffusion of Al atoms to result in nonnegligible oxide charge at this composition range. When a small amount of Al ($x \leq 0.1$) is incorporated into the TaN matrix, octahedral Al sites with a charge of +3 are favored after 900 °C anneal. The interaction between Al^{3+} and the HfO_2 native defects (such as oxygen vacancies) causes the formation of positively charged oxygen vacancies, resulting in more positive fixed oxide charge [33], [34] and decreasing Φ_m for $x \leq 0.1$. After 1000 °C RTA, significant ρ_1 and Q_1 were created, and the degradation of the electrical properties was observed for the Ta-rich ($x < 0.3$) MOSCAPS, which resulted in an inability to systematically extract Φ_m in this range. For $x \geq 0.3$, however, the MOSCAPS still showed robust electrical characteristics, and the corresponding relative Φ_m [derived through (4)] could be extracted. As can be seen in Fig. 7, no significant differences were found compared to the 900 °C RTA. This might be a result of cancellation of different polarities of ρ_1 and Q_1.

Although ρ_1 and Q_1 were not measured directly, one can still qualitatively estimate their effect on Φ_m through the V_{fb} shift. From the previous arguments, we assume that the bulk and fixed oxide charges are almost negligible after 900 °C. Therefore, we can subtract the V_{fb} values of $Ta_{1-x}Al_xN_y$ metal gates after 900 °C from those after the 1000 °C RTA. The values almost result from the net effect of the bulk and fixed oxide charges in the HfO_2 and HfO_2/SiO_2 interfaces, respectively, assuming that the amount of interfacial dipoles are the same for 900 °C and 1000 °C RTAs. Finally, although the quantity Q_2 does not contribute to Φ_m directly, it is still a valuable parameter to look at, since one can gain insight into film quality. Our libraries exhibit a value of $Q_2 \cong 10^{12}/cm^2$ for all the compositions after FGA. After the 900 °C anneal, more defects were removed in the SiO_2/Si interfaces, and Q_2 was reduced by one order of magnitude, which is comparable with the literature values [14].

IV. Conclusion

We have demonstrated the efficiency of combinatorial methodology applied to $Ta_{1-x}Al_xN_y$ alloys as metal gates on HfO_2 for CMOS applications. To the best of our knowledge, this is the first time that combinatorial methodology has been applied to systematically extract Φ_m for the CMOS advanced gate stack. $Ta_{1-x}Al_xN_y/HfO_2(3\ nm)/SiO_2$ (4, 5, 6, or 10 nm) capacitor libraries were fabricated by reactive sputtering $Ta_{1-x}Al_xN_y$ onto HfO_2 through a shadow mask. A standard program was used to fit C–V characteristics on over 2000 MOSCAPS to extract EOT and V_{fb}. The EOT maps indicate that only limited interaction between the gate stack layers took place below 950 °C RTA. The Φ_m of the $Ta_{1-x}Al_xN_y$ libraries was systematically mapped over a wide $(0.05 \leq x \leq 0.50)$ composition range, after forming gas, and 900 °C RTA. After 1000 °C RTA, only Φ_m with compositions $(0.30 \leq x \leq 0.50)$ could be extracted because of the MOSCAP failures, due to the high anneal temperature. Our results show that Φ_m can be tuned as a function of gate metal composition, as well as annealing condition. The fixed oxide charges in the SiO_2/Si interfaces show reasonably small values after 900 °C anneal. We suggest that $Ta_{0.9}Al_{0.1}N_{1.24}$ is potential to replace polysilicon for PMOS applications.

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References

[1] *International Technology Roadmap for Semiconductors*, 2005. [Online]. Available: http://public.itrs.net
[2] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, no. 10, pp. 5243–5275, May 2001.
[3] P. A. Packan, "DEVICE PHYSICS: Pushing the limits," *Science*, vol. 285, no. 5436, pp. 2079–2081, Sep. 1999.
[4] H.-S. P. Wong, "Beyond the conventional transistor," *IBM J. Res. Develop.*, vol. 46, no. 2/3, pp. 133–168, Mar.–May 2002.
[5] C. B. Samantaray and Z. Chen, "Reduction of gate leakage current of HfSiON dielectrics through enhanced phonon-energy coupling," *Appl. Phys. Lett.*, vol. 89, no. 16, pp. 162 903–162 905, Oct. 2006.
[6] M.-H. Cho, K. B. Chung, and D.-W. Moon, "Electronic structure and thermal stability of nitrided Hf silicate films using a direct N plasma," *Appl. Phys. Lett.*, vol. 89, no. 18, pp. 182 908–182 910, Oct. 2006.
[7] "International Technology Roadmap for Semiconductors (ITRS) 2007 Edition," *The Front End Processes*, pp. 21–26.

[8] Y.-S. Suh, G. P. Heuss, J.-H. Lee, and V. Misra, "Effect of the composition on the electrical properties of $TaSi_xN_y$ metal gate electrodes," *IEEE Electron Device Lett.*, vol. 24, no. 7, pp. 439–441, Jul. 2003.

[9] C. Ren, D. S. H. Chan, X. P. Wang, B. B. Faizhal, M.-F. Li, Y.-C. Yeo, A. D. Trigg, A. Agarwal, N. Balasubramanian, J. S. Pan, P. C. Lim, A. C. H. Huan, and D.-L. Kwong, "Physical and electrical properties of lanthanide-incorporated tantalum nitride for n-channel metal–oxide–semiconductor field-effect transistors," *App. Phys. Lett.*, vol. 87, no. 7, pp. 073 506–073 508, Aug. 2005.

[10] C.-L. Cheng, K.-S. Chang-Liao, T.-C. Wang, T.-K. Wang, and H. C.-H. Wang, "$Hf_xTa_yN_z$ metal gate electrodes for advanced MOS devices applications," in *Proc. Int. Symp. VLSI Technol., Syst., Appl.*, Hsinchu, Taiwan, R.O.C., pp. 1–2.

[11] W. P. Bai, S. H. Bae, H. C. Wen, S. Mathew, L. K. Bera, N. Balasubramanian, N. Yamada, M. F. Li, and D.-L. Kwong, "Three-layer laminated metal gate electrodes with tunable work functions for CMOS applications," *IEEE Electron Device Lett.*, vol. 26, no. 4, pp. 231–233, Apr. 2005.

[12] K. Choi, H. N. Alshareef, H. C. Wen, H. Harris, H. Luan, Y. Senzaki, P. Lysaght, P. Majhi, and B. H. Lee, "Effective work function modification of atomic-layer-deposited-TaN film by capping layer," *Appl. Phys. Lett.*, vol. 89, no. 3, pp. 032 113–032 115, Jul. 2006.

[13] C. S. Park, B. J. Cho, and D.-L. Kwong, "An integratable dual metal gate CMOS process using an ultrathin aluminum nitride buffer layer," *IEEE Electron Device Lett.*, vol. 24, no. 5, pp. 298–300, May 2003.

[14] N. Alshareef, K. Choi, H. C. Wen, H. Luan, H. Harris, Y. Senzaki, P. Majhi, B. H. Lee, R. Jammy, S. Aguirre-Tostado, B. E. Gnade, and R. M. Wallace, "Composition dependence of the work function of $Ta_{1-x}Al_xN_y$ metal gates," *Appl. Phys. Lett.*, vol. 88, no. 7, pp. 072 108–072 110, Feb. 2006.

[15] X.-D. Xiang and P. G. Schultz, "The combinatorial synthesis and evaluation of functional materials," *Physica C*, vol. 282–287, pp. 428–430, 1997.

[16] X.-D. Xiang, X. Sun, G. Briceno, Y. Lou, K.-A. Wang, H. Chang, W. G. Wallace-Freedman, S.-W. Chen, and P. G. Schultz, "A combinatorial approach to materials discovery," *Science*, vol. 268, no. 5218, pp. 1738–1740, Jun. 1995.

[17] K.-S. Chang, M. Green, J. Suehle, E. Vogel, H. Xiong, J. Hattric-Simpers, I. Takeuchi, O. Famodu, K. Ohmori, P. Ahmet, T. Chikyow, P. Majhi, B.-H. Lee, and M. Gardner, "Combinatorial study of Ni–Ti–Pt ternary metal gate electrodes on HfO_2 for the advanced gate stack," *Appl. Phys. Lett.*, vol. 89, no. 14, pp. 142 108–142 111, Oct. 2006.

[18] K.-S. Chang, M. Aronova, O. O. Famodu, I. Takeuchi, S. E. Lofland, J. Hattrick-Simpers, and H. Chang, "Multimode quantitative scanning microwave microscopy of *in situ* grown epitaxial $Ba_{1-x}Sr_xTiO_3$ composition spreads," *Appl. Phys. Lett.*, vol. 79, no. 26, pp. 4411–4413, Dec. 2001.

[19] M. L. Green, K.-S. Chang, S. De Gendt, T. Schram, and J. Hattrick-Simpers, "Application of combinatorial methodologies for work function engineering of metal gate/high-k advanced gate stacks," *Microelectron. Eng.*, vol. 84, no. 9/10, pp. 2209–2212, Sep./Oct. 2007.

[20] J. R. Hauser and K. Ahmed, "Characterization of ultra-thin oxides using electrical C–V and I–V measurements," in *Proc. Int. Conf. Characterization Metrol. ULSI Technol.*, 1998, pp. 235–239.

[21] M. Gutowski, J. E. Jaffe, C.-L. Liu, M. Stoker, R. I. Hegde, R. S. Rai, and P. J. Tobin, "Thermodynamic stability of high-K dielectric metal oxides ZrO_2 and HfO_2 in contact with Si and SiO_2," *Appl. Phys. Lett.*, vol. 80, no. 11, pp. 1897–1899, Mar. 2002.

[22] Y. Xu and C. B. Musgrave, "Atomic layer deposition of high-k dielectrics on nitrided silicon surfaces," *Appl. Phys. Lett.*, vol. 86, no. 19, pp. 192 110–192 112, May 2005.

[23] C. S. Lai, W. C. Wu, T. S. Chao, J. H. Chen, J. C. Wang, L.-L. Tay, and N. Rowell, "Suppression of interfacial reaction for HfO_2 on silicon by pre-CF_4 plasma treatment," *Appl. Phys. Lett.*, vol. 89, no. 7, pp. 72 904–72 906, Aug. 2006.

[24] P. K. Park and S.-W. Kang, "Enhancement of dielectric constant in HfO_2 thin films by the addition of Al_2O_3," *Appl. Phys. Lett.*, vol. 89, no. 19, pp. 192 905–192 907, Nov. 2006.

[25] M. Depas, B. Vermeire, P. W. Mertens, M. Meuris, and M. M. Heyns, "Wear-out of ultra-thin gate oxides during high-field electron tunnelling," *Semicond. Sci. Technol.*, vol. 10, no. 6, pp. 753–758, Jun. 1995.

[26] J. K. Schaeffer, C. Capasso, R. Gregory, D. Gilmer, L. R. C. Fonseca, M. Raymond, C. Happ, M. Kottke, S. B. Samavedam, P. J. Tobin, and B. E. White, Jr., "Tantalum carbonitride electrodes and the impact of interface chemistry on device characteristics," *J. Appl. Phys.*, vol. 101, no. 1, pp. 014 503–014 509, Jan. 2007.

[27] J. K. Schaeffer, D. C. Gilmer, C. Capasso, S. Kalpat, B. Taylor, M. V. Raymond, D. Triyoso, R. Hegde, S. B. Samavedam, and B. E. White, Jr., "Application of group electronegativity concepts to the effective work functions of metal gate electrodes on high-k gate oxides," *Microelectron. Eng.*, vol. 84, no. 9/10, pp. 2196–2200, Sep./Oct. 2007.

[28] T. C. Leung, C. L. Kao, and W. S. Su, "Relationship between surface dipole, work function and charge transfer: Some exceptions to an established rule," *Phys. Rev. B, Condens. Matter*, vol. 68, no. 19, pp. 195 408–195 413, Nov. 2003.

[29] C.-L. Cheng, C.-W. Liu, and J.-T. Jeng, "Work function tuning of the Ti_xTa_yN metal gate electrode for advanced metal–oxide–semiconductor devices applications," *Appl. Phys. Lett.*, vol. 90, no. 6, pp. 062 114–062 116, Feb. 2007.

[30] P. Majhi, H.-C. Wen, K. Choi, H. Alshareef, C. Huffman, and B. H. Lee, "A systematic study of the influence of nitrogen in tuning the effective work function of nitrided metal gates," in *Proc. IEEE VLSI-TSA*, 2005, pp. 105–106.

[31] B. Chen, R. Jha, and V. Misra, "Work function tuning via interface dipole by ultrathin reaction layers using AlTa and AlTaN alloys," *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 731–733, Sep. 2006.

[32] H. Y. Yu, C. Ren, Y.-C. Yeo, J. K. Kang, X. P. Wang, H. H. H. Ma, M.-F. Li, D. S. H. Chan, and D.-L. Kwong, "Fermi pinning-induced thermal instability of metal-gate work functions," *IEEE Electron. Device Lett.*, vol. 25, no. 5, pp. 337–339, May 2004.

[33] R. S. Johnson, G. Lucovsky, and I. Baumvol, "Physical and electrical properties of noncrystalline Al_2O_3 prepared by remote plasma enhanced chemical vapor deposition," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 19, no. 4, pp. 1353–1360, Jul. 2001.

[34] M. Haverty, A. Kawamoto, K. Cho, and R. Dutton, "First-principles study of transition-metal aluminates as high-k gate dielectrics," *Appl. Phys. Lett.*, vol. 80, no. 15, pp. 2669–2671, Apr. 2002.

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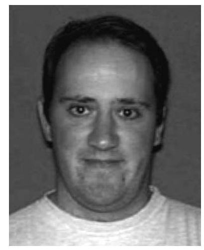

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