Lack of charge offset drift is a robust property of Si single electron transistors

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One of the challenges that single-electron transistors (SETs) face before they can be considered technologically useful is the charge offset drift. Recently, two different types of Si SETs were shown to have a drift of only $0.01e$ (the fundamental charge) over several days. Those devices came from one fabrication source. Here, we present the results for Si SETs fabricated by our group (a different source) demonstrating their operation as SETs. We confirm that the charge offset drift is less than $0.01e$, demonstrating the lack of charge offset drift is generic to Si devices and not dependent on the fabrication source. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2841659]

Single electron transistors (SETs) have attracted attention in the past 20 years.[1] Their ability to manipulate individual electrons makes them very attractive for metrology applications using the charge of the electron.[2] More recently, efforts in quantum computing using charge qubits require SETs for their detection scheme.[3] Also, SETs have attracted attention as possible alternatives to classical computing.[4]

One of the main issues with SET devices is the charge offset drift $Q_0(t)$. The charge offset drift is the random phase change of the periodic characteristic curve of the device as a function of time.[5] This behavior arises from the long term relaxation of charges around the device. This problem makes it virtually impossible to predict the initial state of the device before each operation. Thus, running multiple SET devices in parallel could be a daunting task. The phenomenon of a large $Q_0(t)$ is very well demonstrated in metal devices.[5]

Recently, we have demonstrated[6,7] that silicon (Si) based SET devices are almost free of the problem of the charge offset drift. This is true for both fixed-barrier[6] devices as well as for tunable-barrier ones.[7] We believe that the tunable barrier Si based SET devices are the most promising for any application. They combine (i) compatibility with the current metal oxide semiconductor field effect transistor (MOSFET) technology, with (ii) more controllable fabrication, and (iii) a large flexibility of operation.[8] These characteristics, combined with the very small $Q_0(t)$, make them very appealing. All of the devices previously measured[6,7] were fabricated at the same foundry, denoted by foundry A.[9] We can pose the question, is the very small $Q_0(t)$ an intrinsic property of Si devices, or merely a consequence of the specific foundry?

In this letter, we present results from Si-based tunable-barrier SETs fabricated by our group in foundry B.[9] These devices function as standard SETs. We also demonstrate that, in fact, $Q_0(t)$ in these devices is orders of magnitude smaller than in the metal devices and comparable to that measured for the previously mentioned Si SET devices, thus answering the question posed above; the small $Q_0(t)$ is an intrinsic property of Si devices.

The devices presented here were fabricated using conventional MOSFET processes and electron beam lithography. A schematic representation of the device appears in Figs. 1(a) (lateral) and 1(b) (vertical). A micrograph of a device, similar to the one used but without the upper gate, appears in Fig. 1(c). We start with a silicon on insulator (SOI) substrate and etch a narrow channel, lightly *p*-doped, between heavily *n*-doped source and drain regions. Then, a layer of oxide is grown on top and a layer of localized *in situ* doped polysilicon is deposited. Localized gates, the "lower" gates, are defined through electron beam lithography and etching of the polysilicon, followed by another layer of oxide. Finally, an upper polysilicon gate is deposited and is defined to cover the entire region between source and drain. The upper gate can be used to invert the channel and thus turn on conduction of the device. The lower gates control the conductance of the channel, in the regions below them. By locally turning off conduction, they can be used to create local barriers.

In the following, we present results from a single device (JW2.4-23 EL). We confirmed these results with device JW1.7-24 EL. We have used the upper gate to turn the channel on, and one of the lower gates (LGD) to create a constant barrier. We ramp the voltage of a second lower gate (V_{LGS}), which allows us to form a second barrier, and also to control the potential of the island in between the barriers, through

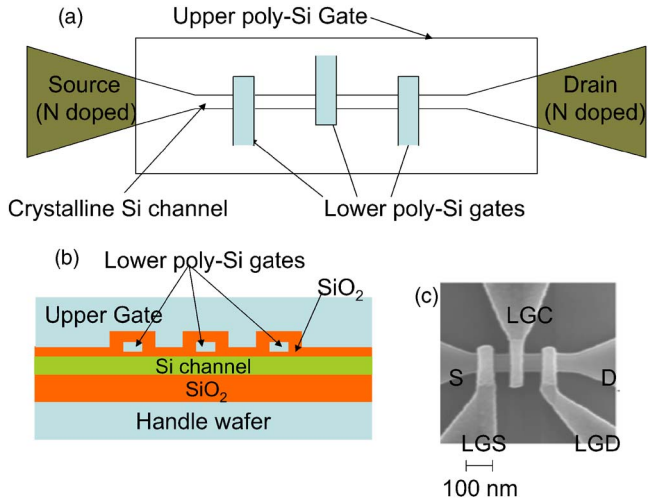

FIG. 1. (Color online) (a) Lateral and (b) vertical schematics of our device. (c) A micrograph of a device with no upper gate.

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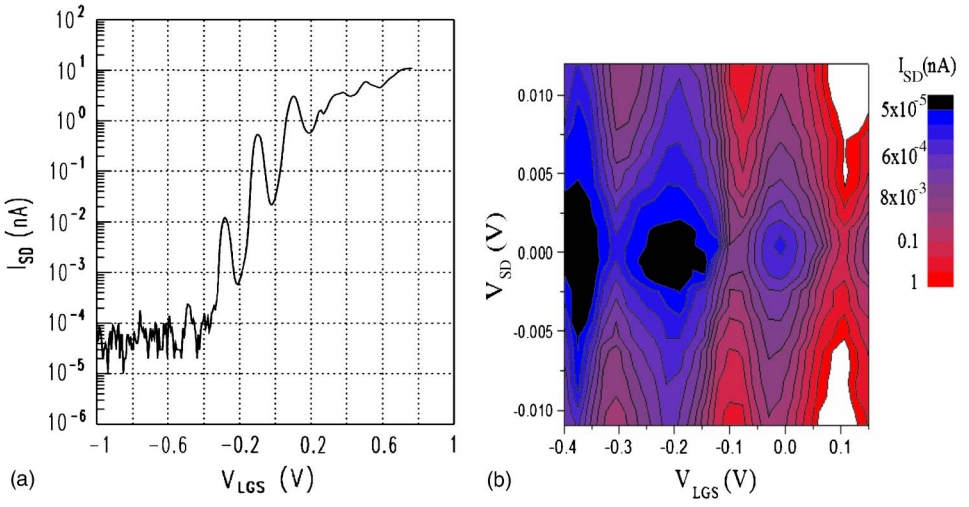

FIG. 2. (Color online) (a) Current through the device (I_{SD}) vs gate voltage (V_{LGS}). Coulomb blockade oscillations are superimposed on the FET characteristic curve. (b) Coulomb blockade "diamonds" are clearly seen in the contour plot of bias voltage (V_{SD}) vs V_{LGS} (the color scale represents I_{SD}).

cross capacitance. By doing so, we observe that the current through the device (I_{SD}) can be turned on and off as a periodic function of the gate voltage (Coulomb oscillations).[10] Figure 2(a) shows such oscillations in I_{SD} versus V_{LGS}. The voltages on the upper gate, lower gate closest to the drain and the bias voltage were $V_{UG}=3$ V, $V_{LGD}=-0.88$ V, and $V_{SD}=10$ mV, respectively. We have not used LGC ($V_{LGC}=0$) due to problems with leakage through this gate. The temperature was 4 K. It is clear that these oscillations are not perfectly periodic. We attribute that to the fact that there are unintentional barriers in the device. We have measured a number of devices fabricated during the same fabrication run as the device presented here and have found they sometimes suffer from leakage problems and unintentional barriers.

Despite the existence of unintentional barriers, though, the dominant source of the Coulomb blockade is a single island as can be seen from the contour plot of Fig. 2(b). These data show clear Coulomb blockade "diamonds."[10] Just as in Fig. 2(a), the value of I_{SD} increases rapidly with V_{LGS} because the values of V_{LGS} correspond to the subthreshold regime of the FET comprised of the gate LGS and the region of the channel directly below it. We believe that this single island is the region between the two barriers formed by LGS and LGD because the gate capacitances to the island C_{UG}, C_{LGS}, and C_{LGD} had the same value for both measured devices.[11]

The height of the diamond [Fig. 2(b)] can be used to calculate the total capacitance of the island ($C_{\Sigma 1}=e/V_{height}$, where e is the fundamental charge), and the slopes of the diamond give us the values of the barrier capacitances[10] (C_S and C_D). In addition, the gate capacitances (C_{UG}, C_{LGS}, and C_{LGD}) can be calculated from the period of the Coulomb blockade oscillations. The height of the diamond at $V_{LGS}=0$ V is 3.5 mV which gives us $C_{\Sigma 1}=46$ aF. We chose this value for the height based on the constant current curve of $I_{SD}\approx 0.002$ nA since it is the lowest value for which we get a clear diamond shape. The addition of the barrier capacitances and the gate capacitances give us $C_{\Sigma 2}=C_S+C_D+C_{UG}+C_{LGS}+C_{LGD}$. We measured $C_S=17$ aF and $C_D=27$ aF (from the slopes), $C_{UG}=1$ aF and $C_{LGS}=1$ aF (from the periods), thus obtaining $C_{\Sigma 2}>46$ aF. We use the inequality because we did not observe any oscillations due to LGD, used as the fixed barrier, so we did not add the contribution of C_{LGD} to the total capacitance of the island. Taking into account that $C_{LGS}=1$ aF and that for two other devices the capacitance of the lower gates to the island were all about 1 aF, we can infer that the true value of $C_{\Sigma 2}$ is not more than a few aF larger than 46 aF. The values of total capacitance, calculated using two different methods, agree, so we have confirmed that the effects we are seeing are due to a single dominant SET island. We note that the oscillations do not significantly die out for larger values of V_{SD}; this is common in devices where the properties of the barrier are controlled by the gate voltage.[12,13]

In Fig. 3, we present the results from measuring the Coulomb blockade oscillations as a function of temperature, at $V_{SD}=3$ mV, $V_{UG}=3$ V, and $V_{LGD}=-0.88$ V. From this, we can see that the oscillations persist to about 40 K. The inset in Fig. 3 shows the temperature dependence of I_{SDmax}/I_{SDmin}, as measured for the peak at $V_{LGS}=-0.1$ V and the valley at $V_{LGS}=0$ V. Fitting these data to[1] $I^*_{SDmax}/I^*_{SDmin}\propto e^{-e^2/2C_\Sigma k_B T}$, we obtain $C_\Sigma=40$ aF with an uncertainty of +10 aF, −15 aF, which agrees very well with the two values determined by the methods described before. The uncertainty in the calculated value comes from the uncertainty in the fitting of the data.

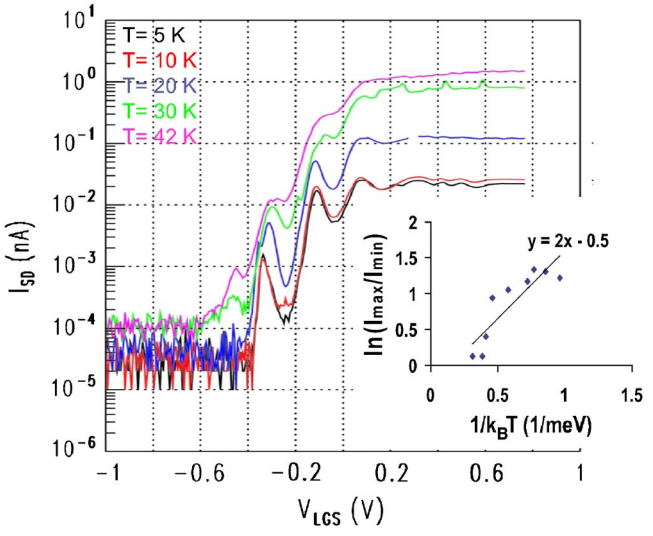

FIG. 3. (Color online) I_{SD} vs V_{LGS} for temperatures of 5, 10, 20, 30, and 42 K. The oscillations persist to about 40 K. Inset: $\ln(I_{SDmax}/I_{SDmin})$ vs $1/k_BT$, where k_B is Boltzmann's constant. The slope of the fitted line is used in determining C_Σ.

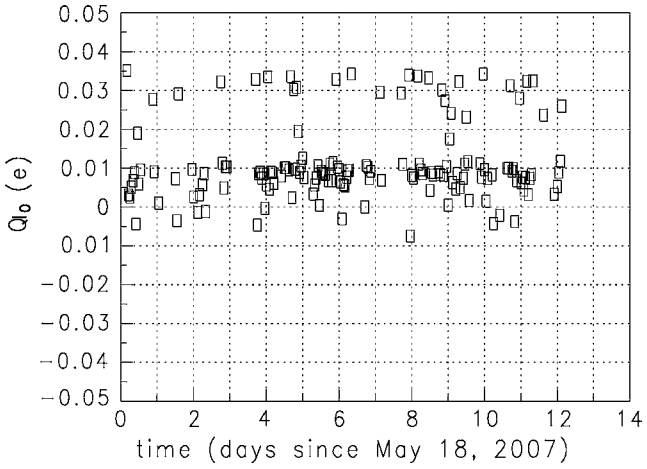

FIG. 4. Charge offset drift Q_0 vs time.

Having demonstrated that these devices operate as single electron transistors, we proceeded to measure the charge offset drift $[Q_0(t)]$. The method we used is as follows: we took I_{SD} versus V_{LGS} curves over a period of several days [similar to the ones in Fig. 2(a)]. We picked a specific peak (near $V_{LGS}=-0.1$ V) in I_{SD} and, by fitting a limited range of the data to a parabola, measured the gate voltage $V_{LGS}(t)$ corresponding to the center of the parabola. Then, we obtained $Q_0(t)=e[V_{LGS}(t)-V_{LGS}(t=0)]/\Delta V_{LGS}$, where ΔV_{LGS} is the value of voltage of an entire period, which corresponds to one extra electron on the gate and is independent of time. The results appear in Fig. 4, where data are shown from May 18 to 31, 2007, for which the total $Q_0(t)$ range is about $0.03e$, with a drift of less than $0.01e$. By range versus drift we specifically mean that, although the minimum and maximum values of the data range have a range of about $0.03e$, the mean or dominant value (at $Q_0=0.01e$) varies not at all over the entire 12 day period. This is in marked contrast to the behavior in metal devices,[5] which have not only a large range but also a large drift. During this period, there were several liquid He transfers to the cryostat which cause mechanical perturbations. There is also evidence of a two level fluctuator in our system, since most of the data appear to fluctuate between two main values ($Q_0=0.01e$ and $0.035e$) with the one at $0.01e$ being the most frequent. The temperature of the device was 1 K, while the rest of the parameters were the same as the ones for the measurements presented in Fig. 2(a).

These results show that the drift in $Q_0(t)$, for this type of device, is at least 100 times better than in metal devices, where it typically changes by at least $1e$ over a few days.[5] They also show that our devices have comparable behavior to the previously measured tunable barrier Si devices.[7] This is a striking result considering the fact that as was mentioned earlier, our devices suffer from a variety of fabrication problems which should have increased the value of Q_0 as compared to the results of Ref. 7. Finally, the robustness of this behavior is demonstrated by the fact that even under mechanical perturbation (liquid He transfers), the drift of $Q_0(t)$ remains orders of magnitude better than in metal devices.

In conclusion, we have demonstrated the operation of tunable barrier Si single electron transistors. We have shown that, despite the existence of unintentional barriers, the device is dominated by a single Coulomb island. We have also confirmed that the charge offset drift, $Q_0(t)$, in this type of device is orders of magnitude less than in metal ones. This has been shown in the past by devices originating from a single fabrication source, foundry A, and is confirmed by devices made at a different foundry B. The difference in $Q_0(t)$ between metal and Si devices can be attributed to the difference in the quality of their fabrication processes. The microelectronics industry has invested huge efforts in perfecting the quality of the fabrication techniques used for Si devices. In particular, the quality of the oxide used and the quality of the interface between the oxide and the Si have been extensively considered.[14] This has led to fabrication processes that produce more stable behavior than the ones used for any other material including metals, which, in our case, is demonstrated by the lower $Q_0(t)$.

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