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HIGH-DENSITY TEST STRUCTURES FOR ASSESSING MICROWAVE/MILLIMETER WAVE MONOLITHIC INTEGRATED CIRCUIT (MIMIC) PERFORMANCE

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Abstract

This paper discusses the unique, high-density implementation of microelectronic test structures used to diagnose and predict MIMIC performance under MIMIC Phase 1, Task 4.E. It also presents assessments and recommendations, based on Task 4.E data, for future test structure methods to evaluate MIMIC performance.

Motivation for Using Test Structures

Developing methods to provide and select affordable and reproducible MIMIC products is a major objective of the DARPA/Tri-Service MIMIC program. Understandably, such methods must be accurate, economical, and themselves reproducible. Such methods must also be applied to activities critical to product success. As demonstrated by Task 4.E[1] and its predecessor[2], critical activities that do exist in the semiconductor manufacturing process are to select materials, to diagnose and control processes, and to predict yield of devices.

A classic method for obtaining the characteristics of semiconductor materials, processes, and devices is to collect data from microelectronic test structures, which are fabricated on the same wafer, and at the same time, as the actual circuits being produced. By correlating and comparing these characteristics, manufacturers can develop criteria for providing and selecting materials, processes, and devices. By comparing characteristics between manufacturers, the Government can develop criteria for specifying and purchasing components and systems. For such comparisons and correlations to be meaningful, a common reference point for assessing MIMIC performance is needed.

To provide a common reference point, a standard test structure methodology is needed. Under Task 4.E, standard test structure design, implementation, measurement, and data reduction methods were specified. This paper presents the major conclusions of the NIST-WL effort to assess this methodology based on the electrical test data collected from wafers produced by the various Task 4.E processes. It also presents recommendations to improve and extend the utility of MIMIC test structure methods when they are applied to processes under development or modification or in production.

Motivation for Using High-Density Test Structures

In an effort unique to the GaAs and MIMIC communities, Task 4.E used a high-density test structure implementation[3,4]. This enabled significant statistical analysis, correlation, and comparison of material, process, and device performance. Sets of test wafers were produced by each manufacturer. Depending on the process, each wafer contained about 200 MIMIC standard test chips. Each test chip included FETs, parametric test structures, and manufacturer-specific Monolithic Microwave Integrated Circuits (MMICs), many of which were measured more than once, at different process steps.

The parametric test structures include the Transmission Line Model (TLM) and van der Pauw resistors, shown in Figure 1, as well as those contained in the MIMIC standard Process Control Monitor (PCM), which is shown in Figure 1 and detailed in Figure 2. In addition to test chip replications, each wafer included manufacturer-specific PCMs at five drop-in sites (at the middle and in each quadrant of the wafer), as is often done, independent of Task 4.E, when using test structures for process monitoring.

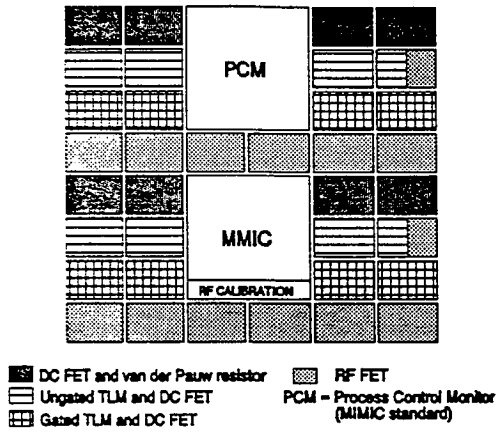

Figure 1. Block diagram of the MIMIC standard test chip

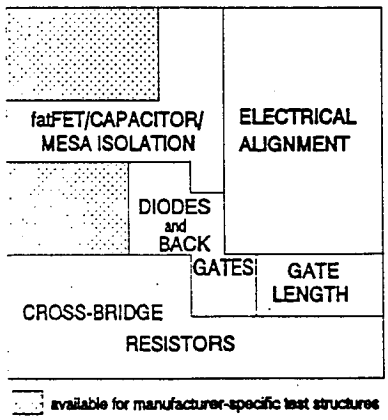

Figure 2. Block diagram of the MIMIC standard PCM

The utility of the high-density approach over a limited drop-in approach is demonstrated in the following example of FET data from the post-recess process step. Using the high-density approach, only 48.3% of the measured values for Ids (drain-to-source current) were within the desired range, as indicated by the black areas of the wafer map in Figure 3. Also, the percent standard deviation (%σ) is an unacceptable 28.1%. Note that all five drop-ins are within the black areas, indicating acceptable Ids values. This data set also has a much lower %σ of 10.7%. Had only the limited drop-in area data been considered, yield could have been considered adequate, rather than poor. The variability in the two data sets is further contrasted by the Figure 3 box plots. The range of the two quartiles of data (the bounds of the box) around the median (line inside box) is much larger for the full wafer data than the limited data.

This high density-data raised a process control concern not evident with limited data. Investigation revealed that in manual dip recess etching, if data from the drop-ins did not meet target values, additional partial dipping was done to "correct" the etch depth, introducing the non-uniformities. Such observations prompted some manufacturers to adopt automated spray etch processes, which improved uniformity and yield. For the process line of the Figure 3 data, this process modification resulted in the improvements shown

in Figure 4. The full wafer data yield increased to 83.1%, its %σ decreased to 8.0%, and the distribution and variability are similar for the full wafer and limited data sets. This indicates good process control for Ids. Now, data from the drop-in areas alone could be used to successfully predict yield.

Thus, for processes where contol has not been demonstrated, high-density data collected at intermediate process steps can help manufacturers to detect and fix yield limiting problems. In such cases, relying on limited drop-in data could cause manufacturers to continue to expend resources on non-productive processing.

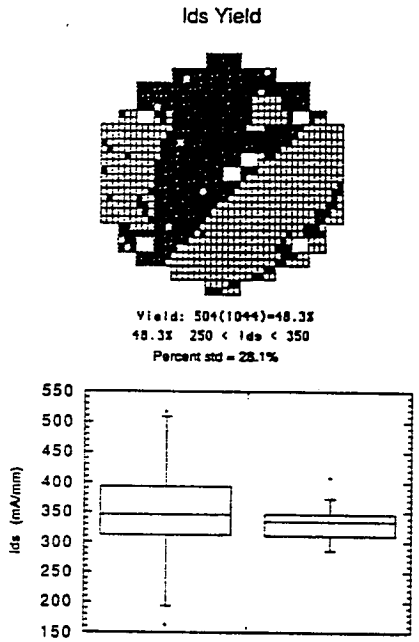

Figure 3. Post-recess Ids data from 200μm FETs: wafer map of yield (top) and box plot (bottom) showing upper-lower quartile variability for full wafer (left) vs limited (right) data

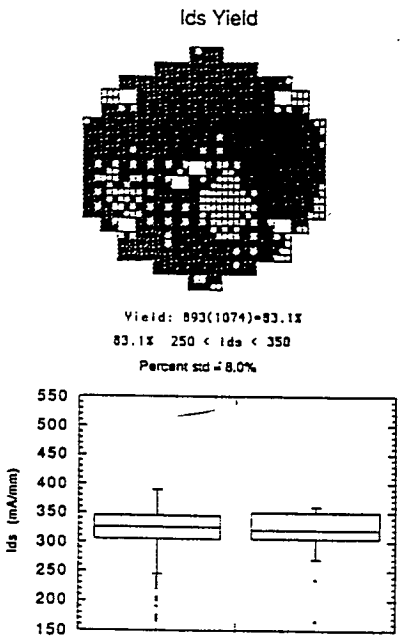

Figure 4. Post-recess Ids data from 200μm FETs in modified process: yield (top) and variability (bottom) for full wafer (left) vs limited (right) data

Test Structure Performance

Using high-density test structures played an important role in diagnosing processing problems on Task 4.E[1]. To further confirm this positive indication of generally satisfactory performance, a study of test structure data was made to assure the structures performed as intended[5]. The structures studied were the TLMs and van der Pauw resistors, as well as the MIMIC standard PCM test structures.

Most of the test structures performed at least adequately for most of the manufacturers. Successful performance for a given test structure was readily recognized by analysts using wafer maps, correlation plots, box plots, basic statistics, and knowledge of first principles and the process. An example follows showing how performance of the van der Pauw sheet resistor was determined to be successful, given that it measures the post-ohmic active layer sheet resistance, which is inversely related to the post-ohmic FET Ids. The post-ohmic active layer sheet resistance and the post-ohmic Ids data were uniform, with %σ's of 2.5% and 1.8%. Both data sets correlated as expected, as shown in Figure 5 by the similar patterns in the wafer maps and the straight line in the correlation plot. The sheet resistance measurements from the van der Pauw resistor can also be validated by comparison with measurements from the active layer cross-bridge sheet resistor, which is essentially equivalent but has a different layout. As seen in Figure 6, the box plot shows the distributions of these two data sets are nearly identical.

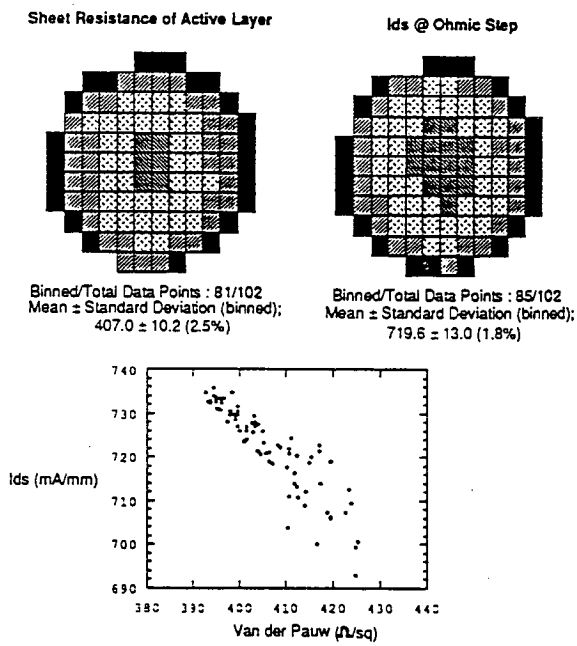

Figure 5. Correlation of 200μm FET Ids and van der Pauw sheet resistance by wafer map (top) and correlation plot (bottom)

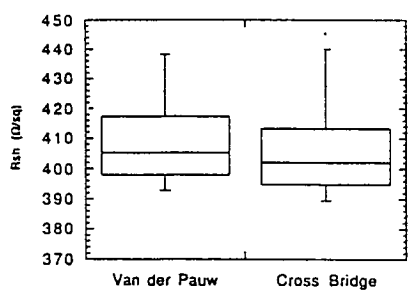

Figure 6. Active layer sheet resistance measurements from the van der Pauw resistor (left) are validated by measurements from the cross-bridge resistor (right)

More extensive analysis was needed for a few test structures. Investigations revealed problems related to measurement procedures and test conditions, a deficiency in test structure design, and process characteristics that precluded test structures from working as expected. Full analyses are documented elsewhere[5], but some brief illustrations of the results are given below.

The gated and ungated TLMs were intended to provide measurements that could be used to determine channel thickness and resistance values for use with doping profile models. This was to be done by measuring contact resistances before and after the recess process, using a least squares fit and an estimation of recess channel length and width, extrapolating for channel resistance, and graphically determining channel thickness from the doping profile. Interferences from processing and test structure geometry affected the success of this determination to varying degrees. Depending on the etch process, the recess width is some function of the etch rate and recess length, values which must be known for successful curve fit and extrapolation. Further, the contact resistance measurements from the TLM are affected by parasitic resistances in the geometry of the structure as well as sheet resistance variations[6] resulting from less than ideal process control. Hence, the values used in the curve fit are not accurate, causing the extrapolated channel resistance and thickness to be inaccurate.

The electrical alignment structure was most affected by processing and measurement procedures. Due to long (150μm) bridge measurements, it is sensitive to sheet resistance variations and thus did not accurately indicate misalignment for processes with non-uniformities in the bridge material. For some processes, a thermal offset, due to interface layer conditions in a bridge contact, was a problem. In these cases, forcing current in both directions through the contact and averaging the voltage measurements resulted in misalignment values that could be validated by visual measurements. Also, in measuring bridge voltages, attention to equipment resolution is important. These measurements require sensing small voltages which are accurately obtained only with a microvolt meter.

The fatFET and diode test structures, used to characterize the active layer, were also process sensitive. Unlike the TLM and the alignment structures, these structures were tolerant of processing variations but did require the bias conditions to be optimized for the process. The test structures could then provide good data, if care was taken with the measurement procedure. Often this meant making the measurements manually rather than with an automated tester. The C-V measurements involved are susceptible to noise and require using coaxial cable down to the probe tips to obtain reliable and accurate data[7].

This study did not reveal total failure of any Task 4.E test structure, as every test structure appeared to perform adequately for some process lots and lines. The inconsistent performance related mainly to the TLM and electrical alignment measurements. Since these test structures are important monitors of FET performance[1], designs free of parasitics and with more tolerance to processing are needed. More rigorous test specifications are also needed to assure that appropriate test equipment and procedures are used.

Recommendations for Future Implementations

Based on this test structure performance analysis and other Task 4.E experiences, some recommendations are made concerning future methods for test structure design, implementation, measurement, data reduction, and documentation. The following recommendations are intended to improve and extend the performance of particular test structures and of the general test structure methodology.

Test Structures

Several test structures were developed to address the performance anomalies described above. Others were suggested to obtain information which is not available from the Task 4.E structures but is useful in process diagnosis and circuit design. An evaluation of these structures, which are summarized in Table 1, is underway.

Test Structure Methodology

The Task 4.E effort demonstrated the need for a more flexible implementation philosophy. More flexibility is needed to accommodate differences in process steps and standard operating procedures at the different manufacturers. These differences affect which test structures are meaningful and where on chips and wafers they can be placed. For example, test chip area allocated for several structures with n+ layers is non-productive space for a manufacturer who has no n+ in his process. Also, different processes use different numbers, sizes, and spacing of chips, need uniquely located dropouts for alignment marks, and routinely allocate unique locations for their own drop-ins. Regardless of the exact implementation at the chip and wafer level, high density testing can be maintained. The exact location of each data point is less important than the whole-wafer data profile. This is also true when using lower density monitoring for controlled processes, where location to location variation is minimal anyway. However, standards are still needed for test structure designs, test methods, and data reduction if comparisons between development and production lots or between manufacturers are to be valid. To facilitate using such standards, a

Table 1. Proposed changes and additions* to Task 4.E test structures

PROPOSED STRUCTURE	RATIONALE
Kelvin-cross contact resistor	Directly measures the interfacial contact resistance value that indicates contact quality (replaces TLM which included parasitic and sheet resistances in front contact resistance)
Mesa/channel van der Pauw	Directly measures channel sheet resistance, suitable for use with doping profile to determine channel thickness (replaces TLM which did not accurately measure contact resistances used to graphically determine channel sheet resistance and thickness)
Nanometer resolution electrical alignment[8]	Improves accuracy and reduces effects of sheet resistance variations; includes validation test pattern (replaces Task 4.E alignment structure, extending measurement precision from 0.1μm to 15nm)
Kelvin TLM	Improves accuracy of front contact resistance by using a Kelvin measurement technique (replaces TLM which included parasitic resistances)
van der Pauw alignment	Measures misalignment (replaces Task 4.E alignment structure)
*Contact resistor series	Enables assessment of contact uniformity
*Meander	Detects step coverage problems
*Interconnect resistor	Provides contact load resistance for designer
*Rotated FET series	Measures effect of stress due to nitride on different FET orientations

framework is needed to provide test structure designs and to document their use. This framework must also be consistent with providing flexible chip and wafer level implementations.

Such a framework is being successfully used in the silicon industry and is realized in the form of a computer-aided design (CAD) test structure library and test plan provided by NIST. When applied to the MIMIC technology, the test structure library consists of cells containing the layouts for test structures applicable to typical MIMIC processes. For most structure types, layouts for different size/layer combinations are included. The test plan document[9] covers the range of activities from choosing test structure implementations and designs to assessing the data obtained. Suitable cells can be selected and their implementation tailored for a process line, based on guidance provided in the test plan. The standard test structures are then measured and data reduced according to standard methods specified in the test plan. Some key points and features of the document regarding test structure implementation, design, measurement, and data reduction are discussed below.

Test Structure Implementation: In implementing the selected test structures, the reason for using test structures must be clear, as it affects the implementation approach. If a new process is being developed, high-density test structures may be needed to diagnose process problems, as illustrated in Figure 3. However, once these methods have identified the critical parameters for predicting yield and the process is stable, limited monitoring of these parameters is sufficient, as demonstrated in Figure 4, unless a higher density approach is needed as a statistical base for correlation.

When selecting test structures, the process must be defined, the physics of the process and products understood, and the yield goals known. Without this knowledge, the need for a particular monitor will not be obvious and the resultant test vehicle will not be totally effective. These considerations affect the choice of which test structure types and layer/size combinations are needed. Also, including validation test structures, such as alignment structures with built-in offsets, can be useful in diagnosing measurement problems.

Manufacturers typically use their own Process Vehicle Monitors (PVMs) independently from Task 4.E. Test structures used in PVMs often contain design interferences causing inaccurate measurements. However, including PVMs when using standard PCMs (as on Task 4.E and in Phase 2) is important. Such structures do provide results that can be used by the manufacturer to identify process conditions based on previous process history, although they cannot be reliably used for comparison with other processes.

The physical implementation of the selected test structures depends on the density required. For process diagnosis, a full wafer test chip implementation provides the high-density data required. For comparing or monitoring a controlled and characterized process, a reduced implementation is sufficient. Since the most meaningful test structures are ones that provide the critical parameters for assessing the performance of a given MMIC, the appropriate sets of critical test structures should be placed in regular patterns adjacent to the MMICs they monitor. If valid comparisons between manufacturers must be assured, specification of minimum sets and densities of test structures are needed. Depending on the density needed, the structures could be included either on-chip or in the kerf area.

Test Structure Design: For each type of test structure in the library, the test plan references the CAD library cell names for the existing layer/size combinations and provides top and side views for one combination. An appendix includes information pertinent to the CAD library, such as conventions for layer names, colors, and cell hierarchy. Most designs include a label, implemented in the top metal layer and adjacent to material of the unique layers, to aid in identifying the structure when viewed under a microscope. The test plan also provides information concerning the layout of each structure. It includes an explanation of design constraints needed to assure portability and immunity to yield limiting defects and specifies elements of the layout that can or should be adapted to the manufacturer-specific process. All layouts were designed for 2x6 modular probing, a commonally achievable capability.

Test Structure Measurement: As previously discussed, obtaining reliable and accurate data depends on using proper measurement procedures and instrumentation. The test plan specifies general requirements for such factors as dark kits, cabling, probe tips, impedance and resolution of meters, Kelvin measurements, and reproducibility measurements. Any exceptions are noted in each test procedure description.

Test Structure Data Reduction: The test plan specifies general requirements for outlier exclusion and measurement reproducibility analysis and discusses how these methods provide low overhead mechanisms that help avoid analyzing meaningless data. For each structure, the plan also presents, in tabular format, the measurements and computations to be made and discusses factors to consider in assessing the results.

The goal of supplying such a CAD library and test plan specification for the MIMIC community is to assist in providing a realistic, common reference point for assessing MIMIC performance.

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References

1. King,J.,Sizelove,J.,Krueger,T.,Brown,J.,Worley,R.,Gillespie,J., Cummins,S.E.,and Look,D.C.(1991).Overview of MIMIC Phase I Material/Device Correlation Study.GOMAC 1991

2. King,J.M.,Look,D.C.,Sewell,J., and Mitchell,W.(1989).GaAs Material/Device Correlation Study.Final Report.WRDC-TR-89-5015

3. Ayasli,Y. and Moniz,J.(1988).GaAs Materials/Device Analysis and Correlation.Final Report.Contract F33615-86-C-1050/S-793-02A-001

4. Statement of Work, MIMIC Materials/Devices Correlation, Added Task.(1988).Contract DAAL01-88-C-0835

5. Schuster,C.E. and Linholm,L.W.(Draft).Test Structure Assessment Document, MIMIC Phase 1.NIST Special Publication

6. Mazer,J.A.,Linholm,L.W., and Saxena,A.N.(1985).An Improved Test Structure and Kelvin-Measurement Method for the Determination of Integrated Circuit Front Contact Resistance.J.of the Electrochemical Society,Vol.132,No.2,February 1985,pp.440-443

7. Roitman,P.R.,Suehle,J.S.,Russell,T.J.,and Gaitan,M.(1986).On The Measurement of Capacitance on Wafers.IEEE VLSI Workshop on Test Structures,pp.96-104

8. Cresswell,M.W.,Gaitan,M.,Linholm,L.W., and Allen,R.A.(1991). A Slide Wire Potentiometer Test Structure for Wafer Mapping Interlevel Misregistrations of the Order of Nanometers.Proc.IEEE 1991 Int. Conference on Microelectronic Test Structures,Vol.4,No.1,March 1991,pp.129-134

9. Schuster,C.E.,Linholm,L.W.,Ellenwood,C.H.,and Marshall,J.C. (Draft).A Computer-Aided Design Library and Test Plan for MIMIC technologies.NIST Special Publication