Characterization of Paralleled Super Junction MOSFET Devices under Hard- and Soft-Switching Conditions

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Abstract— **The super junction (SJ) MOSFET exhibits conduction and switching properties similar to those of conventional power MOSFETs. In this paper, we investigate possible benefits and problems associated with connecting SJ MOSFET in parallel for high-power applications. Measured circuit performances of paralleled SJ MOSFET devices are evaluated under hard- and soft-switching conditions. The measurements include (1) turn-on and turn-off switching voltage and current comparison, (2) gate driver resistance effects on current sharing between paralleled SJ MOSFET devices, and (3) SJ MOSFET body diode behavior under hard- and soft-switching conditions. Two test circuits are developed for paralleled SJ MOSFET evaluation. One is an auxiliary resonant snubber chopper for the near zero-voltage switching test, and the other one is an auxiliary resonant snubber inverter for the true zero-voltage condition test. Experimental results indicate that SJ MOSFET can be paralleled without the need for precise device matching if the gate drive resistances are closely matched.**

I. Introduction

A new class of MOS-gated power semiconductor devices, the super junction (SJ) MOSFET, is considered a breakthrough device because it offers a much-reduced on-resistance for high voltage applications over the conventional power MOSFET [1]. This device exhibits conduction properties similar to those of conventional power MOSFETs with positive temperature coefficients [2]. It is therefore expected that the SJ MOSFET can be used in parallel configurations under steady state conditions.

Conventional power MOSFETs often are used in parallel configurations for higher power switching applications. The purpose of this paper is to study the dynamic current sharing behavior of SJ MOSFET for parallel operation in both hard- and soft-switching circuits.

Conventional power MOSFETs and SJ MOSFET devices suffer effects of slow recovery of the drain-body diode. In chopper-type converters where the current flows through an inductor in one direction, the commutating diode turn-off current is diverted through a fast external diode, and the associated MOSFET turn-on current does not contain a large diode-recovery current transient. Therefore, the drain-body diode in SJ MOSFET is not expected to restrict the use of paralleled SJ MOSFET devices in this type of converter. For two- and four-quadrant inverter applications, however, it is difficult to use MOSFET devices and parallel them for high power applications due to the slow reverse recovery of the drain-body diode.

For hard-switching applications, a series diode can be used with the MOSFET to block the recovery of the drain-body diode. An anti-parallel, fast-recovery diode can then be used in parallel with the MOSFET-series-diode combination to implement commutation. The resulting device of this remedy does not allow parallel-operation because the added diode has a negative temperature coefficient.

An option that may allow parallel MOSFETs to be used in inverter applications is the use of the zero-voltage soft-switching circuit. This circuit temporarily diverts the freewheeling or commutating diode current. This technique provides extra time for the drain-body diode in the MOSFET to recover before voltage is reapplied [3–6].

In this paper, the switching behavior of paralleled SJ MOSFET devices under soft-switching conditions is studied to explore the possibility of applying paralleled SJ MOSFET in high-power inverter applications. The experimental results indicate that SJ MOSFET can be paralleled without the need for precise matching. However, the gate drive resistors need to be matched to ensure equal switching delays and thus equal dynamic current sharing. Under hard turn-on conditions, the differences between gate-drives resistances-related switching delays might cause the slower device to be over-stressed. Under the zero-voltage soft turn-on condition, the mismatch of gate resistances is less of a problem because the switching energy and stress are nearly zero. It is also found that better current sharing can be achieved with lower-value gate resistors because the MOSFETs switch faster, and the periods of potential mismatch are reduced.

II. Zero-Voltage Soft-Switching Test Circuits

A. Device Test Circuits

Two test circuits are developed for evaluating paralleled SJ MOSFET switching performance. The first one, shown in Fig. 1, is an auxiliary resonant snubber chopper (ARSC). The second is an auxiliary resonant snubber inverter (ARSI), shown in Fig 2.

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The ARSC circuit consists of a two-quadrant chopper with two pairs of paralleled SJ MOSFET devices (S_1, S_2) and (S_3, S_4), and the freewheeling diodes D_1 and D_2. For soft turn-off, snubber capacitors C_r are connected across the main devices including the SJ MOSFET pairs and the freewheeling diodes. An auxiliary resonant circuit that consists of an auxiliary switch S_x, diode D_x, and resonant inductor L_r, is connected across the inductive load L. Because the initial condition of the resonant inductor current is not controllable, this type of circuit can achieve only near-zero-voltage turn-on [7]. The major components used in this circuit are listed as follows:

S_1 - S_4: SJ MOSFET, rated 190 mΩ, 20 A, 600 V
D_1, D_2: fast reverse recovery diode, rated 20 A, 600 V
L: 2 mH
L_r: 3 μH
C_r: 0.027 μF

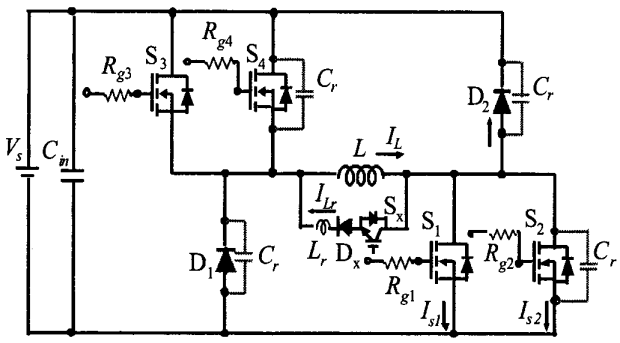


Fig. 1. The auxiliary resonant snubber chopper test circuit.

The two freewheeling diodes, D_1 and D_2, can be replaced with SJ MOSFET devices, and the test circuit becomes an auxiliary resonant snubber inverter (ARSI), as shown in Fig. 2. By connecting gates and sources together, the two paralleled switch pairs, (S_5, S_6) and (S_7, S_8), become freewheeling diodes, and the circuit operation is identical to Fig. 1.

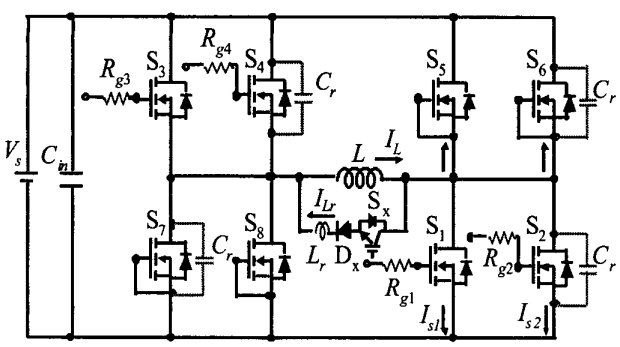


Fig. 2. The auxiliary resonant snubber inverter test circuit.

If the gate-sources of (S_5, S_6) and (S_7, S_8) switch pairs are controlled with pulse-width-modulation (PWM) signals, then the circuit becomes a four-quadrant, soft-switching chopper or inverter. In this case, D_x needs to be changed to add an anti-paralleled switch to allow bi-directional, resonant current control. As described in [3], the circuit allows the establishment of an initial resonant inductor current by keeping (S_5, S_6) and (S_7, S_8) switch pairs on for a short period at the beginning of resonance to achieve true zero-voltage turn-on.

B. Switch Timing

A two-pulse sequence strategy is used to gate the main devices (S_1, S_2, and S_3, S_4) with a fixed time period to establish the desired load current in L. The soft-switching operation of the ARSI and ARSC circuits was previously described [7][8]. During turn-on, the resonant branch circuit diverts the current in the freewheeling diode to the drain-body diode and provides a zero-voltage condition to the MOSFET. During turn-off, the voltage rate of rise is reduced by snubber capacitor C_r.

Fig. 3 shows the gate signals and corresponding device voltage and current waveforms for the ARSC test circuit. The SJ MOSFET devices are turned on with V_{gs} at time t_1, and the load inductor L is linearly charged with a $di/dt = V_s/L$. At time t_2, the load current, I_L, increases to $(t_2 - t_1)V_s/L$, and the two SJ MOSFET devices are turned off to discharge the load current. For the ARSC circuit, the freewheeling diodes, D_1 and D_2, are fast reverse recovery types. For the ARSI circuit, the slow recovery body diodes of SJ MOSFET devices ($S_5 \sim S_8$) are used. Results for the ARSI circuit are shown in section III. *D*. Between time t_3 and t_4, the auxiliary switch, S_x, turns on with V_{Aux_GE}, and the resonant branch circuit establishes a resonant current, I_{Lr}, to divert the load current away from the freewheeling diodes and allows the devices to be switched under the zero-voltage condition. The second V_{gs} pulse starts right after the SJ MOSFET drain-source voltage, V_{ds}, drops to zero. The purpose of this second pulse is to monitor the zero-voltage turn-on condition so it is typically a short pulse of a few microseconds.

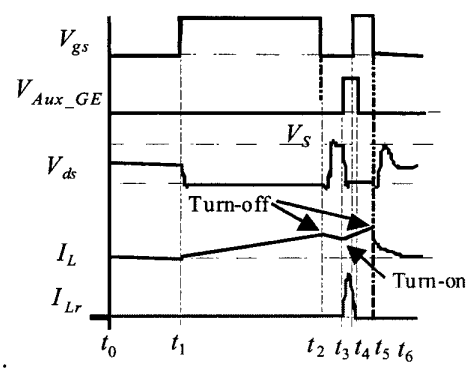


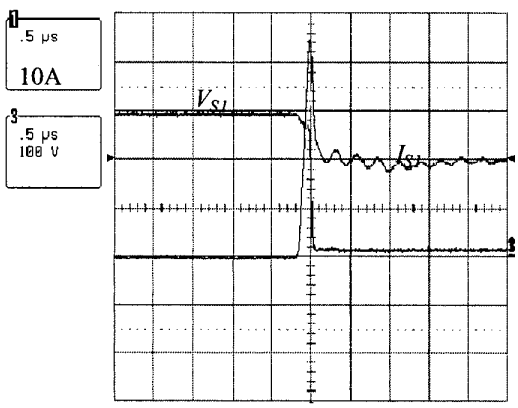
Fig. 3. Corresponding gating signals and waveforms of the test circuits.

III. Device Characterization Results

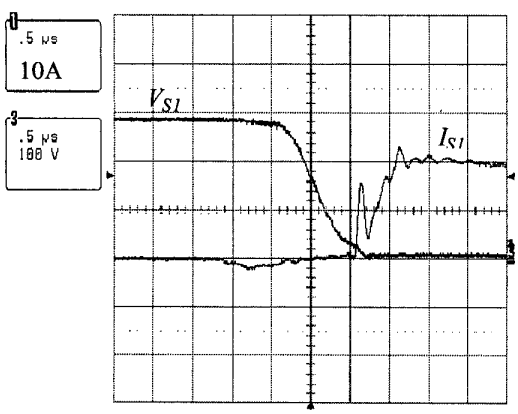
A. Turn-on Characteristic

Fig. 4 shows the turn-on waveforms of the current and voltage of the SJ MOSFET under hard- and soft-switching conditions in the ARSC tester at 300 V bus voltage and a load current of 40 A. Each device shares 20 A equally.

It can be seen that the turn-on current of the SJ MOSFET has an overshoot of 45 A with 225 A/μs rate under hard-switching conditions. Under soft-switching conditions, there is no overshoot current, and the current rise rate is reduced significantly. Notice that there is an initial current bump in soft turn-on because the device is not turned on at true zero voltage, and a small voltage across the snubber capacitor needs to be discharged when the device is gated on. This initial current bump corresponds to the capacitor discharge current. Its magnitude, however, is much smaller than the diode reverse recovery current under the hard-switching condition.



(a) Turn-on under hard switching



(b) Turn-on under soft switching

Fig. 4. SJ MOSFET turn-on under hard- and soft-switching conditions.

Fig. 4(b) indicates that the intersection area of voltage and current diminishes, and the turn-on loss under soft switching is reduced drastically as compared with the hard-switching case. The turn-on energy can be obtained by the integration of the intersection area.

Fig. 5 shows the integration results of the turn-on energy for both hard- and soft-switching conditions. The SJ MOSFET turn-on energy under soft switching is reduced significantly compared to hard switching. At this 20 A current condition, the turn-on energy is reduced from 1 mJ to 0.12 mJ. The turn-on loss associated with soft switching comes from the zero crossing area, where the device voltage is not truly zero because it is tested with the ARSC circuit, which does not provide initial inductor boost current to discharge the resonant capacitor.

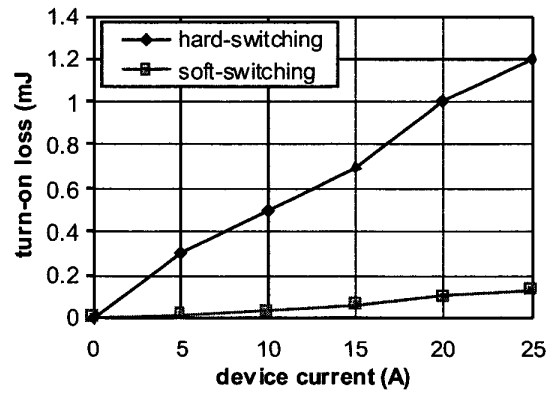
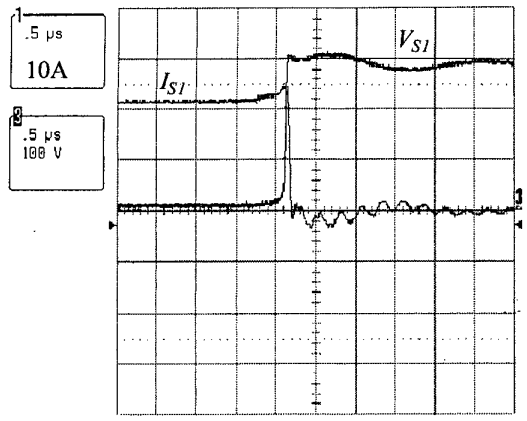


Fig. 5. Turn-on losses under hard- and soft-switching conditions.

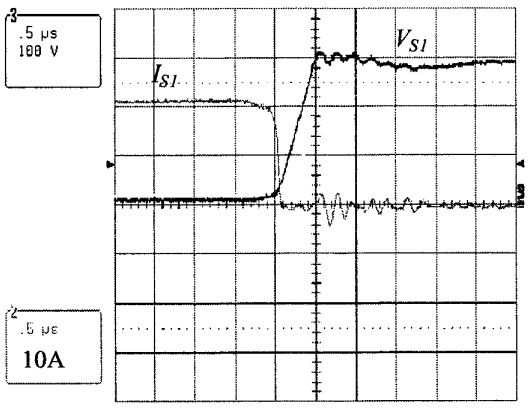
B. Turn-off Characteristic

Fig. 6 shows the turn-off waveforms of the current and voltage of the SJ MOSFET devices under hard- and soft-switching conditions in the ARSC test circuit at a 300 V bus and with a device current of 20 A. The dv/dt under hard switching is about 3000 V/μs, while under soft switching it is about 600 V/μs. The test results indicate that the turn-off voltage has nearly zero overshoot voltage under both hard- and soft-switching conditions. This can be attributed to a good circuit layout that involves minimum parasitic inductance.

The turn-off energy, again, can be obtained from the integration of the intersection area of the voltage and current. Fig. 7 shows the integration results at different current conditions. It indicates that the turn-off energy is greatly reduced because the resonant capacitor slows down the SJ MOSFET voltage rise during turn-off, thus diminishing the intersection area of voltage and current. At the 20 A condition, the turn-off loss is decreased from 0.55 mJ under hard switching to 0.12 mJ under soft switching.



(a) Turn-off under hard switching



(b) Turn-off under soft switching

Fig. 6. SJ MOSFET turn-off under hard- and soft-switching conditions.

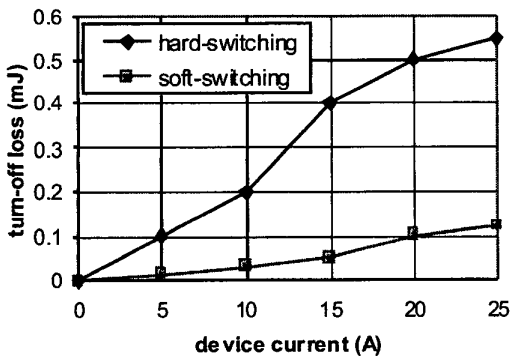
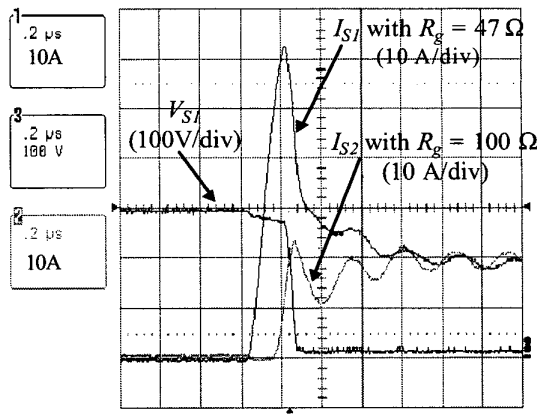


Fig. 7. Turn-off loss under hard- and soft-switching conditions.

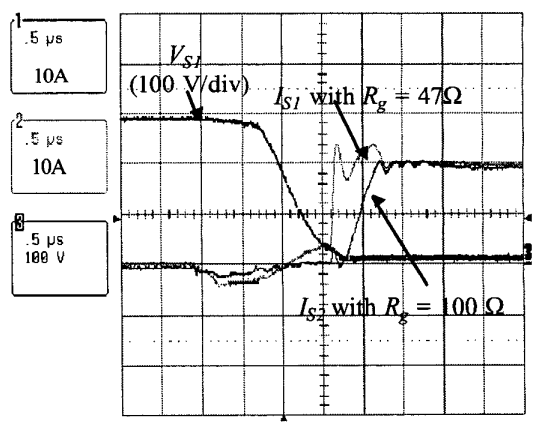
C. Current Sharing with Different Gate Driver Resistance

When there is a variation in gate drive resistance, current sharing during switching is no longer equal between two paralleled devices. Fig. 8 compares turn-on current sharing of paralleled SJ MOSFET devices with different gate-drive resistances (47 Ω & 100 Ω) under hard and soft switching in the ARSC circuit. For the current rise in the hard-switching condition, the device with smaller gate drive resistance initially takes all the load current of 40 A plus the overshoot current caused by the reverse recovery of the freewheeling diode. Under soft switching, the device with the smaller gate drive resistance initially takes all of the current, but because of the reduced rate of current rise this current never exceeds the steady-state current. The device with the larger gate resistor begins conducting, and the currents eventually balance.

It can be seen from these tests that the SJ MOSFET devices can be paralleled for both hard- and soft-switched turn-on as long as the gate resistors for each device are matched. For soft-switched operation, the matching is not as critical in balancing the switching energies, in part because the energy is so much less.



(a) Turn-on current sharing under hard switching



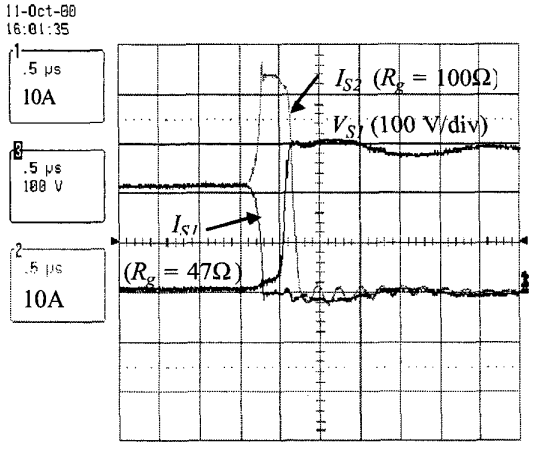
(b) Turn-on current sharing under soft switching

Fig. 8. Comparison of SJ MOSFET turn-on current sharing under hard and soft switching.

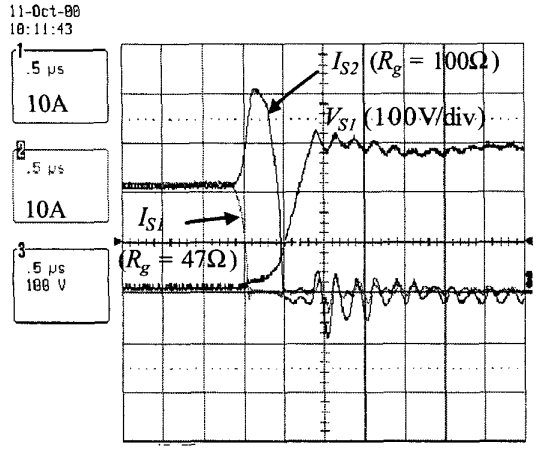
Fig. 9 shows the comparison of turn-off current sharing of paralleled SJ MOSFET devices with different gate drive resistance (47 Ω & 100 Ω) for hard- and soft-switching conditions. The device with the smaller gate drive resistance

shuts off first, causing the other device having the larger gate drive resistance to take the entire load current. There is no significant difference between hard and soft switching in current fall and current sharing during turn-off, except that the soft switching exhibits a slower voltage rise-rate, dv/dt.

In terms of turn-off energy, the device with the smaller gate resistance has very little intersection between voltage and current, and thus the turn-off loss is nearly zero. The device with larger gate resistance assumes the bulk of the turn-off energy; however, this energy is reduced for the soft-switched case.



(a) Turn-off current sharing under hard switching



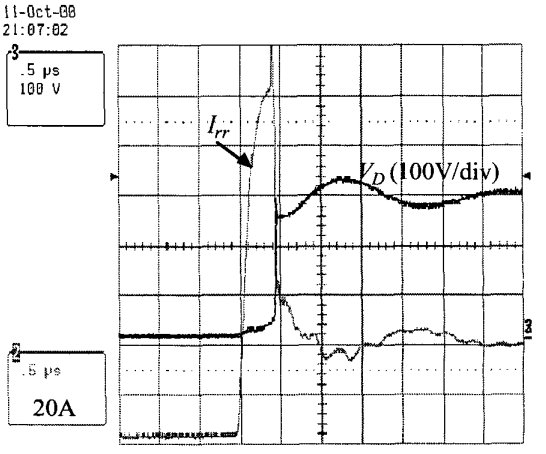
(b) Turn-off current sharing under soft switching

Fig. 9. Comparison of SJ MOSFET turn-off current sharing under hard and soft switching

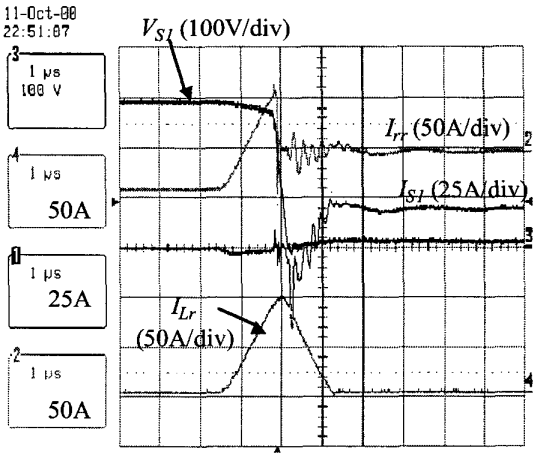
D. Body Diode Effect on Soft Switching

The ARSI circuit of Fig. 2 is used to investigate the drain-body diode in the SJ MOSFET. For this investigation, the gates and sources of S_5 and S_6 are connected together to obtain the drain-body diode characteristics and to observe its effects on the switching MOSFETs S_1-S_4. Fig. 10(a) shows current and voltage waveforms for the S_5-S_6 combination acting as a diode for the hard-switching condition. The current I_{rr} is the reverse-recovery current, and V_D is the drain (cathode) voltage of this diode. The peak recovery current is 120 A. Fig. 10(b) shows the current and voltage waveforms for the SJ MOSFET switch S_1, and also I_{rr} and resonant-branch current I_{Lr} for soft switching. The value of the soft switching is evident in the reduction of I_{rr} in Fig. 10(b).

For hard-switching conditions, the reverse-recovery time, t_{rr}, is about 1 μs, and the peak reverse-recovery current is about 120 A for a 40 A load condition. For soft-switching conditions, the resonant inductor diverts the current away from the slow body diode, and the reverse-recovery current is reduced to 55 A. When this reverse current is shut off during the reversal of the inductor current I_{Lr} slope, the drain-body diodes in S_3-S_4 conduct initially. Devices S_3-S_4 then are turned on under zero-voltage conditions. The switch current and voltage do not show overlap, and thus the turn-on loss is eliminated.



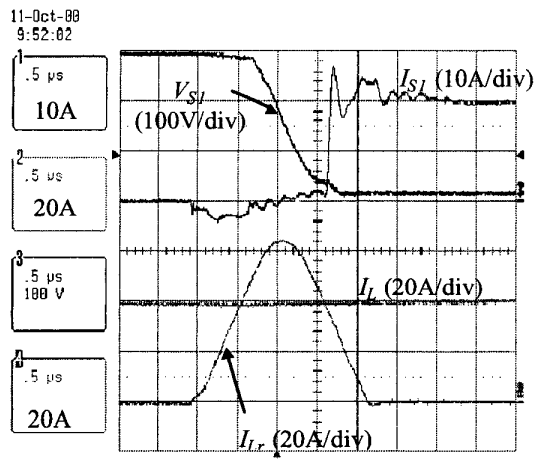
(a) Reverse recovery under hard switching



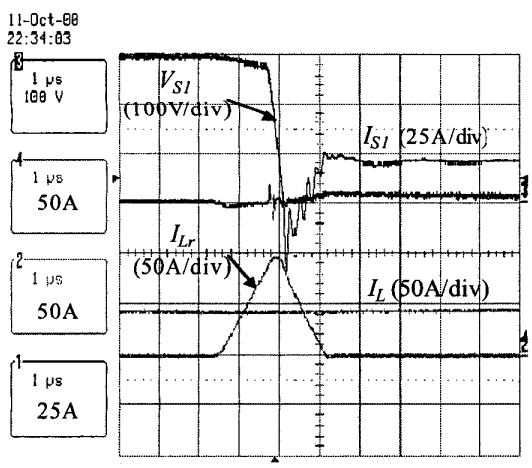
(b) Reverse recovery under soft switching

Fig. 10. Reverse recovery of the paralleled body diodes under hard- and soft-switching in the ARSI circuit.

The slower recovery of the drain-body diodes actually offers an advantage in the ARSI circuit of Fig. 2. The recovery current causes an additional boost for I_{Lr} that drives V_{S1} down sooner and provides true zero-voltage turn-on. Figs. 11(a) and 11(b) compare the difference between the use of fast and slow recovery diodes. Fig. 11(a) indicates that the SJ MOSFET can only reach near zero-voltage switching in the ARSC circuit that uses the fast-recovery diodes, while Fig. 11(b) shows that the SJ MOSFET achieves true zero-voltage switching in the ARSI circuit with the drain-body diodes.



(a) Near zero-voltage switching with ARSC



(b) True zero voltage switching in ARSI

Fig. 11. Comparison of soft switching in the ARSC and ARSI circuit.

IV. Conclusion

The switching performance of paralleled SJ MOSFET devices was characterized under hard- and soft-switching conditions through empirical measurements. The experimental results indicate that SJ MOSFET devices can be paralleled without precise matching. Under hard-switching conditions, the devices need not necessarily be matched, but the gate driver resistors need to be matched to ensure equal dynamic current sharing. For soft-switching applications, a mismatch in gate resistors does not increase switching stress, but still causes uneven power dissipation. Measurements show that better current sharing can be achieved with smaller gate resistors. This yields faster switching and reduces the unequal current sharing period for both hard- and soft-switching conditions.

When utilizing the slow reverse recovery characteristic of the paralleled body diodes of the SJ MOSFET, an initial resonant inductor current can be created to achieve true zero-voltage switching in the ARSI test circuit. This true zero-voltage switching feature is very desirable in further reduction of turn-on loss and noise.

From this work, it can be concluded that SJ MOSFET devices can be paralleled without special device matching, provided the gate resistances are matched. Therefore, SJ MOSFET devices can be applied to high-power inverter designs.

References

[1] L. Lorenz, M. Maerz, and G. Doboy, "Improved MOSFET," in *PCIM Magazine*, Sept. 1998, pp. 14 – 23.

[2] J.-S. Lai, B. M. Song, R. Zhou, A. R. Hefner, D.W. Berning, and C. C. Shen, "Characteristics and Utilization of a New Class of Low On-Resistance MOS-Gated Power Device," *Conf. Rec. of IEEE IAS*, Nov. 1999, pp. 867-873.

[3] J. S. Lai, R. W. Young, G. W. Ott, and F.Z. Peng, "A Delta-Configured Auxiliary Resonant Snubber Inverter," *IEEE Trans. Ind. Appl., Vol.32, No.3, May/June 1996*, pp. 518-524.

[4] R. W. DeDoncker and J. P. Lyons, "The Auxiliary Quasi-Resonant dc Link Inverter," in *Conf. Rec. of IEEE PESC*, June 1991, pp. 248–253.

[5] W. McMurray, "Resonant Snubbers with Auxiliary Switches," *IEEE Trans. on Ind. Appl.*, Vol. 29, No. 2, Mar./Apr. 1993, pp. 355–362.

[6] J. P. Gegner and C. Q. Lee, "Zero-Voltage Transition Converters using Inductor Feedback Technique," in *Conf. Rec. of IEEE APEC*, Orlando, FL, Mar. 1994, pp. 862–868.

[7] H. Yu, B. M. Song, J. S. Lai, "Design of a Novel Soft-Switching Chopper," VPEC Seminar, Blacksburg, VA, Sep. 1998, pp. 273-277.

[8] J. S. Lai, "Fundamentals of a New Family of Auxiliary Resonant Snubber Inverters," *Conf. Rec. of IEEE IECON*, Nov. 1997, pp. 645-650.