

Driving High Surge Currents into Long Cables: More Begets Less

Arshad Mansoor, Member, IEEE
Power Electronics Applications Center
Knoxville, TN 37932 USA

François D. Martzloff, Life Fellow, IEEE
National Institute of Standards and Technology¹
Gaithersburg, MD 20899 USA

Abstract - Reality checks can and should be applied to proposals for characterizing the surge environment and application of surge-protective devices (SPDs) to end-user, low-voltage power systems. One such check is the fact that driving a large current with steep front toward an SPD installed at the far end of a branch circuit cable could require such a high voltage that the connections at the near end of the cable will flashover, limiting the stress applied to the far-end SPD. Tests and numerical modeling were performed to support this thesis. The results of real-world measurements and modeling, presented in the paper, are in good agreement and validate each other. From that point on, the model allows parametric variations of cable length and surge current amplitude and waveform, of which several examples are presented.

I. INTRODUCTION

In the never-ending quest for better data on the frequency of occurrence and level of threat of overvoltages, we should not overlook some "reality checks" that can be applied to proposals for characterizing the surge environment. One such check is the fact that forcing a large surge current with steep front toward a surge-protective device (SPD) installed at the far end of a branch circuit cable could require such a high voltage that the wiring device connections at the near end of the cable will flashover, limiting the stress applied to the far-end SPD.

¹ Electricity Division, Electronics and Electrical Engineering Laboratory, Technology Administration, U.S. Department of Commerce

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Large surge currents considered by standards-writing bodies and discussed in this paper are presumed to impinge from the outside of a building, as a result of a direct or indirect lightning flash. These involve postulated rise times in the order of a few microseconds, with a duration ranging from a few tens to a few hundreds of microseconds. While there are different propositions made on what duration should be considered as "representative" waveforms, there is a consensus on rise times ranging from about 4 μ s to 20 μ s [1]. However, consensus on what value to select for "representative" amplitude(s) has been challenged by proposals to increase the current surge capability of devices intended for installation at the end of branch circuits.

A growing trend in the application of SPDs to residential or commercial installations is to provide "whole-house protection" with an *upstream* SPD connected at the service entrance, and *downstream* SPDs in the form of plug-in devices installed at receptacles. Selecting the ratings for these two devices is the subject of some debate. The *voltage rating* of the devices introduces the issue of cascade coordination which has been addressed at length in the literature [2]-[8] and will not be discussed here. At this point in time, the vast majority of installations do not include an upstream SPD intentionally connected at the service entrance, other than a gap in the revenue-meter socket. This gap is provided by the meter manufacturer to protect the meter more than the downstream installation. Nevertheless, there are other "gaps" at the service panel -- the clearances of the wiring devices, which have some limits to their voltage withstand capability.

II. SURGE PROPAGATION IN WIRING

The possibility of a clearance flashover is the basis of our thesis: If a large surge current is postulated as propagating downstream (and then taken as a requirement for the downstream SPD), the propagation characteristics of this surge current would result in high voltages at the service entrance, upstream. In turn, the high voltage would cause flashover of upstream clearances, acting as a relief valve for the surge energy headed for the downstream SPD. This relief action would then contradict the proposed requirement for high energy-handling capability of the downstream SPD. Thus, appropriate selection of *current ratings* for the downstream SPD, in the light of our thesis, should take into consideration this reality check that defines an upper limit for the current rating required for the downstream SPD.

The surge propagation characteristics mentioned in the preceding paragraph are controlled by three parameters: the impinging surge, the impedance of the wiring from the service entrance to the downstream SPD, and the I-V response of the downstream SPD. The impinging surge could be considered either as a voltage source or as a current source. The present consensus is to consider it as a current source, resulting from the coupling and subsequent division of a lightning surge, part of which impinges on a given service entrance.

The impedance of the wiring is that of two parallel wires of known dimensions and separation. It can be represented either by lumped parameters -- series R and L and parallel C -- or by a "short" transmission line. The reason for placing quote marks around the qualifier of "short" is that the term is to be viewed by comparing travel time over the length of the transmission line and duration of the traveling pulse -- another subject discussed in the literature [9] that we will not discuss here, with the exception of a brief comparison of results obtained when modeling the propagation with lumped parameters or with a transmission line.

When using the lumped RLC model, during the rise of the surge current, the significant parameter of the wiring impedance is its inductance, L . The voltage at the upstream end resulting from driving the surge current into such an impedance is primarily $L \times di/dt$, with di/dt determined by the amplitude and rise time.

By performing surge measurements on real-world wiring components, followed by numerical modeling with the Electromagnetic Transients Program (EMTP)² [10], this proposition can be verified and applied to a range of postulated surge waveforms and typical configurations found in the premises wiring of low-voltage systems. These results will allow developing realistic recommendations for the rating of SPDs offered for surge protection at the equipment location -- either as plug-in additions by the end-user, or as permanently wired devices at the end of typical branch circuits. The measurement results also show the need to consider the possibility of "blind spots" in the protection schemes, and illustrate our title paradox of "*more begets less*."

Measurements were conducted on a simple circuit consisting of 9 meters of nonmetallic jacket cable typical of residential installations, with a metal-oxide varistor connected downstream at the far end. A Combination Wave surge generator, suitable for producing the waveform described in IEEE/ANSI C62.41-1992 [1] was used to inject a surge current at the upstream end of the cable. Current and voltage waveforms were recorded. The current waveform resulting from this injection was duplicated in a closed-form equation to be applied as the postulated surge current injected into the EMTP model of the circuit, allowing computation of the corresponding voltages.

² Certain commercial instruments and software packages are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that these are necessarily the best available for the purpose.

III. MEASUREMENTS AND MODELING

A. Characterizing the varistor

First, the varistor to be connected at the far end was tested to determine its I-V response and demonstrate that the model to be used for this highly nonlinear component would be adequate to simulate its behavior in the circuit when connected at the downstream end. Figure 1 shows the test circuit used for making that measurement. The surge generator used for the tests was the KeyTek 711 with a P7 wave-shaping output network.

The varistor used in these tests was a 20-mm diameter metal-oxide varistor (MOV) disc, rated 130 V rms (200 V at 1 mA dc). The inductance L_p shown in series with the varistor is not a deliberate addition of a real component, but is the representation of the coupling between the loop where the surge current flows and the voltage measurement loop formed by the varistor leads and the two probes used for the differential measurement. That inductance is included in the model as a discrete series inductance, with a value of 0.5 μ H selected to emulate the observed voltage at the point of measurement -- which is not the "pure" varistor voltage, as discussed in the narrative of Figure 2.

Figure 2 shows the recording obtained for a particular setting of the surge generator, and Figure 3 shows the result of modeling the circuit shown in Figure 1 for an injected current surge corresponding to the actual current surge recorded in Figure 2. The equation used for the modeling is a damped sine wave that allows a close approximation of the current delivered by typical Combination Wave generators into inductive loads [7]. It is known that actual generators tend to produce an "undershoot" when connected to an inductive load, and this test was no exception. However, computational artifacts occur when using a simple damped sine wave because its di/dt derivative (a cosine) is not zero at time zero. Furthermore, we know that nature does not allow an instantaneous jump of current from zero to a steep rise. By adding a multiplier term $[1-e^{(-t)}]$, these artifacts are eliminated and the waveform has a "gentle toe" which is a better model of reality. This improved equation is then:

$$I = 4200 * \sin(0.126t) * e^{(-t/28.1)} * [1-e^{(-t)}] \quad (1)$$

with I in amperes and t in microseconds.

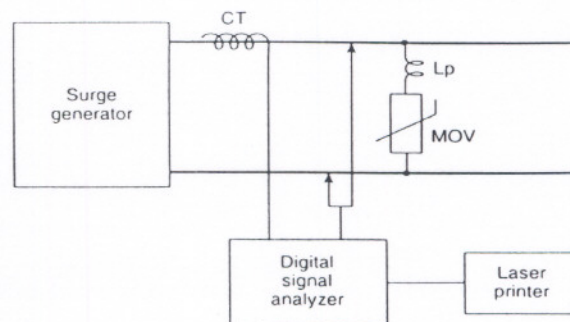


Figure 1 - Test circuit for determination of the I-V characteristics of the varistor

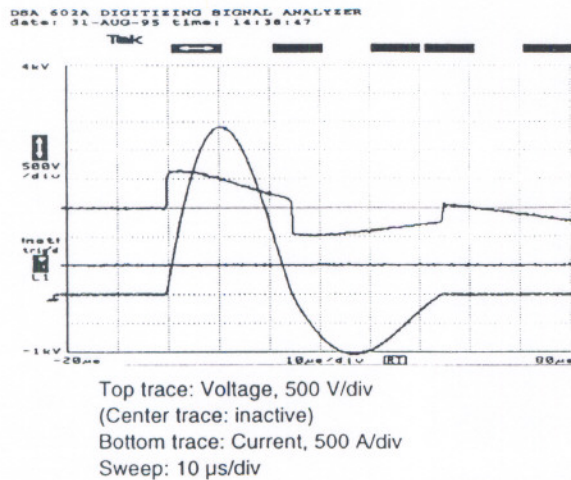


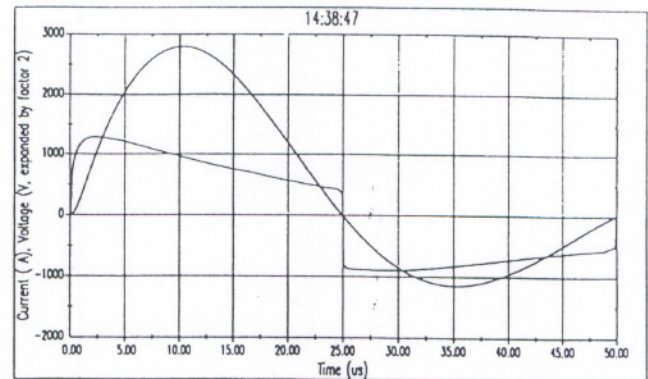
Figure 2 - Real-world recording

Inspection of Figures 2 and 3 clearly shows the agreement between real-world measurements³ and model, and thus merits some observations. One might have expected a flat-top voltage waveform reflecting the clamping action of the varistor. Instead, a drooping waveform is observed. This droop is caused by the parasitic inductance L_p in series with the ideal varistor. At the time of current peak ($di/dt = 0$), the "true" varistor voltage is seen on the oscillogram. Before the peak, the positive $L_p \times di/dt$ adds a spurious voltage to the recording. After the peak, the negative $L_p \times di/dt$ subtracts the spurious voltage.

These observations are significant in appreciating the all-important inductive effects during the rise and fall of a surge current in the wiring of branch circuits. The issue of the importance of inductance versus other circuit parameters [11] hopefully has been put to rest by the surge and impedance measurements with corresponding computations performed in the so-called "Upside-Down House" [12], a real-world replica of a typical residential wiring system. In [12], it was shown that inductive effects prevail, so that *rate of rise* of the surge current and *circuit inductance*, more than any other parameter, are the significant parameters for the voltage necessary at the upstream end to drive a given current into the branch circuit.

The model used in the simulation for the varistor is derived from the published varistor I-V characteristic (general shape and slope of the curve) with one specific point defined by the "true" varistor voltage read from the oscillogram of Figure 2 at the point of zero $L_p \times di/dt$ contribution. In turn, this varistor model will be used for the modeling of a varistor connected at the downstream end of a branch circuit, as discussed in the following reported measurements and simulations.

³ The measurements reported in this paper have been made with instrumentation for which the cumulative uncertainty should not exceed 5 to 6%. Given the process of applying the measurement results to the response of surge-protective devices exposed to environment with characteristics that are at best known within an order of magnitude, this level of uncertainty does not affect the practical conclusions.



Note: the voltage trace has been expanded by a factor of 2 to enhance resolution on the vertical scale.

Figure 3 - Modeling the circuit of Figure 1 with the impinging current set to match the test current, as shown in Figure 2

B. Measurement and modeling with varistor installed at the downstream end of a branch circuit

The circuit of Figure 4 shows the varistor characterized by the test and modeling in the preceding paragraphs, connected at the downstream end of a "branch circuit" consisting of two copper conductors of 2-mm² cross-section (#12 AWG) with solid insulation and a separation of 6 mm between centers. The first current transformer monitors the total current impinging at the upstream end. The second current transformer monitors the current flowing toward the downstream end, which will be imposed on the varistor. The clearances at the upstream end, such as clearances in a service-entrance panel, are represented by a discrete gap that will be set to produce sparkover at some given voltage during the test as well as in the model.

Figure 5 shows the recording obtained with the circuit of Figure 4, with the surge generator left at the same setting as that used for Figure 2. To determine the response of the circuit without the clearance limitation, the gap setting was adjusted for this test so that no sparkover occurred at the upstream voltage developed for the current delivered by the generator.

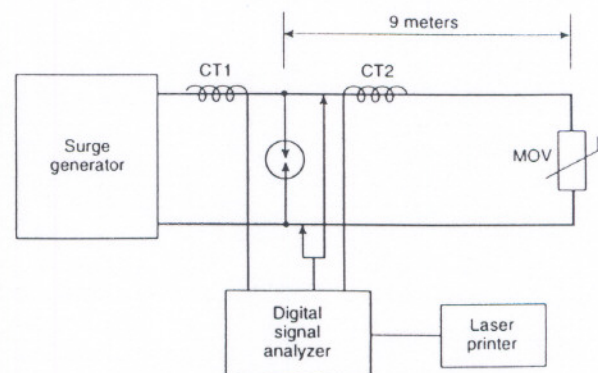


Figure 4 - Test circuit for determination of the voltage necessary at the sending end to drive a given current into the far-end SPD

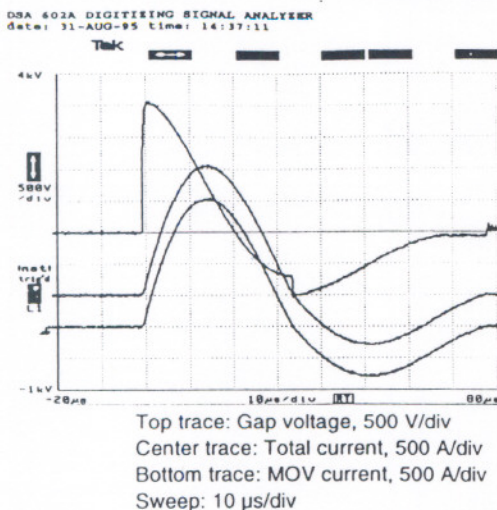


Figure 5 - Real-world recording of sending-end voltage with gap set for no sparkover

Comparing the traces of Figure 5 and Figure 2, the addition of the inductance of the 9 meters of branch circuit changes the load on the surge generator, reducing the current peak from the 2.8 kA in Figure 2 down to 2 kA in Figure 5.

The two current traces of Figure 5 are identical. Since there is no current diverted by the gap, the current in the branch circuit is the same as the current delivered by the surge generator.

Another effect of the added inductance is the increase in the time from origin to the first current zero, 33 μs in Figure 5, compared to 25 μs in Figure 2. In the subsequent model, that change of the actual impinging current surge is taken into consideration by modifying the current equation as follows:

$$I = 3571 * \sin(0.095t) * e^{(-t/26.1)} * [1 - e^{(-t)}] \quad (2)$$

with I in amperes and t in microseconds.

Turning to the modeling, Figures 6 and 7 show the waveforms of the impinging current, as defined by Eq. (2), and the resulting voltage at the upstream end. To address some concerns expressed by colleagues in discussions of this subject, the EMTP modeling was also done with the transmission-line model which is readily available in the EMTP code. Figure 6 was obtained with the lumped-parameter circuit model, and Figure 7 was obtained with the transmission-line model.

Inspection of the two figures reveals no difference in the results. The only difference is in the consumption of computing time: with the transmission line model, the computation time-step has to be significantly shorter (0.02 μs in this case) than the travel time for the reflections, while in the case of the lumped model, the time-step can be longer (0.1 μs in that case). The result is that the simulation of Figure 6 took 43 seconds on a 486-based PC, compared to 263 seconds for Figure 7. Therefore, the lumped-parameter model is perfectly adequate to represent reality, and performing a transmission-line analysis [5] is an unnecessary consumption of computing time and resources.

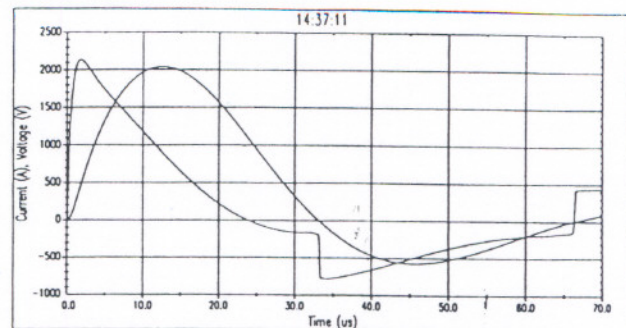


Figure 6 - Impinging current and resulting upstream voltage as computed with lumped-parameters model

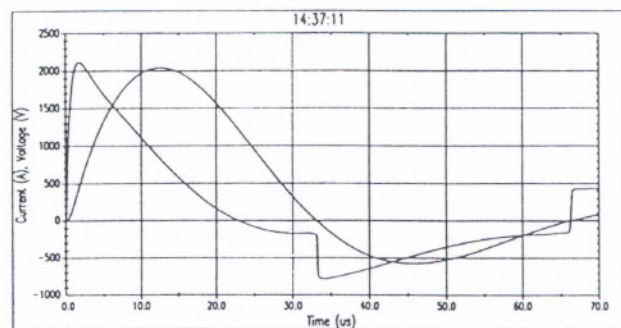


Figure 7 - Impinging current and resulting upstream voltage as computed with transmission-line model

In both Figures 6 and 7, the effect of the branch circuit inductance on the resulting voltage is apparent as the peak voltage occurs at the beginning of the rise (as soon as the "gentle toe" effect ceases), not at the peak of the current. The step change in the voltage trace corresponds to the reversal of the current in the varistor, showing the relative contributions of the varistor effect and of the inductive effect as seen from the upstream end.

Table 1 below shows the results of such computations for the waveform of Figures 5, 6 and 7. As mentioned above, the insertion of an inductance in the load connected to the surge generator increased the rise time beyond the standard 8 μs. In making the parametric computations, we chose to stay with this 10 μs value to maintain continuity with the test/model validation.

TABLE 1

Upstream voltage (in kV) necessary to drive a current of the peak value shown (columns) and rise time of 10 μs into a branch circuit of length as shown (rows), terminated with a 130-V rated varistor

Length \ Peak	2 kA	3 kA	5 kA	7 kA	10 kA
10 m	2.3	3.3	5.2	7.2	10.1
30 m	5.8	8.5	13.9	19.4	27.0
50 m	9.3	13.7	22.7	31.6	45.0

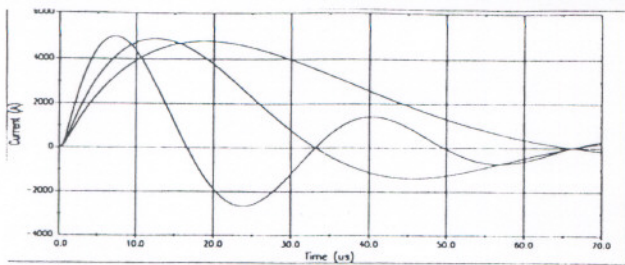


Figure 8 - Three surge current waveforms with different rise times used to compute the values of Table 2

Figure 8 shows three waveforms of same amplitude, with nominal rise time of 5 μ s, 10 μ s, and 20 μ s, obtained by taking half or double of the frequency used in Eq. (2). The actual rise time [$1.25 \times (\text{time from } 10\% \text{ to } 90\%)$], as opposed to the nominal rise time used to describe the waveforms, was computed as well as the maximum rate of rise for each wave. The maximum rate of rise (which is obtained when the second derivative of the current is equal to zero) occurs initially, once the gentle toe is over, and determines the maximum resulting voltage produced by the inductive effect. Table 2 shows the corresponding values of the rise time, maximum rate of rise, and resulting voltage for a branch circuit length of 10 m and amplitude of 5 kA. Note that for a 1-to-4 increase in nominal rise time, the maximum di/dt decreases only by one half, with the same decrease appearing in the resulting voltage, showing once again that initial rate of rise is more important than rise time and amplitude.

TABLE 2

Effect of the rate of rise of the postulated current on the resulting voltage at the upstream end of the branch circuit

Nominal rise time, μ s	5	10	20
Actual rise time, μ s	4.3	9.5	13.5
Maximum di/dt , A/ μ s	1250	850	630
Resulting voltage, kV	7.0	5.2	3.6

In the scenario tested and modeled so far, no flashover possibility was considered. Nevertheless, the values shown in Table 1 clearly indicate that some real-world circuit lengths and surge parameters postulated in some SPD application standards under development can produce high upstream voltages that will cause a flashover of the upstream wiring devices.

C. The paradox of "more begets less"

Common-sense intuition might lead the unwary to expect that higher surge currents would impose a greater stress on the circuit components, including the downstream varistor. Also, a longer branch circuit, with its corresponding higher inductance, could be expected to have the capability of storing more energy during build-up of the surge current toward the downstream varistor, into which that stored energy ultimately has to be dissipated. Cascade coordination studies [4], [6], [8], have shown that in some cases, the downstream varistor continues to carry current long after the impinging surge current has gone past its peak.

To explore the validity of such expectations, we performed tests and modeling, with an actual gap in the test circuit, and a switch in the model circuit, to bypass the current at the upstream end when sparkover voltage is attained. By measuring the current that flows in the branch circuit toward the downstream varistor and the voltage across the varistor, the energy deposited in the varistor during the total surge event can be determined. Likewise, the modeling can determine the current in the varistor, hence the voltage across it, and allow computation of the energy.

In [4], agreement was reported between, on the one hand, computing the deposited energy through actual measurement of the current and voltage, followed by computation of the energy by means of the digital signal analyzer used for measurements and, on the other hand, the model computations. Therefore, in the tests reported here, we were satisfied to verify waveform agreement between the actual varistor current measurement and the computed varistor current, and let the model alone compute the energy deposited in the downstream varistor.

Figure 9 shows the real-world recording of the situation that develops for a "clearance" sparkover of 2 kV. This relatively low value, compared to the 6 kV to 10 kV level that we might expect from typical low-voltage wiring devices, is made necessary for the test case where only 9 meters of branch circuit were considered, and the setting of the surge generator was maintained at the same nominal 3 kA short-circuit current. The object, of course, is to demonstrate that the clearances are likely to flash over, as indicated by progressively higher values of the necessary upstream driving (or resulting) voltage shown in Table 1.

Under the conditions of Figure 9, sparkover of the gap occurred at approximately 1 μ s. After sparkover, the current delivered by the surge generator is the sum of the currents in the gap and in the branch circuit. Its peak (3.2 kA) is greater than those of Figures 2 and 5 because the generator does not need to overcome the varistor that reduced the voltage available for driving the current, nor the impedance of the 9 meters of cable.

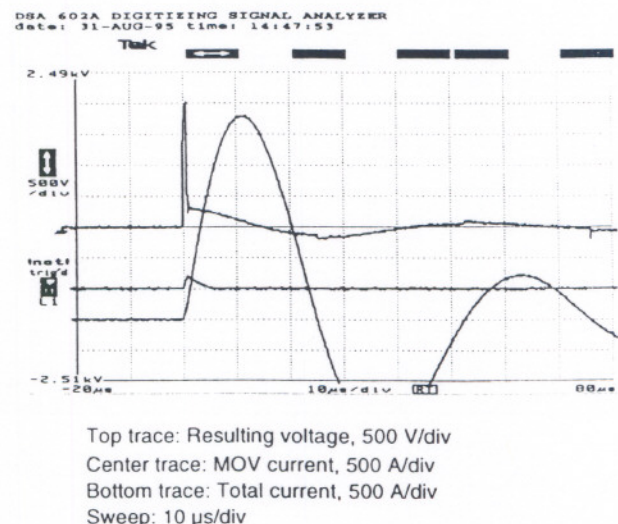


Figure 9 - Voltage and currents with gap sparkover at 2 kV

Figures 10 and 11 show the results obtained by the model for voltages and current in the circuit. In the modeling, only one current waveform was applied to the circuit, the one prevailing until flashover occurs, which the postulated current-source real world would maintain. In contrast, the surge current delivered by the surge generator (Figure 9) increases after the flashover, but that is not relevant to our consideration of what happens to the circuit before and up to the time of flashover.

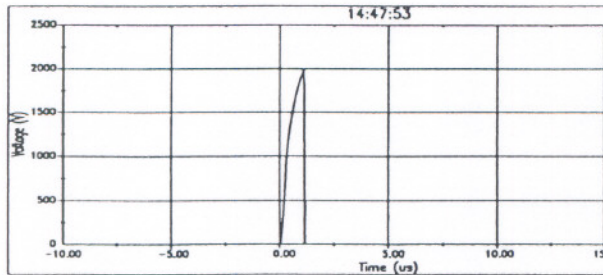


Figure 10 - Voltage across the gap set to sparkover at 2 kV

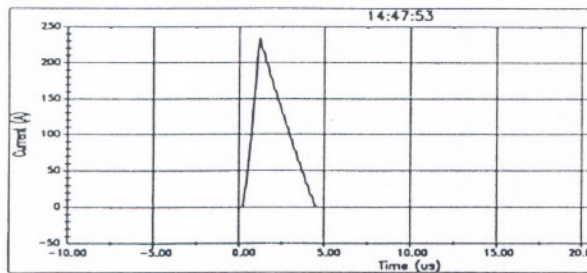


Figure 11 - Current in downstream varistor

The waveforms of Figures 10 and 11 are shown with an expanded scale, compared to that of Figure 9, that gives a better resolution for the gap voltage and current in the varistor. There is good correspondence between the waveforms of the two traces and the gap voltage and downstream current traces of Figure 9. In Figure 10, however, the gap voltage collapses to zero, while it does not in Figure 9. The difference is that the real-world circuit has a parasitic inductive voltage added to the true gap voltage, already discussed for the varistor of Figure 2. Figure 11 shows the linear ramps typical of current changes in an inductance.

As mentioned above, we can expect that the energy deposited in the downstream varistor for a given impinging surge will be influenced by the length of the branch circuit. Using the model developed and validated according to Figures 5 and 6, the energy can be readily computed. In the case described by Figures 9, 10, and 11, the gap sparkover voltage was preset at 2 kV so that sparkover could indeed occur for the surge current available from the real-world generator and the resulting upstream voltage.

Now that we are in the (validated) model-world, we can arbitrarily set the sparkover voltage at a level more typical of the flashover point of clearances, say 6 kV. Of course, we have the possibility of assessing energy for a wide range of parameters.

In the example reported below, we kept the same three values of branch circuit length and performed the computations for the same five values of impinging current as those used for the computations of Table 1. Table 3 shows the energy deposited in the downstream varistor for these combinations of branch circuit length and peak current values, for the applied current waveform of Figure 5, and a 6 kV flashover point.

TABLE 3

Energy deposited into a 130-V rated far-end varistor as a function of the branch circuit length shown (rows), current peak (columns) of waveform shown in Figure 5, and flashover of the clearances set to occur at 6 kV

Peak/Length	2 kA	3 kA	5 kA	7 kA	10 kA
10 m	17 J	27 J	51 J	670 mJ	218 mJ
30 m	17 J	128 mJ	30 mJ	23 mJ	18 mJ
50 m	69 mJ	34 mJ	17 mJ	11 mJ	10 mJ

The results shown in Table 3 merit close examination as they reveal some counter-intuitive trends: we might have expected that for higher impinging current values, the resulting energy deposited in the downstream varistor would be higher. Likewise, we might also have expected that for a longer branch circuit, the greater inductance would store more energy, ultimately to be deposited in the varistor. In fact, the opposite occurs. The table also reveals the interesting finding that the first three lower-current, short-line cases (**bold face** type in the table) produce larger energy deposition, compared to the other cases. Actually, the explanation that follows is simple and might be anticipated (especially with hindsight, illustrating that intuition is a hazardous process when dealing with nonlinear circuit components).

Starting with the second observation (more joules at lower threat levels), we have a beautiful illustration of the *blind spot* effect -- not limiting tests and designs to the maximum stress of a worst-case scenario -- [13]: for 10 meters of circuit and at the lower current levels, the resulting voltage at the clearance is not sufficient to cause flashover, and all the energy has to go to the downstream varistor. At the higher threat level of 7 kA, the voltage produced in the inductance of 10 meters of line, added to the varistor voltage, is sufficient to sparkover the 6 kV gap, relieving the varistor from further involvement beyond that of discharging the energy stored in the line. In the case of the 30-m long line, this transition occurs between 2 kA and 3 kA.

Turning now to the first observation, that higher current or greater inductance result in less stress, this apparent paradox is caused by the fact that with the higher values of di/dt and L , the voltage at the clearance rises more quickly to the flashover point. Consequently, the build-up of energy in the line inductance is shut-off earlier so that the current level in the line reached at that point is lower and, in spite of the greater inductance, the stored energy $\frac{1}{2} L i^2$ is lower for higher applied current peaks and longer branch circuits.

IV. CONCLUSIONS

The development of a validated EMTP model using existing computational tools allows us to look into all scenarios of surge propagation and surge mitigation schemes. The reality check proposed by the measurements and modeling reported in this paper should be useful in the process of selecting stress levels to be specified in the application of SPDs downstream from the service entrance, from the point of view of successful cascade coordination as well as integrity of electromagnetic compatibility. Specific conclusions can be drawn:

1. Realistic surge current amplitudes and rise times can be defined for SPDs installed at the end of branch circuits, with upper limits set by the laws of physics applied to real-world conditions.
2. The general practice for describing surge waveforms is to cite "rise time" or "front time", followed by duration, as in 8/20. However, when the effects of circuit inductance are assessed, in particular by numerical modeling, the maximum rate of rise must be considered, not an average over the rise time. It is especially important to define the conditions at the origin of the waveform, such as inclusion of a gentle toe.
3. The importance of looking for blind spots is, once again, demonstrated by the parametric computations, a much simpler task than exhaustive equipment-exhausting tests.
4. Reliable computational tools make it possible to obtain a wide range of parametric assessments, and thus avoid recourse to intuition when dealing with nonlinear circuits, where blind reliance on common-sense may lead to flawed conclusions.
5. The parametric computations offered in the paper point out the need to consider a balance or trade-off among several critical factors in the design of branch circuit protection, in particular the uncontrollable length of branch circuits in actual installations.

V. ACKNOWLEDGMENTS

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Arshad Mansoor (M' 1995) is Electrical Systems Engineer at the EPRI Power Electronics Applications Center (PEAC). He received his MS and Ph.D. in electrical engineering from the University of Texas, Austin, in 1992 and 1994 respectively. His areas of interest include power quality, power systems transients, harmonics, surge protection, and EMTP model development.

François Martzloff (M' 1956, F' 1983) Born and educated in France, with additional MS degrees from Georgia Tech and from Union College, worked at General Electric for 29 years and now ten years at the National Institute of Standards and Technology. He is contributing to several committees for development of standards on EMC and surge protection in the IEEE and the IEC.