High-Frequency Behavior of Coupled CMOS Interconnects Built in Different Metallization Layers

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***Abstract*- In this paper we apply a broadband measurement method to determine the propagation characteristics of coupled-line structures fabricated in different metallization layers of a 0.25 µm CMOS technology. We show that the matrices of frequency-dependent line parameters, as extracted from calibrated four-port S-parameter measurements, agree well with data predicted by numerical calculations, and discuss the impact of metal level height above the substrate on the transmission characteristics.**

INTRODUCTION

Most of the recent publications dealing with the experimental characterization of coupled transmission lines built in CMOS technology report on symmetric coupled lines [1,2]. The measurement method used in this paper, which is based on the procedure introduced in [3], has been demonstrated for asymmetric coupled lines built in CMOS technology [4], and is equally well suited for symmetric coupled lines on silicon [5]. However, to the authors' knowledge, no measurement results have yet been reported for identical coupled line geometries built in different metallization layers. In this paper, we investigate the performance of the measurement method presented in [4] for asymmetric coupled lines built in different metal levels of a 0.25 µm CMOS technology. We study both coupled conductors in one of the top metallization layers, as well as coupled conductors in a layer close to the substrate's surface.

Figure 1 shows a cross section of the asymmetric coupled lines we studied. We investigated two different test-structure geometries, which we will refer to as experiment I and experiment II. In experiment I the signal conductors are fabricated on the second metal level of the six-metal-layer CMOS technology, which is near the substrate. In experiment II the signal conductors are fabricated on the fifth

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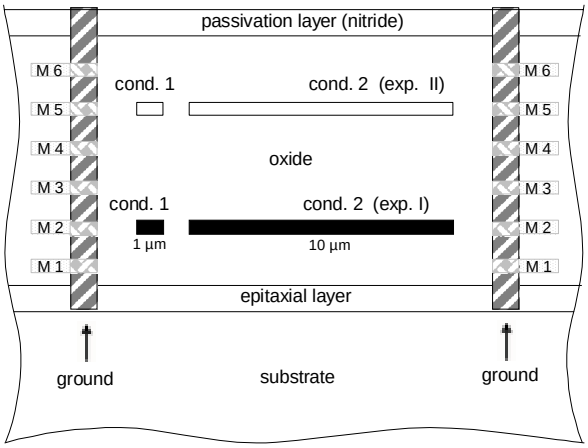

Fig. 1. Cross section of the asymmetric coupled lines.

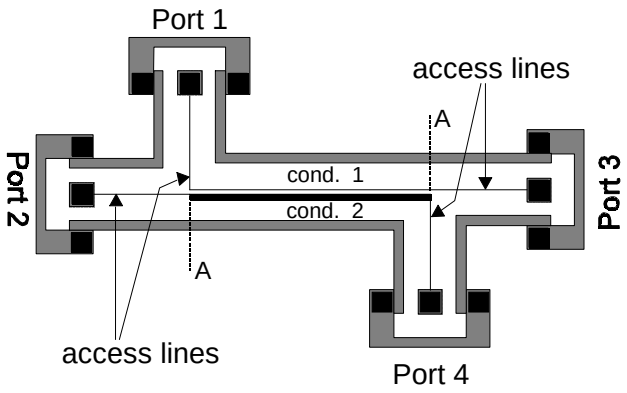

Fig. 2. Top view of the test structures.

metal level, much farther from the substrate. In both experiments the first signal conductor has a width of 1 µm, the second a width of 10 µm, and the two signal conductors are separated by a gap of 1 µm. The thickness of metal 2 is 0.7 µm, and the thickness of metal 5 is 1.1 µm. The metal conductivity is 27.8×10^6 S/m, and the conductivity of the silicon substrate is 10^4 S/m. The asymmetric coupled lines are surrounded by 20 µm wide grounds that are connected to the substrate with via arrays connected through all six metallization layers. The distance between the grounds and the center of the coupled-line structure is 65 µm.

Fig. 2 shows the top view of the coupled-line test structures. We used on-wafer probes to connect to four 50 µm by 50 µm contact pads fabricated in the top metal layer (metal 6). These are labeled ports 1-4 in Fig. 2. In experiment I vias connect the signal pads on metal 6 to the access lines on metal 2, and in experiment II vias connect the signal pads on metal 6 to the access lines on metal 5. These access lines connect the pads to the coupled-line segment, which we wish to characterize, on the same metal layer. The width of the access lines is 1 µm, and their length is 200 µm. These coupled lines were fabricated with lengths of 0.5 mm, 1.0 mm and 2.5 mm.

MEASUREMENT AND DEEMBEDDING PROCEDURE

We used two-port measurements to characterize the contacts and access lines and four-port measurements to characterize the coupled-line system. We employed the method of [6], which is designed to account for large contact-pad capacitances on lossy substrates, with a coplanar-waveguide reference calibration to measure the characteristic impedance Z_0 of the access lines, and determined the propagation constant from a

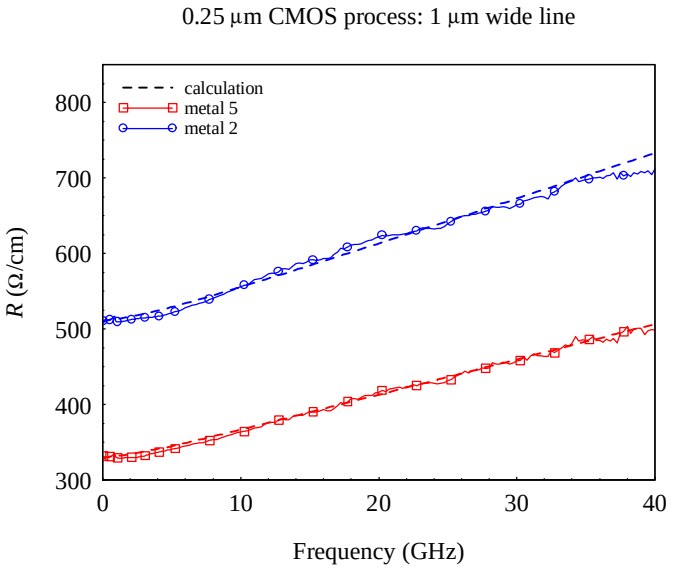

Fig. 3. Resistance per unit length of the access lines.

multiline Thru-Reflect-Line (TRL) calibration [7]. We verified the measurements using the quasi-analytic calculations described in [8].

Figure 3 shows that the measured and calculated resistance per unit length of the 1 µm wide access lines agrees very well. We found similar agreement between measurement and calculation for the other line parameters.

The calibration procedure used for the four-port measurement is described in [9]. The procedure eliminates the need for orthogonal calibration standards, and requires only three in-line calibrations. To this end, we again used the multiline TRL calibration of [7] with coplanar-waveguide standards. We moved the initial reference plane position of this four-port calibration [9] in the coplanar waveguide near the probe tips. At this point we still required an additional deembedding step to account for the silicon contact pads and access lines. We employed the error boxes we determined from our second-tier two-port calibrations to account for these contact pads and access lines. Here we used the propagation constant from the TRL calibration to locate the reference planes of this final 4-port calibration at the beginning of the coupled line segment, and the calibration comparison method [6] to set the reference impedance to 50 Ω.

EXPERIMENTAL RESULTS

We determined the matrices of the line parameters $\boldsymbol{R}_c$, $\boldsymbol{L}_c$, $\boldsymbol{G}_c$, and $\boldsymbol{C}_c$ in the conductor representation of [10], choosing voltage paths between each of the two signal conductors and ground. In our analysis, we ignored the four-port error boxes that represent the discontinuities between the single-mode access lines and the multi-mode coupled-line segment.We estimated the line parameter matrices from the four-port measurement data using ODRPACK, an implementation of the weighted orthogonal distance regression algorithm of [11], using the procedure described in [4].

Figures 4, 5 and 6 compare the measurement results for the asymmetric coupled lines of experiments I and II with calculated quasi-analytic data of [8]. The agreement between measured and calculated values is good over the entire frequency band, thereby demonstrating that the method of [4] is applicable to the characterization of coupled line systems in arbitrary metallization layers of current CMOS processes. However, at the frequency of 2 GHz, a systematic measurement error, which is still under investigation, is apparent in Figures 5 and 6.

From [4] we know that the matrices of resistances $\boldsymbol{R}_c$ and inductances per unit length $\boldsymbol{L}_c$ can be frequency dependent for CMOS interconnects built on highly conductive substrates, whereas the matrix of capacitance per unit length $\boldsymbol{C}_c$ usually stays constant with frequency. The conductance per unit length $\boldsymbol{G}_c$ plays only a minor role in signal propagation. Figures 4 and 5 show that the matrix components for the resistance per unit length increase significantly with frequency in both experiments, which can be explained by the fact that the magnetic field penetrates deeply into the substrate, leading to a strong skin effect in the highly conductive silicon substrate.

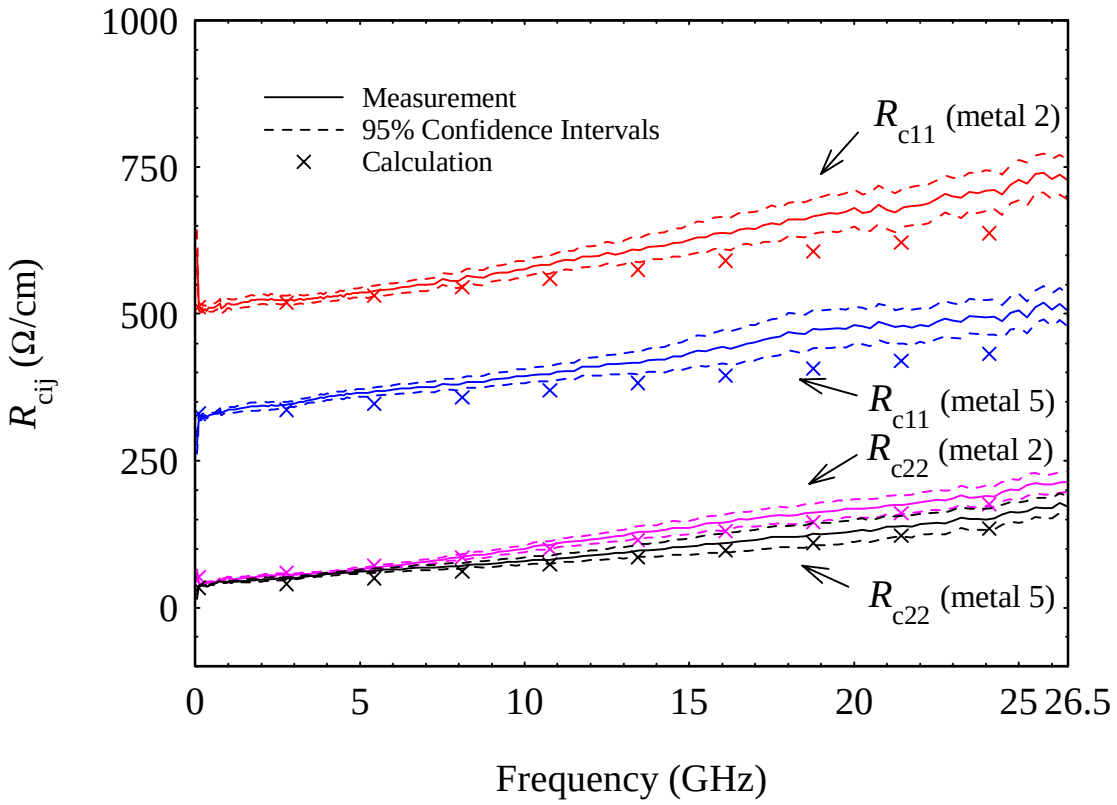

Fig. 4. Resistances per unit length for the asymmetric coupled lines of Figures 1 and 2. For reasons of clarity the line parameter R_{c12} is not shown here (see Fig. 5).

The frequency-dependent resistance per unit length R_{c22} of Fig. 4, which corresponds to the 10 µm wide conductor of Fig. 1, increases more rapidly with frequency when the signal conductor is on metal 2 than when it is on metal 5. However, for the 1 µm wide conductor, the slope of the frequency-dependent resistance per unit length R_{c11} appears to be identical for signal conductors on metal 2 and metal 5. This indicates that the wider lines are more strongly affected by the vicinity to the substrate than the narrower lines are.

Figure 5 compares the frequency-dependent resistance per unit length R_{c12} in metal 2 and metal 5. This quantity is a measure of the influence of the return current flowing in the substrate due to the skin effect there. The agreement between measured and calculated data is excellent for both metal levels. R_{c12} of metal 2 increases more rapidly with frequency than does R_{c12} of metal 5, which clearly shows that the influence of the skin effect in the substrate is more pronounced for the structures closer to the substrate surface.

Finally, Fig. 6 compares the frequency-dependent mutual inductance per unit length L_{c12} in metal 2 and metal 5. Here the agreement between measured and calculated values is not so good, which may be due to the assumption made in the quasi-analytic calculations of [8] that the grounds are approximated by infinitely thin conductors connected to the substrate. While this is only a very rough approximation of the ground stack shown in Fig. 1, the tendencies indicated by the calculations are nevertheless comparable to those in the measured data. The figure shows that the mutual inductance decreases with frequency due to

the increasing skin effect in the substrate in both metal 2 and metal 5, but the effect in metal 2 is more pronounced. This is consistent with the close proximity of metal 2 and the substrate, and is consistent with the resistance data shown in Figs. 4 and 5.

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REFERENCES

[1] Y. Eo, W. R. Eisenstadt, J.Y. Jeong, and O. Kwon, "A New On-Chip Interconnect Crosstalk Model and Experimental Verification for CMOS VLSI Circuit Design", *IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 129-140, January 2000.

[2] D. E. Bockelman and W. R. Eisenstadt, "Direct Measurement of Crosstalk Between Integrated Differential Circuits", *IEEE Trans. Microwave Theory Tech.*, vol. 48, no. 8, pp. 1410-1413, August 2000.

[3] D. F. Williams, J. E. Rogers, and C. L. Holloway, "Multiconductor Transmission Line Characterization: Representations, Approximations, and Accuracy", *IEEE Trans. Microwave Theory Tech.*, vol. 47, no. 4, pp. 403-409, April 1999.

[4] U. Arz, D. F. Williams, D. K. Walker, J. E. Rogers, M. Rudack, D. Treytnar, and H. Grabinski, "Characterization of Asymmetric Coupled CMOS Lines", *2000 IEEE MTT-S Symposium Dig.*, pp. 609-612, June 11-16, 2000.

[5] U. Arz, D. F. Williams, D. K. Walker, and H. Grabinski, "Accurate Electrical Measurement of Coupled Lines on Lossy Silicon", *2000 EPEP Conference Dig.*, October 23-25, 2000.

[6] D. F. Williams, U. Arz, and H. Grabinski, "Accurate Characteristic Impedance Measurement on Silicon", *1998 IEEE MTT-S Symposium Dig.*, pp. 1917-1920, June 9-11, 1998.

[7] R. B. Marks, "A Multiline Method of Network Analyzer Calibration", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-39, no. 7, pp. 1205-1215, July 1991.

[8] E. Grotelüschen, L. S. Dutta and S. Zaage, "Quasi-analytical Analysis of the Broadband Properties of Multiconductor Transmission Lines on Semiconducting Substrates", *IEEE Trans. Comp., Packag., and Manufact. Tech.-Part B*, vol. 17, pp. 376-382, Aug. 1994.

[9] D. F. Williams and D. K. Walker, "In-line Multiport Calibration", *51st ARFTG Conf. Dig.*, pp. 88-90, June 12, 1998.

[10] D. F. Williams, L. A. Hayden, and R. B. Marks, "A Complete Multimode Equivalent-Circuit Theory for Electrical Design", *J. Res. Natl. Inst. Stand. Technol.*, vol. 102, no. 4, pp. 405-423, July - Aug.1997.

[11] P. T. Boggs, R. H. Byrd, and R. D. Schnabel, "A Stable and Efficient Algorithm for Nonlinear Orthogonal Distance Regression", *SIAM J. Sci. Stat. Comput.*, pp. 1052-1078, Nov. 1987.

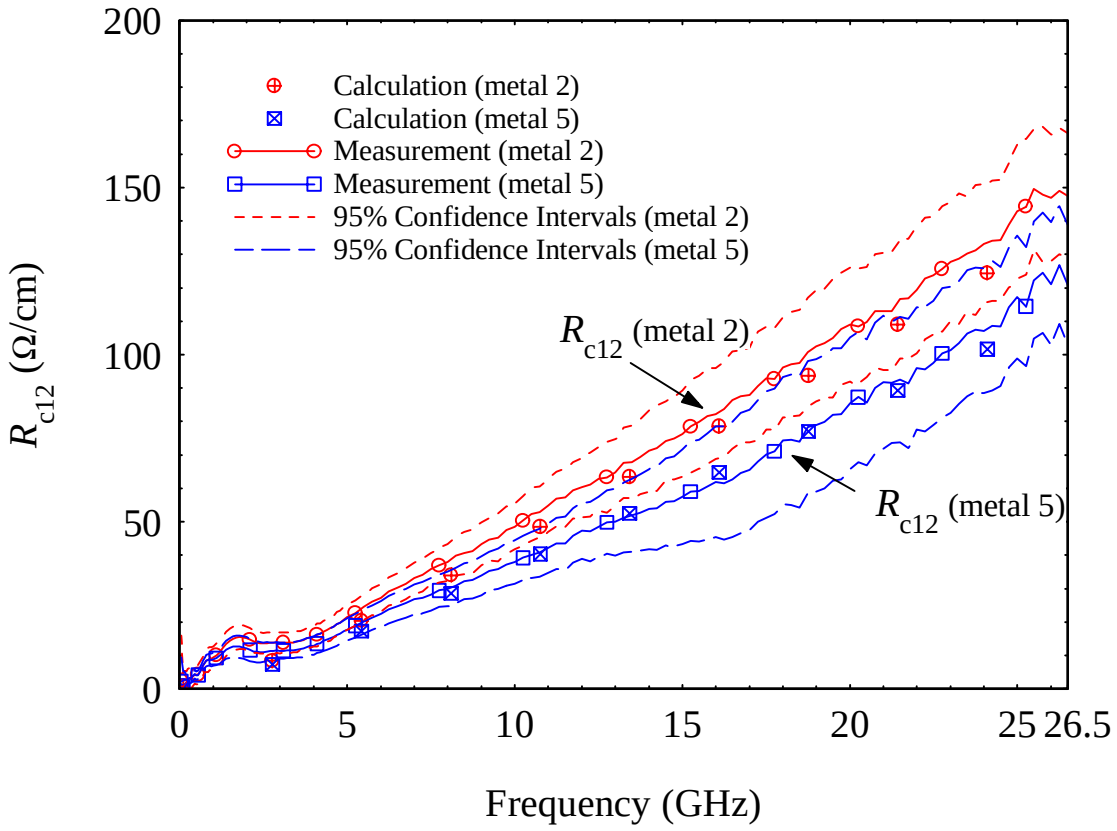

Fig. 5. Resistance per unit length R_{c12} for the asymmetric coupled lines of Figures 1 and 2.

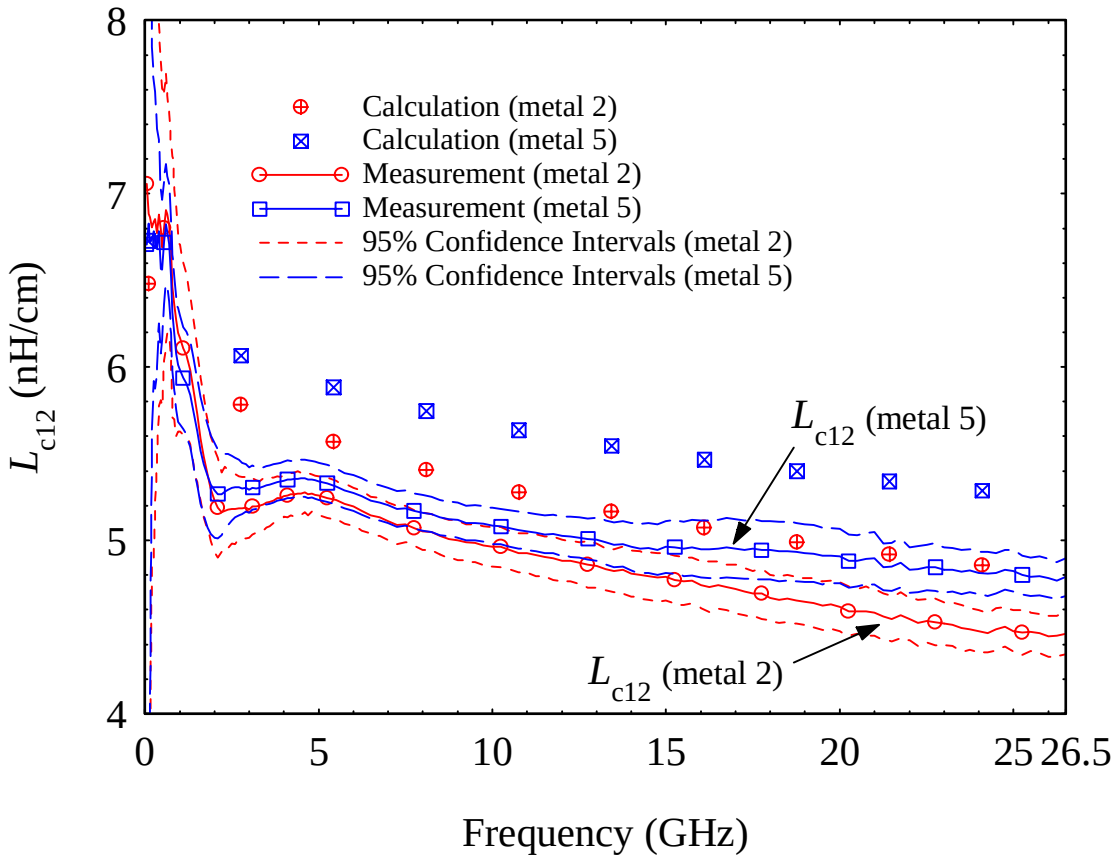

Fig. 6. Resistance per unit length L_{c12} for the asymmetric coupled lines of Figures 1 and 2.